# Self-Protected Low Side Driver with Temperature and Current Limit

# NCV8402, NCV8402A

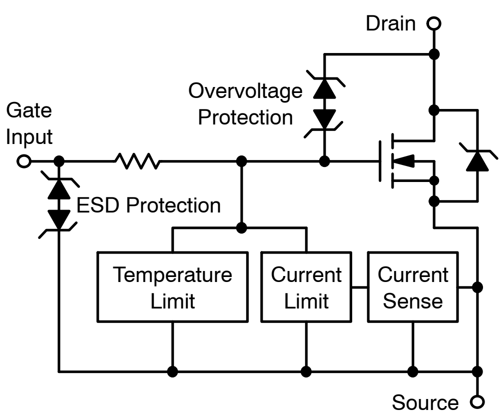
NCV8402/A is a three terminal protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

### Features

- Short−Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- NCV8402AMNWT1G − Wettable Flanks Product
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial



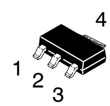

**ON Semiconductor**®

www.onsemi.com

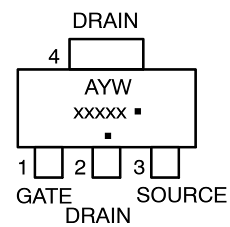
| $V_{(BR)DSS}$ (Clamped) | $R_{DS(ON)}$ TYP | $I_D$ MAX |
|---|---|---|
| 42 V | 165 mΩ @ 10 V | 2.0 A* |

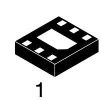
*Max current limit value is dependent on input condition.

### MARKING DIAGRAMS

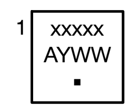


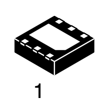

**SOT−223**
**CASE 318E**
**STYLE 3**



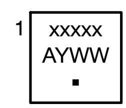




**DFN6**
**CASE 506AX**



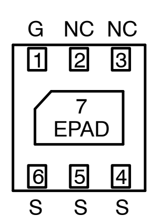

**DFN6 (WF)**
**CASE 506DK**




A = Assembly Location
Y = Year
W or WW = Work Week
xxxxx = V8402 or 8402A
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### DFN6 PACKAGE PIN DESCRIPTION




| Pin # | Symbol | Description |
|---|---|---|
| 1 | G | Gate Input |
| 2 | NC | No Connect |
| 3 | NC | No Connect |
| 4 | S* | Source |
| 5 | S* | Source |
| 6 | S* | Source |
| 7 | EPAD | Drain |

*Pins 4, 5, 6 are internally shorted together. It is recommended to short these pins externally.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain−to−Source Voltage Internally Clamped | | $V_{DSS}$ | 42 | V |
| Drain−to−Gate Voltage Internally Clamped | ($R_G$ = 1.0 MΩ) | $V_{DGR}$ | 42 | V |
| Gate−to−Source Voltage | | $V_{GS}$ | ±14 | V |
| Continuous Drain Current | | $I_D$ | Internally Limited | |
| Total Power Dissipation − SOT−223 Version | @ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2)<br>@ $T_S$ = 25°C) | $P_D$ | 1.1<br>1.74<br>8.9 | W |
| Total Power Dissipation − DFN Version | @ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2)<br>@ $T_S$ = 25°C) | $P_D$ | 0.76<br>1.78<br>8.9 | W |
| Maximum Continuous Drain Current − SOT−223 Version | @ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2)<br>@ $T_S$ = 25°C) | $I_D$ | 1.54<br>1.94<br>6.75 | A |
| Maximum Continuous Drain Current − DFN Version | @ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2)<br>@ $T_S$ = 25°C) | $I_D$ | 1.28<br>1.97<br>6.75 | A |
| Thermal Resistance | SOT223 Junction−to−Ambient Steady State (Note 1)<br>SOT223 Junction−to−Ambient Steady State (Note 2)<br>SOT223 Junction−to−Soldering Point Steady State<br><br>DFN Junction−to−Ambient Steady State (Note 1)<br>DFN Junction−to−Ambient Steady State (Note 2)<br>DFN Junction−to−Soldering Point Steady State | $R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JS}$<br><br>$R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JS}$ | 114<br>72<br>14<br><br>163<br>70<br>14 | °C/W |
| Single Pulse Drain−to−Source Avalanche Energy<br>($V_{DD}$ = 32 V, $V_G$ = 5.0 V, $I_{PK}$ = 1.0 A, L = 300 mH, $R_{G(ext)}$ = 25 Ω) | | $E_{AS}$ | 150 | mJ |
| Load Dump Voltage | ($V_{GS}$ = 0 and 10 V, $R_I$ = 2.0 Ω, $R_L$ = 9.0 Ω, $t_d$ = 400 ms) | $V_{LD}$ | 55 | V |
| Operating Junction Temperature | | $T_J$ | −40 to 150 | °C |
| Storage Temperature | | $T_{stg}$ | −55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface−mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06″ thick).
2. Surface−mounted onto 2″ sq. FR4 board (1″ sq., 1 oz. Cu, 0.06″ thick).

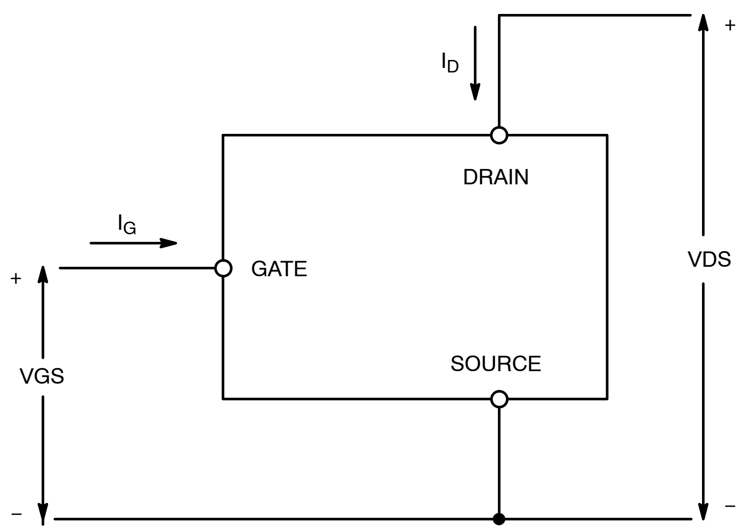



**Figure 1. Voltage and Current Convention**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage (Note 3) | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 25°C | $V_{(BR)DSS}$ | 42 | 46 | 55 | V |
| | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 150°C (Note 5) | | 40 | 45 | 55 | |
| Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V, $T_J$ = 25°C | $I_{DSS}$ | | 0.25 | 4.0 | μA |
| Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V, $T_J$ = 150°C (Note 5) | $I_{DSS}$ | | 1.1 | 20 | μA |
| Gate Input Current | $V_{DS}$ = 0 V, $V_{GS}$ = 5.0 V | $I_{GSSF}$ | | 50 | 100 | μA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 150 μA | $V_{GS(th)}$ | 1.3 | 1.8 | 2.2 | V |
| Gate Threshold Temperature Coefficient | | $V_{GS(th)}/T_J$ | | 4.0 | | −mV/°C |
| Static Drain−to−Source On−Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.7 A, $T_J$ = 25°C | $R_{DS(on)}$ | | 165 | 200 | mΩ |
| | $V_{GS}$ = 10 V, $I_D$ = 1.7 A, $T_J$ = 150°C (Note 5) | | | 305 | 400 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 1.7 A, $T_J$ = 25°C | | | 195 | 230 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 1.7 A, $T_J$ = 150°C (Note 5) | | | 360 | 460 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 0.5 A, $T_J$ = 25°C | | | 190 | 230 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 0.5 A, $T_J$ = 150°C (Note 5) | | | 350 | 460 | |
| Source−Drain Forward On Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | $V_{SD}$ | | 1.0 | | V |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| Turn−On Time (10% $V_{IN}$ to 90% $I_D$) | $V_{GS}$ = 10 V, $V_{DD}$ = 12 V, $I_D$ = 2.5 A, $R_L$ = 4.7 Ω | $t_{on}$ | | 25 | 30 | μs |
| Turn−Off Time (90% $V_{IN}$ to 10% $I_D$) | | $t_{off}$ | | 120 | 200 | μs |
| Turn−On Rise Time (10% $I_D$ to 90% $I_D$) | | $t_{rise}$ | | 20 | 25 | μs |
| Turn−Off Fall Time (90% $I_D$ to 10% $I_D$) | | $t_{fall}$ | | 50 | 70 | μs |
| Slew−Rate ON (70% to 50% $V_{DD}$) | | $-dV_{DS}/dt_{ON}$ | | 0.8 | 1.2 | V/μs |
| Slew−Rate OFF (50% to 70% $V_{DD}$) | | $dV_{DS}/dt_{OFF}$ | | 0.3 | 0.5 | V/μs |
| **SELF PROTECTION CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 4) | | | | | | |
| Current Limit | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 25°C | $I_{LIM}$ | 3.7 | 4.3 | 5.0 | A |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 150°C (Note 5) | | 2.3 | 3.0 | 3.7 | |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 25°C | | 4.2 | 4.8 | 5.4 | |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 150°C (Note 5) | | 2.7 | 3.6 | 4.5 | |
| Temperature Limit (Turn−off) | $V_{GS}$ = 5.0 V (Note 5) | $T_{LIM(off)}$ | 150 | 175 | 200 | °C |
| Thermal Hysteresis | $V_{GS}$ = 5.0 V | $\Delta T_{LIM(on)}$ | | 15 | | |
| Temperature Limit (Turn−off) | $V_{GS}$ = 10 V (Note 5) | $T_{LIM(off)}$ | 150 | 165 | 185 | |
| Thermal Hysteresis | $V_{GS}$ = 10 V | $\Delta T_{LIM(on)}$ | | 15 | | |
| **GATE INPUT CHARACTERISTICS** (Note 5) | | | | | | |
| Device ON Gate Input Current | $V_{GS}$ = 5 V $I_D$ = 1.0 A | $I_{GON}$ | | 50 | | μA |
| | $V_{GS}$ = 10 V $I_D$ = 1.0 A | | | 400 | | |
| Current Limit Gate Input Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | $I_{GCL}$ | | 0.05 | | mA |
| | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | | 0.4 | | |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GATE INPUT CHARACTERISTICS** (Note 5) | | | | | | |
| Thermal Limit Fault Gate Input Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | $I_{GTL}$ | | 0.15 | | mA |
| | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | | 0.7 | | |
| **ESD ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 5) | | | | | | |
| Electro−Static Discharge Capability | Human Body Model (HBM) | ESD | 4000 | | | V |
| | Machine Model (MM) | | 400 | | | |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL PERFORMANCE CURVES

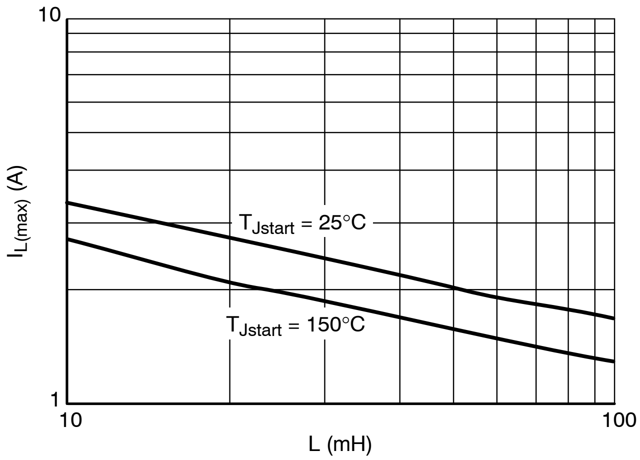



**Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance**

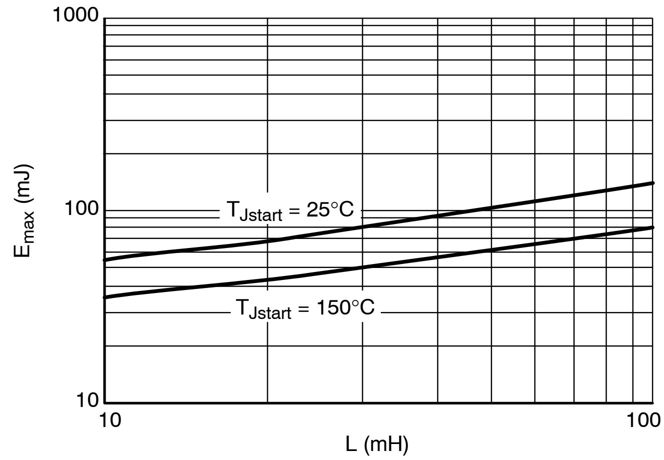



**Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance**

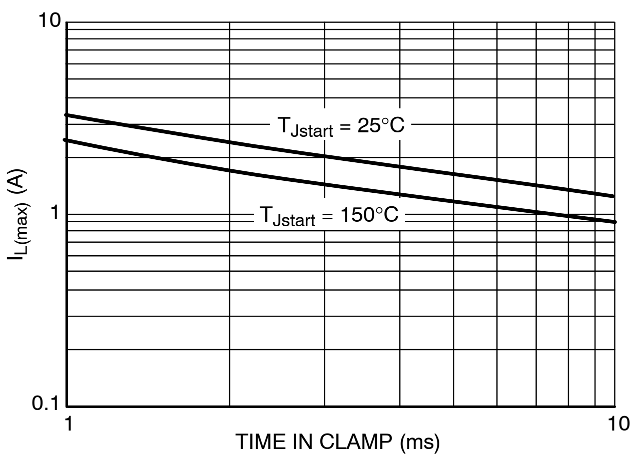



**Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp**

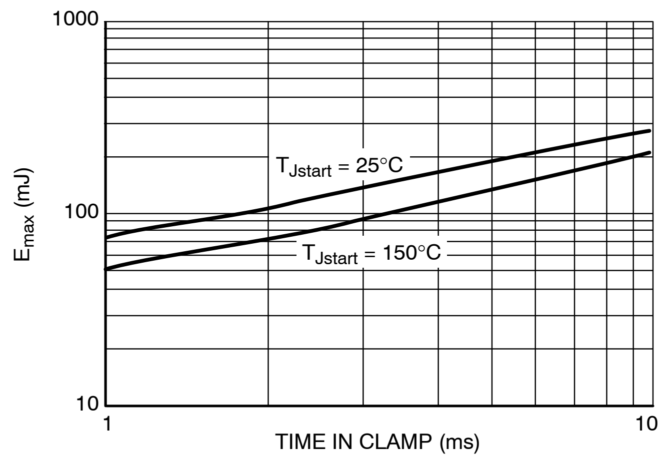



**Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp**

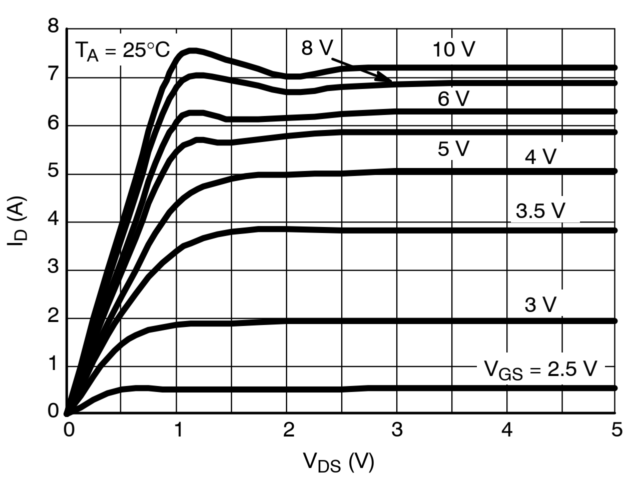



**Figure 6. On−state Output Characteristics**

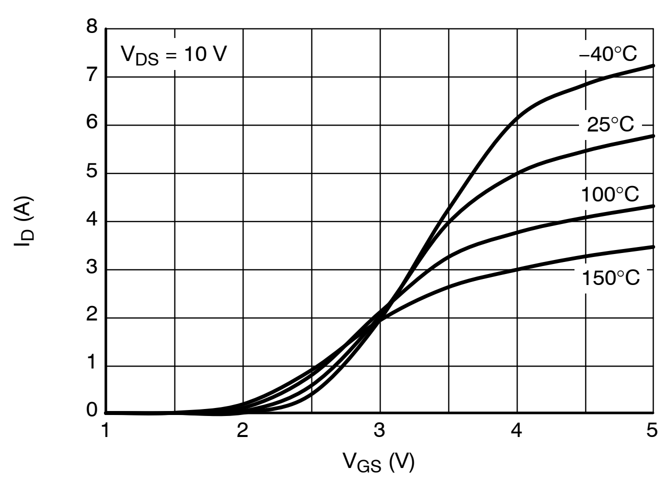



**Figure 7. Transfer Characteristics**

## TYPICAL PERFORMANCE CURVES

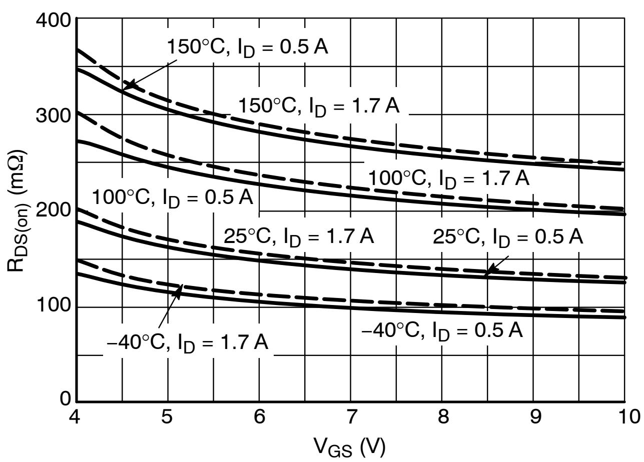



**Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage**

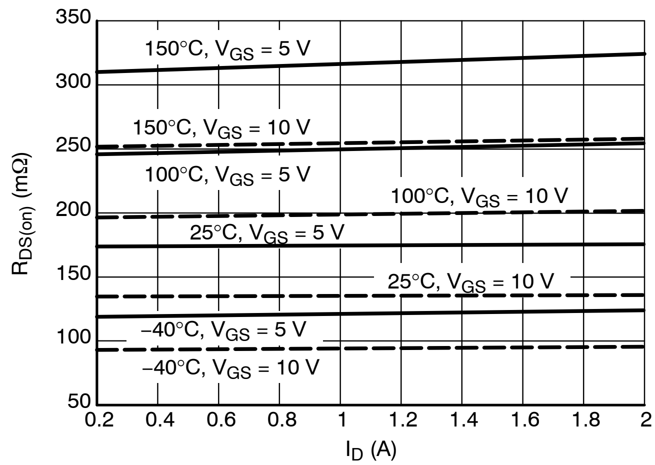



**Figure 9. $R_{DS(on)}$ vs. Drain Current**

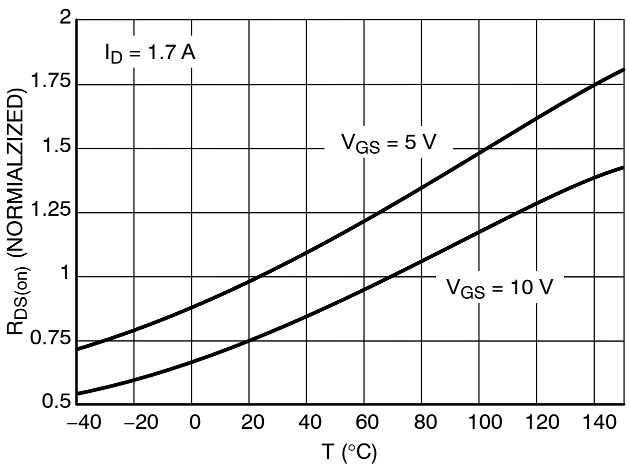



**Figure 10. Normalized $R_{DS(on)}$ vs. Temperature**

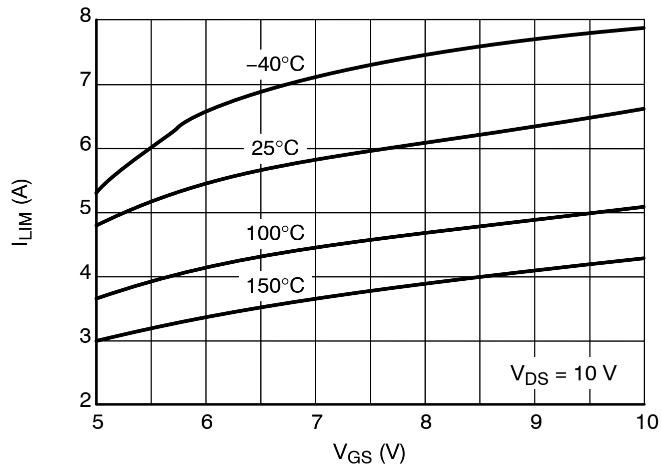



**Figure 11. Current Limit vs. Gate−Source Voltage**

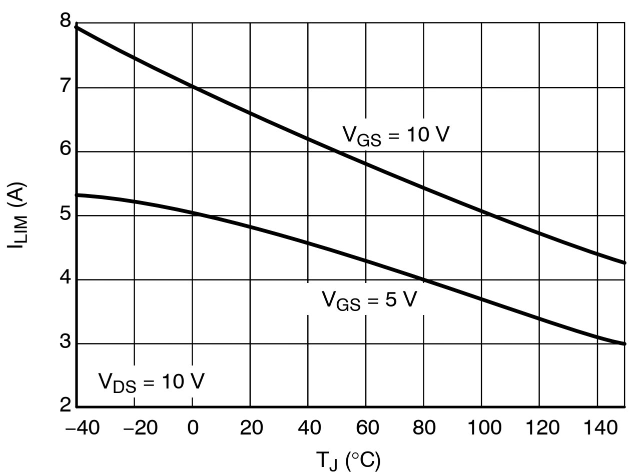



**Figure 12. Current Limit vs. Junction Temperature**

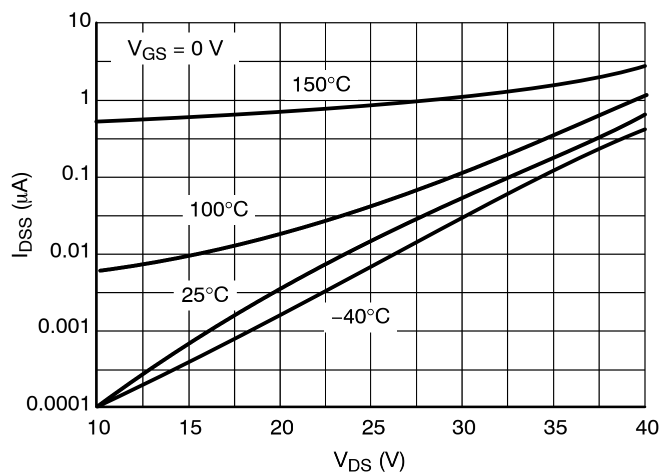



**Figure 13. Drain−to−Source Leakage Current**

## TYPICAL PERFORMANCE CURVES

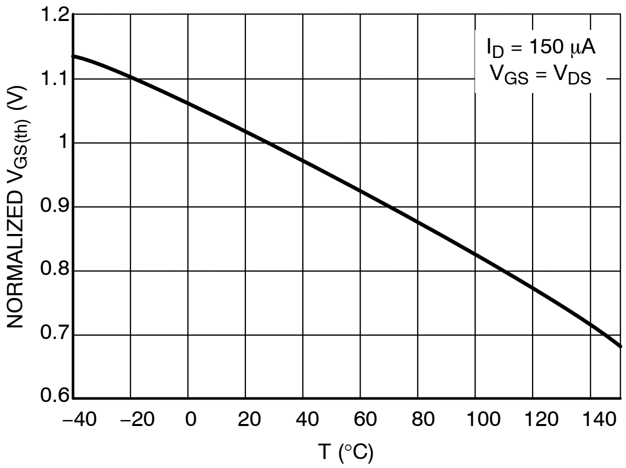



**Figure 14. Normalized Threshold Voltage vs. Temperature**

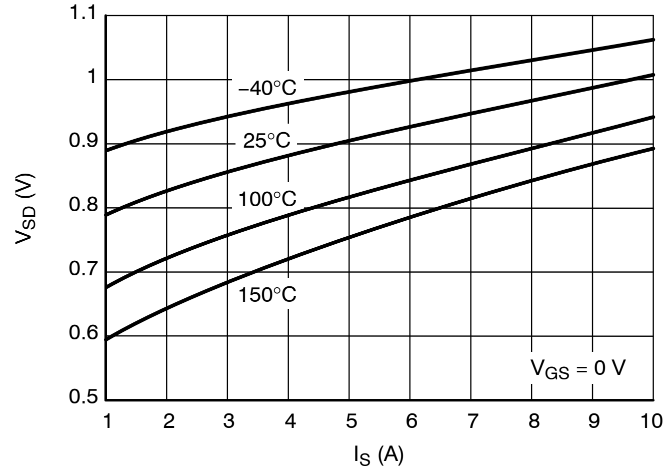



**Figure 15. Source−Drain Diode Forward Characteristics**

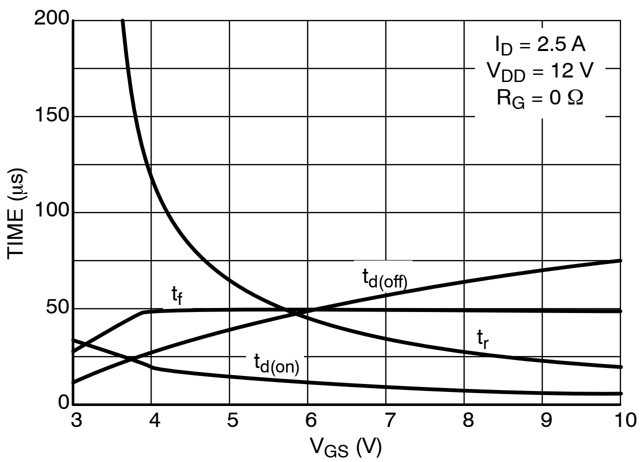



**Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage**

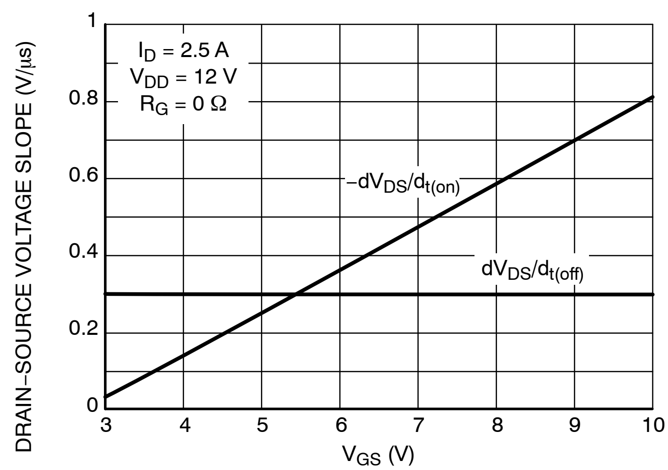



**Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage**

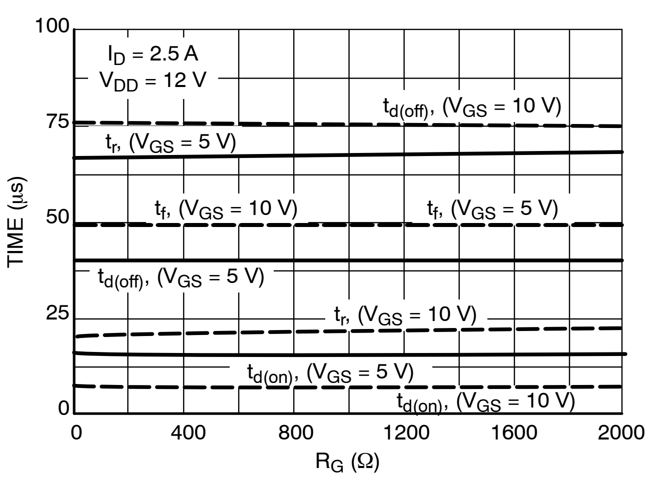



**Figure 18. Resistive Load Switching Time vs. Gate Resistance**

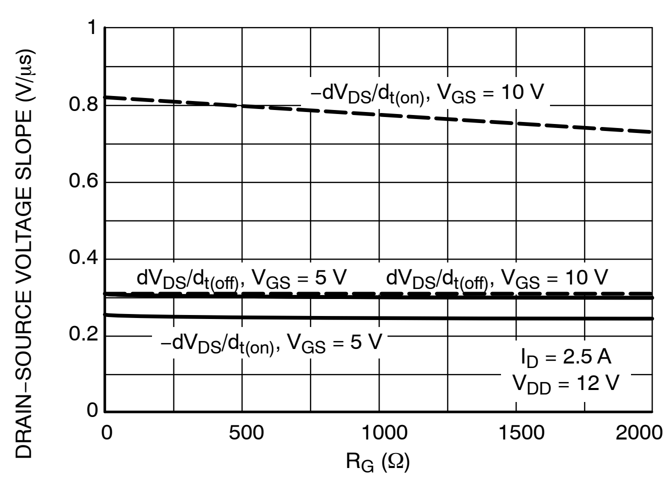



**Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance**

## TYPICAL PERFORMANCE CURVES

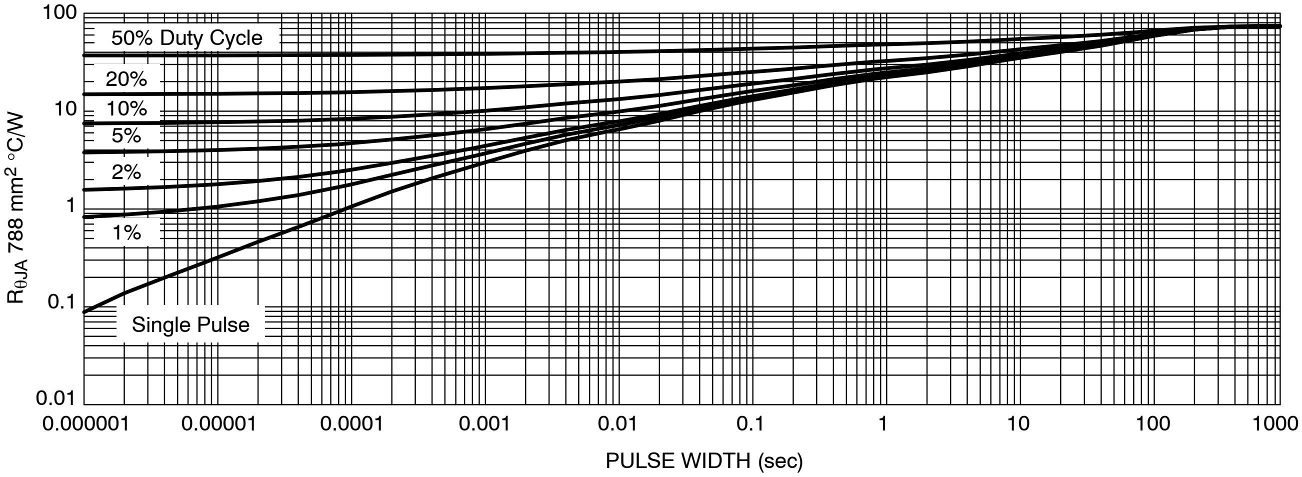



**Figure 20. Transient Thermal Resistance − SOT−223 Package**

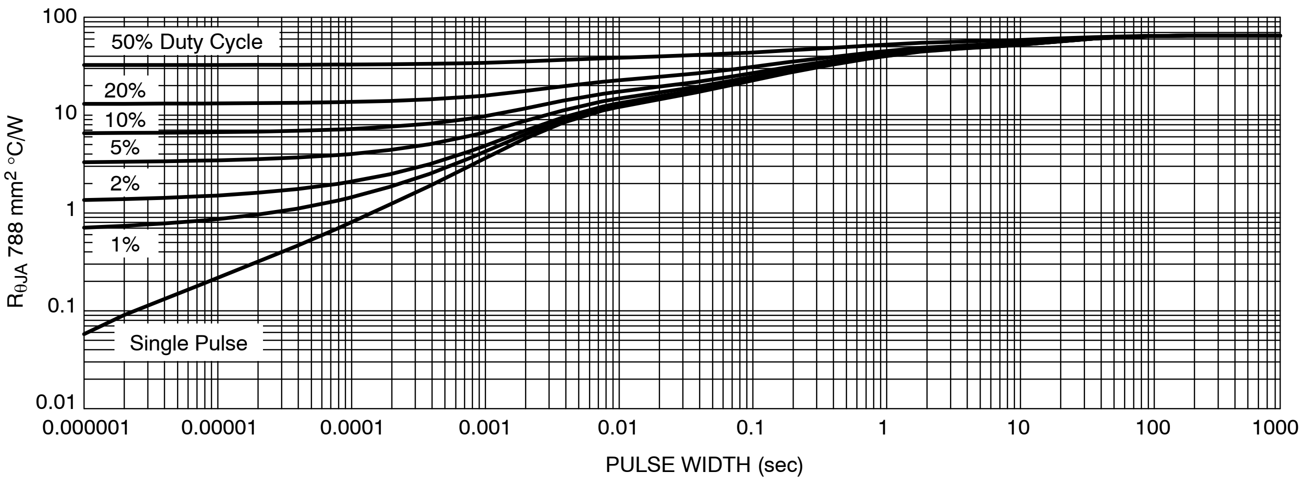



**Figure 21. Transient Thermal Resistance − DFN Package**

## TEST CIRCUITS AND WAVEFORMS

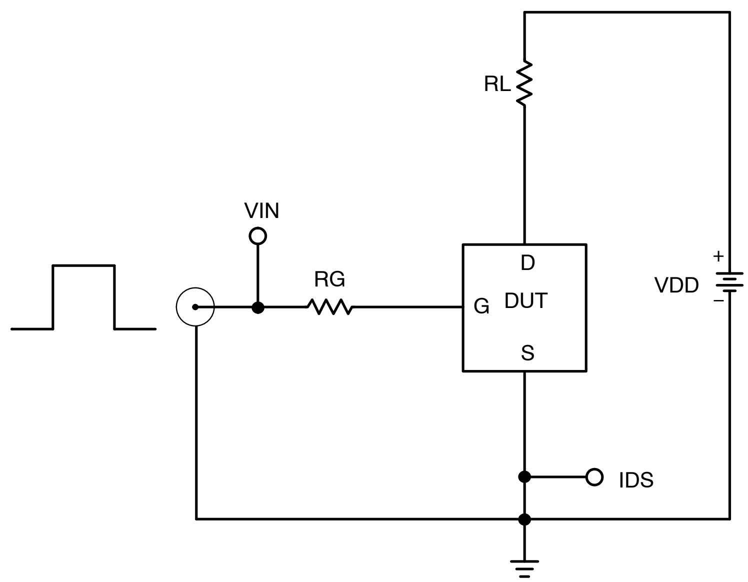



**Figure 22. Resistive Load Switching Test Circuit**

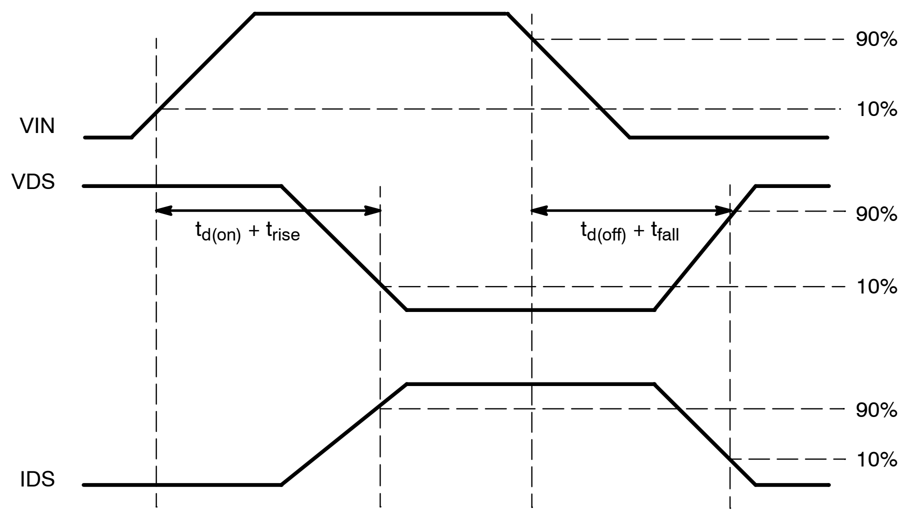



**Figure 23. Resistive Load Switching Waveforms**

## TEST CIRCUITS AND WAVEFORMS

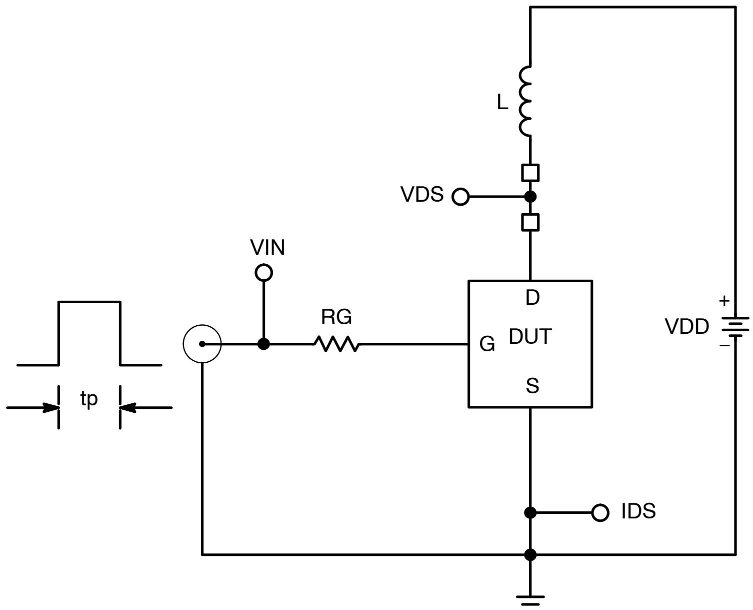



**Figure 24. Inductive Load Switching Test Circuit**

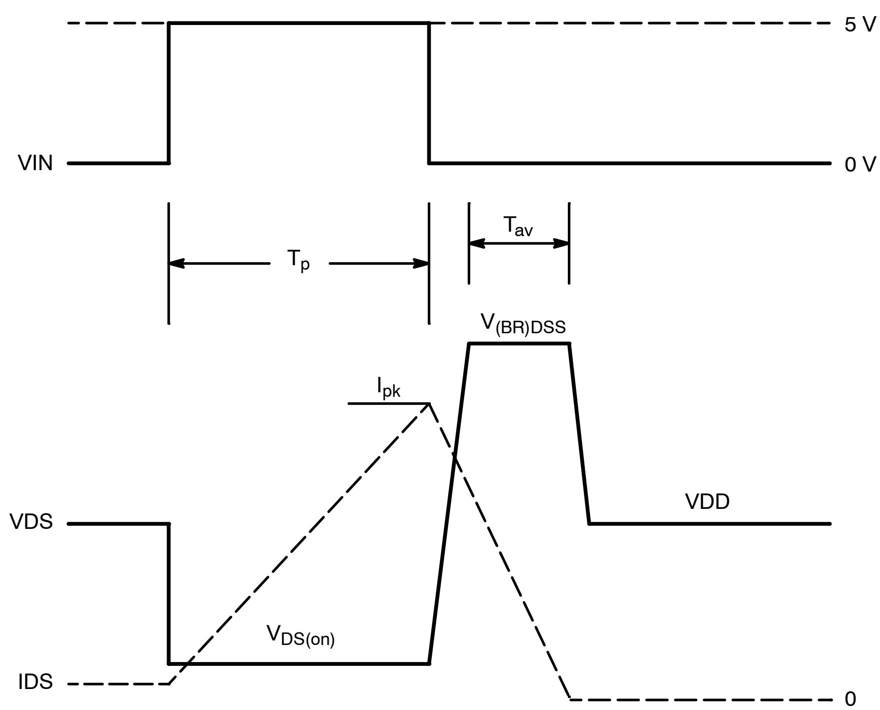


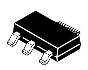

**Figure 25. Inductive Load Switching Waveforms**

## ORDERING INFORMATION

| Device* | Package | Shipping† |
|---|---|---|
| NCV8402STT1G | SOT−223 (Pb−Free) | 1000 / Tape & Reel |
| NCV8402ASTT1G | | |
| NCV8402STT3G | SOT−223 (Pb−Free) | 4000 / Tape & Reel |
| NCV8402ASTT3G | | |
| NCV8402AMNT2G | DFN6 (Pb−Free) | 2000 / Tape & Reel |
| NCV8402AMNWT1G | DFN6 (Pb−Free, Wettable Flank) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

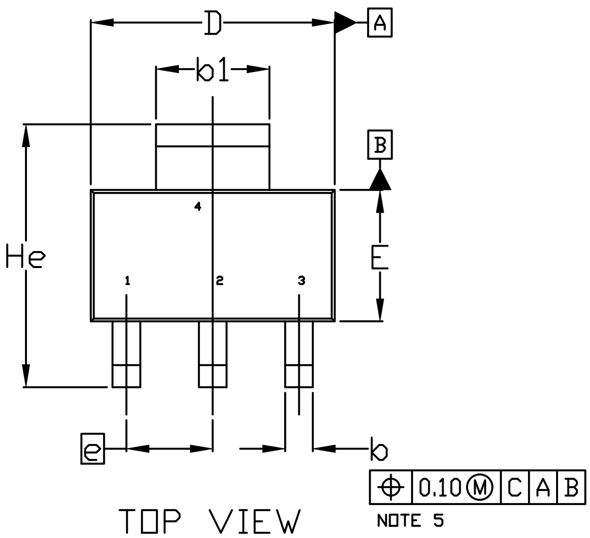
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.



**SCALE 1:1**

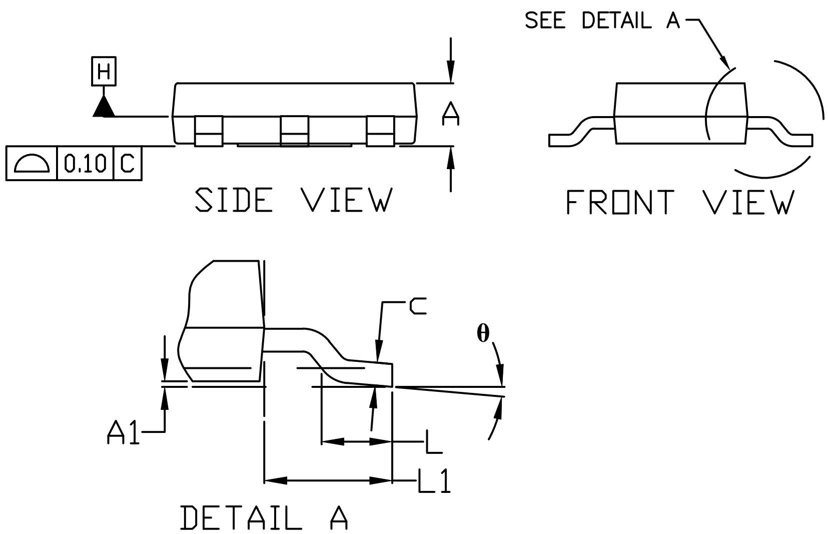
**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

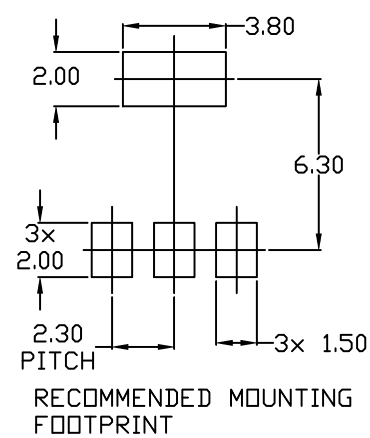
DATE 02 OCT 2018




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |




| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42680B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOT−223 (TO−261)** | **PAGE 1 OF 2** |

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

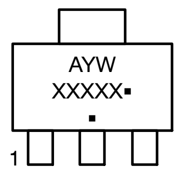
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**GENERIC**
**MARKING DIAGRAM***

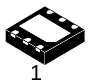



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

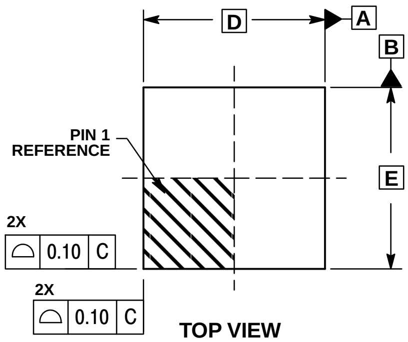
| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42680B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **SOT−223 (TO−261)** | **PAGE 2 OF 2** |



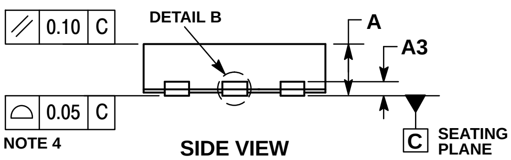

SCALE 2:1

**DFN6 3x3, 0.95P**
CASE 506DK
ISSUE O

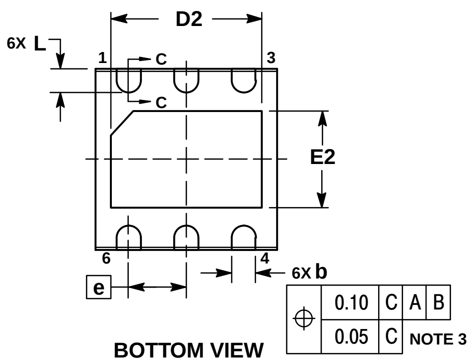
DATE 23 JUN 2016



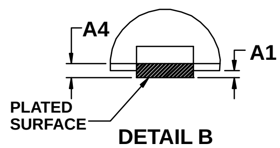

**TOP VIEW**



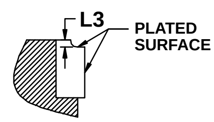

**SIDE VIEW**




**BOTTOM VIEW**




**DETAIL B**




**SECTION C−C**

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| **DIM** | **MIN** | **MAX** |
| **A** | 0.75 | 0.95 |
| **A1** | 0.00 | 0.05 |
| **A3** | 0.20 REF | |
| **A4** | 0.05 | 0.15 |
| **b** | 0.35 | 0.45 |
| **D** | 3.00 BSC | |
| **D2** | 2.40 | 2.60 |
| **E** | 3.00 BSC | |
| **E2** | 1.50 | 1.70 |
| **e** | 0.95 BSC | |
| **L** | 0.30 | 0.50 |
| **L3** | 0.00 | 0.10 |

**GENERIC MARKING DIAGRAM***

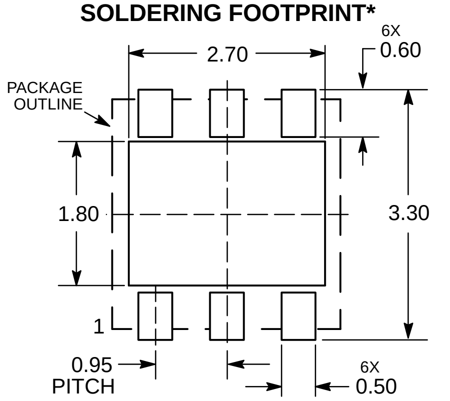
XXXXX
XXXXX
ALYW▪
▪

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

**RECOMMENDED SOLDERING FOOTPRINT***

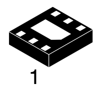



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON12549G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **STATUS:** | **ON SEMICONDUCTOR STANDARD** | |
| **NEW STANDARD:** | | |
| **DESCRIPTION:** | **DFN6 3X3, 0.95P** | **PAGE 1 OF 2** |

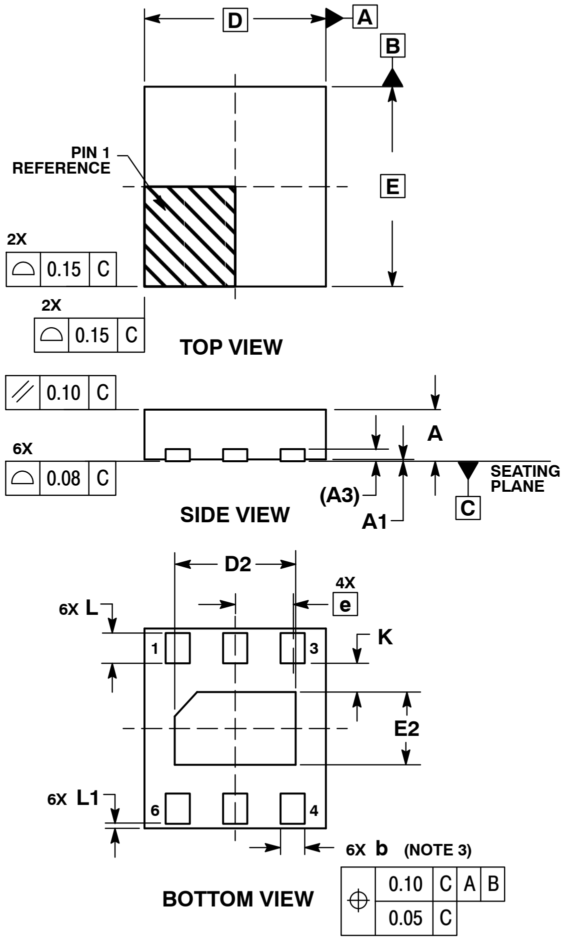
| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION. REQ. BY B. MARQUIS. | 23 JUN 2016 |




SCALE 2:1

**DFN6 3x3.3 MM, 0.95 PITCH**
CASE 506AX−01
ISSUE O

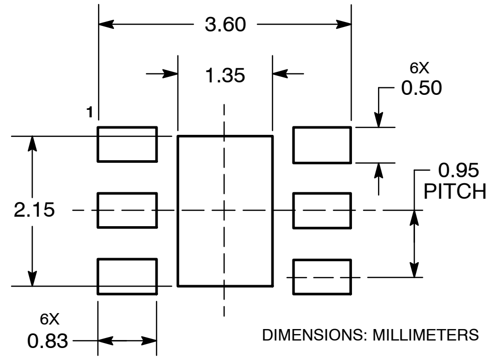
DATE 20 JAN 2006




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.80 | --- | 0.90 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.30 | --- | 0.40 |
| D | 3.00 BSC | | |
| D2 | 1.90 | --- | 2.10 |
| E | 3.30 BSC | | |
| E2 | 1.10 | --- | 1.30 |
| e | 0.95 BSC | | |
| K | 0.20 | --- | --- |
| L | 0.40 | --- | 0.60 |
| L1 | 0.00 | --- | 0.15 |

**SOLDERING FOOTPRINT***




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | | |
|---|---|---|---|
| DOCUMENT NUMBER: | 98AON21930D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| DESCRIPTION: | DFN6 3X3.3 MM, 0.95 PITCH | | PAGE 1 OF 1 |

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**ON Semiconductor Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative