NCV47821

LDO Regulator - Dual, Adjustable Current Limit, Diagnostic Features

3.3 V to 20 V

The NCV47821 dual channel LDO regulator with 200 mA per channel is designed for use in harsh automotive environments. The device has a high peak input voltage tolerance and reverse input voltage, reverse bias, overcurrent and overtemperature protections. The integrated current sense feature (adjustable by resistor connected to CSO pin for each channel) provides diagnosis and system protection functionality. The CSO pin output current creates voltage drop across CSO resistor which is proportional to output current of each channel. Extended diagnostic features in OFF state are also available and controlled by dedicated input and output pins.

Features

- Adjustable Outputs: 3.3 V to 20 V ±3% Output Voltage
- Output Current per Channel: up to 200 mA
- Two Independent Enable Inputs (3.3 V Logic Compatible)
- Adjustable Current Limits: up to 300 mA
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage and Reverse Bias Voltage
- Diagnostic Features:
  - Short To Battery (STB) and Open Load (OL) in OFF State
  - Internal Components for OFF State Diagnostics
  - Open Collector Flag Output
- AEC–Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Audio and Infotainment System
- Active Safety System

**Figure 1. Application Schematic**

(See Application Section for More Details)
Figure 2. Simplified Block Diagram

---

NCV47821

---

www.onsemi.com

2
Table 1. PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vin</td>
<td>Power Supply Input for Channel 1 and supply of control circuits of whole chip. At least 4.4 V power supply must be used for proper IC functionality.</td>
</tr>
<tr>
<td>2</td>
<td>CSO1</td>
<td>Current Sense Output 1, Current Limit setting and Output Current value information. See Application Section for more details.</td>
</tr>
<tr>
<td>3</td>
<td>EN1</td>
<td>Enable Input 1; low level disables the Channel 1. (Used also for OFF state diagnostics control for Channel 1)</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Power Supply Ground.</td>
</tr>
<tr>
<td>5</td>
<td>EN2</td>
<td>Enable Input 2; low level disables the Channel 2. (Used also for OFF state diagnostics control for Channel 2)</td>
</tr>
<tr>
<td>6</td>
<td>CSO2</td>
<td>Current Sense Output 2, Current Limit setting and Output Current value information. See Application Section for more details.</td>
</tr>
<tr>
<td>7</td>
<td>Vin</td>
<td>Power Supply Input for Channel 2. Connect to pin 1 or different power supply rail.</td>
</tr>
<tr>
<td>8</td>
<td>Vout2</td>
<td>Regulated Output Voltage 2.</td>
</tr>
<tr>
<td>9</td>
<td>ADJ2</td>
<td>Adjustable Voltage Setting Input 2. See Application Section for more details.</td>
</tr>
<tr>
<td>10</td>
<td>DE</td>
<td>Diagnostic Enable Input.</td>
</tr>
<tr>
<td>11</td>
<td>EF</td>
<td>Error Flag (Open Collector) Output. Active Low.</td>
</tr>
<tr>
<td>12</td>
<td>CS</td>
<td>Channel Select Input for OFF state diagnostics. Set CS = Low for OFF state diagnostics of Channel 1. Set CS = High for OFF state diagnostics of Channel 2. Corresponding EN pin has to be used for diagnostics control (see Application Information section for more details).</td>
</tr>
<tr>
<td>13</td>
<td>ADJ1</td>
<td>Adjustable Voltage Setting Input 1. See Application Section for more details.</td>
</tr>
<tr>
<td>14</td>
<td>Vout1</td>
<td>Regulated Output Voltage 1.</td>
</tr>
<tr>
<td>EPAD</td>
<td>EPAD</td>
<td>Exposed Pad is connected to Ground. Connect to GND plane on PCB.</td>
</tr>
</tbody>
</table>
### Table 2. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage DC</td>
<td>$V_{in}$</td>
<td>−42</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Note 1)</td>
<td>$U_{a}$</td>
<td>−</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Load Dump – Suppressed</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable Input Voltage</td>
<td>$V_{EN1,2}$</td>
<td>−42</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>ADJ Input Voltage</td>
<td>$V_{ADJ1,2}$</td>
<td>−0.3</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>CSO Voltage</td>
<td>$V_{CSO1,2}$</td>
<td>−0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>DE, CS and EF Voltages</td>
<td>$V_{DE, VCS, VEF}$</td>
<td>−0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{out1,2}$</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_{J}$</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{STG}$</td>
<td>−55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.


### Table 3. ESD CAPABILITY (Note 2)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Capability, Human Body Model</td>
<td>ESDHBM</td>
<td>−2</td>
<td>2</td>
<td>kV</td>
</tr>
</tbody>
</table>

2. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per AEC–Q100–002 (JS–001–2010)
Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50 mm2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002–2014.

### Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture Sensitivity Level</td>
<td>MSL</td>
<td>1</td>
<td>–</td>
<td></td>
</tr>
</tbody>
</table>

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

### THERMAL CHARACTERISTICS (Note 4)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Characteristics (single layer PCB)</td>
<td>$R_{JA}$</td>
<td>52</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Reference, Junction−to−Air (Note 5)</td>
<td>$R_{JA}$</td>
<td>9.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Characteristics (4 layers PCB)</td>
<td>$R_{JA}$</td>
<td>31</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Reference, Junction−to−Lead (Note 5)</td>
<td>$R_{JA}$</td>
<td>10</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

5. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate. Single layer – according to JEDEC51.3, 4 layers – according to JEDEC51.7

### Table 5. RECOMMENDED OPERATING RANGES

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (Note 6)</td>
<td>$V_{in}$</td>
<td>4.4</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Nominal Output Voltages</td>
<td>$V_{out,nom1,2}$</td>
<td>3.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Output Current Limit (Note 7)</td>
<td>$I_{LIM1,2}$</td>
<td>10</td>
<td>300</td>
<td>mA</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_{J}$</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Current Sense Output (CSO) Capacitor</td>
<td>$C_{CSO1,2}$</td>
<td>1</td>
<td>4.7</td>
<td>µF</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum $V_{in} = 4.4$ V or $(V_{out1,2} + 0.5$ V), whichever is higher.

7. Corresponding $R_{CSO1,2}$ is in range from 25.5 kΩ down to 850 Ω.
Table 6. ELECTRICAL CHARACTERISTICS  

\( V_{in} = 13.5 \text{ V}, V_{EN1,2} = 3.3 \text{ V}, V_{DE} = 0 \text{ V}, R_{CSO1,2} = 0 \text{ }\Omega, C_{CSO1,2} = 1 \mu\text{F}, C_{in} = 1 \mu\text{F}, C_{out1,2} = 10 \mu\text{F} \). Min and Max values are valid for temperature range \(-40 \degree C \leq T_J \leq +150 \degree C\) unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to \( T_J = 25 \degree C \) (Note 8).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>REGULATOR OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage (Accuracy %) (Note 9)</td>
<td>( V_{in} = V_{in_min} \text{ to } 40 \text{ V} )</td>
<td>( V_{out1,2} )</td>
<td>-3</td>
<td>-</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td>Line Regulation (Note 9)</td>
<td>( V_{in} = V_{in_min} \text{ to } (V_{out_nom1,2} + 20 \text{ V}) )</td>
<td>( \text{Regline1,2} )</td>
<td>0.1</td>
<td>1.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>( V_{in} = (V_{out_nom1,2} + 8.5 \text{ V}) )</td>
<td>( \text{Regload1,2} )</td>
<td>0.4</td>
<td>1.4</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Dropout Voltage (Note 10)</td>
<td>( V_{out_nom1,2} = 5 \text{ V}, I_{out1,2} = 200 \text{ mA} )</td>
<td>( V_{DO1,2} )</td>
<td>-250</td>
<td>500</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td><strong>DISABLE AND QUIESCENT CURRENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Disable Current</td>
<td>( V_{EN1,2} = 0 \text{ V}, V_{out_nom1,2} = 5 \text{ V}, -40 \degree C \leq T_J \leq +125 \degree C )</td>
<td>( I_{DIS} )</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Quiescent Current, ( I_q = I_n - (I_{out1} + I_{out2}) )</td>
<td>( I_{out1} = I_{out2} = 200 \mu\text{A}, V_{in} = (V_{out_nom} + 8.5 \text{ V}) )</td>
<td>( I_q )</td>
<td>0.6</td>
<td>1.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Quiescent Current, ( I_q = I_n - (I_{out1} + I_{out2}) )</td>
<td>( I_{out1} = I_{out2} = 500 \mu\text{A}, V_{in} = (V_{out_nom} + 8.5 \text{ V}) )</td>
<td>( I_q )</td>
<td>15.5</td>
<td>25</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>CURRENT LIMIT PROTECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td>( V_{out1,2} = 0.9 \times V_{out_nom1,2}, V_{in} = (V_{out_nom1,2} + 8.5 \text{ V}) )</td>
<td>( I_{LIM1,2} )</td>
<td>300</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td><strong>PSRR &amp; NOISE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Ripple Rejection (Note 11)</td>
<td>( f = 100 \text{ Hz}, 0.5 V_{P-p1,2} )</td>
<td>( \text{PSRR}_{1,2} )</td>
<td>75</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Output Noise Voltage (Note 11)</td>
<td>( f = 10 \text{ Hz to } 100 \text{ kHz}, C_{b1,2} = 10 \text{ nF} )</td>
<td>( V_{n1,2} )</td>
<td>137</td>
<td>-</td>
<td>-</td>
<td>( \mu\text{V}_{rms} )</td>
</tr>
<tr>
<td><strong>ENABLE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable Input Threshold Voltage</td>
<td>( V_{out1,2} = 0.1 \text{ V} )</td>
<td>( V_{th(EN1,2)} )</td>
<td>0.99</td>
<td>1.8</td>
<td>2.31</td>
<td>V</td>
</tr>
<tr>
<td>Enable Input Threshold Voltage Logic Low (OFF)</td>
<td>( V_{out1,2} = 0.9 \times V_{out_nom1,2}, (V_{out_nom1,2} = 5 \text{ V}) )</td>
<td>( V_{th(EN1,2)} )</td>
<td>0.99</td>
<td>1.8</td>
<td>2.31</td>
<td>V</td>
</tr>
<tr>
<td>Enable Input Threshold Voltage Logic High (ON)</td>
<td>( V_{out1,2} = 3.3 \text{ V} )</td>
<td>( I_{EN1,2} )</td>
<td>2</td>
<td>8</td>
<td>20</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Enable Input Current</td>
<td>( V_{out1,2} = 3.3 \text{ V}, I_{out1,2} = 5 \text{ V} )</td>
<td>( I_{EN1,2} )</td>
<td>2</td>
<td>8</td>
<td>20</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Enable Input Current</td>
<td>( V_{out1,2} = 100 \text{ mA}, C_{b1,2} = 10 \text{ nF}, R_{n1} = 82 \text{ k\Omega}, R_{n2} = 27 \text{ k\Omega} )</td>
<td>( I_{on} )</td>
<td>1.7</td>
<td>-</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td><strong>OUTPUT CURRENT SENSE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSO Voltage Level at Current Limit</td>
<td>( V_{out1,2} = 0.9 \times V_{out_nom1,2}, (V_{out_nom1,2} = 5 \text{ V}) )</td>
<td>( V_{CSO_lim1,2} )</td>
<td>2.448</td>
<td>2.55</td>
<td>2.652</td>
<td>V</td>
</tr>
<tr>
<td>CSO Transient Voltage Level</td>
<td>( C_{CSO1,2} = 4.7 \mu\text{F}, R_{CSO1,2} = 1 \text{ k\Omega} )</td>
<td>( V_{CSO1,2} )</td>
<td>-</td>
<td>-</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Output Current to CSO Current Ratio (Note 11, 12)</td>
<td>( V_{CSO1,2} = 2 \text{ V}, I_{out1,2} = 1 \text{ mA to } 10 \text{ mA} (V_{out_nom1,2} = 5 \text{ V}) )</td>
<td>( I_{out1,2}/I_{CSO1,2} )</td>
<td>98</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output Current to CSO Current Ratio (Note 12)</td>
<td>( V_{CSO1,2} = 2 \text{ V}, I_{out1,2} = 10 \text{ mA to } 300 \text{ mA} (V_{out_nom1,2} = 5 \text{ V}) )</td>
<td>( I_{out1,2}/I_{CSO1,2} )</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>CSO Current at no Load Current</td>
<td>( V_{CSO1,2} = 0 \text{ V}, I_{out1,2} = 0 \text{ mA}, (V_{out_nom1,2} = 5 \text{ V}) )</td>
<td>( I_{CSO_off1,2} )</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>( \mu\text{A} )</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at \( T_A = T_J \). Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

9. Minimum input voltage \( V_{in\_min} \) is 4.4 V or \( (V_{out\_nom1,2} + 1 \text{ V}) \) whichever is higher. \( V_{out\_nom1,2} \) measured at ADJ1,2 pin due to excluding \( R_{n1} \) and \( R_{n2} \) accuracy.

10. Measured when the output voltage \( V_{out1,2} \) has dropped by 2% of \( V_{out\_nom1,2} \) from the nominal valued obtained at \( V_{in} = V_{out1,2} + 8.5 \text{ V} \).

11. Values based on design and/or characterization.

12. Not guaranteed in dropout.
Table 6. ELECTRICAL CHARACTERISTICS  \( V_{\text{in}} = 13.5 \, \text{V}, \, V_{\text{EN1,2}} = 3.3 \, \text{V}, \, V_{\text{DE}} = 0 \, \text{V}, \, R_{\text{CSO1,2}} = 0 \, \Omega, \, C_{\text{CSO1,2}} = 1 \, \mu\text{F}, \, C_{\text{in}} = 1 \, \mu\text{F}, \) \( C_{\text{out1,2}} = 10 \, \mu\text{F} \), Min and Max values are valid for temperature range \(-40^\circ \text{C} \leq T_J \leq +150^\circ \text{C} \) unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to \( T_J = 25^\circ \text{C} \) (Note 8)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DIAGNOSTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overcurrent Voltage Level Threshold</td>
<td>( V_{\text{out_nom1,2}} = 5 , \text{V}, , R_{\text{CSO1,2}} = 1 , \text{k}\Omega )</td>
<td>( V_{\text{DC1,2}} )</td>
<td>92</td>
<td>95</td>
<td>98</td>
<td>% of ( V_{\text{CSO_lim1,2}} )</td>
</tr>
<tr>
<td>Short To Battery (STB) Voltage Threshold in OFF state</td>
<td>( V_{\text{in}} = 4.4 , \text{V to 18 V}, , I_{\text{out1}} = I_{\text{out2}} = 0 , \text{mA}, , V_{\text{DE}} = 3.3 , \text{V} )</td>
<td>( V_{\text{STB1,2}} )</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>Open Load (OL) Current Threshold in OFF state</td>
<td>( V_{\text{in}} = 4.4 , \text{V to 18 V}, , V_{\text{DE}} = 3.3 , \text{V} )</td>
<td>( I_{\text{OL1,2}} )</td>
<td>5.0</td>
<td>10</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>Diagnostics Enable Threshold Voltage</td>
<td></td>
<td>( V_{\text{th(DE)}} )</td>
<td>0.99</td>
<td>1.8</td>
<td>–</td>
<td>2.31</td>
</tr>
<tr>
<td></td>
<td>Logic Low</td>
<td></td>
<td>–</td>
<td>1.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Logic High</td>
<td></td>
<td>–</td>
<td>1.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel Select Threshold Voltage</td>
<td></td>
<td>( V_{\text{th(CS)}} )</td>
<td>0.99</td>
<td>1.8</td>
<td>–</td>
<td>2.31</td>
</tr>
<tr>
<td></td>
<td>Logic Low</td>
<td></td>
<td>–</td>
<td>1.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Logic High</td>
<td></td>
<td>–</td>
<td>1.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error Flag Low Voltage</td>
<td>( I_{\text{EF}} = -1 , \text{mA} )</td>
<td>( V_{\text{EF_Low}} )</td>
<td>–</td>
<td>0.04</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td><strong>THERMAL SHUTDOWN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Temperature (Note 11)</td>
<td>( I_{\text{out1}} = I_{\text{out2}} = 5 , \text{mA}, , V_{\text{out_nom1,2}} = 5 , \text{V}, ) each channel measured separately</td>
<td>( T_{\text{SD1,2}} )</td>
<td>150</td>
<td>175</td>
<td>195</td>
<td>°C</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at \( T_A = T_J \). Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

9. Minimum input voltage \( V_{\text{in\_min}} \) is 4.4 V or \( V_{\text{out\_nom1,2}} + 1 \, \text{V} \) whichever is higher. \( V_{\text{out\_nom1,2}} \) measured at ADJ1,2 pin due to excluding \( R_{\text{n1}} \) and \( R_{\text{n2}} \) accuracy.

10. Measured when the output voltage \( V_{\text{out1,2}} \) has dropped by 2% of \( V_{\text{out\_nom1,2}} \) from the nominal valued obtained at \( V_{\text{in}} = V_{\text{out1,2}} + 8.5 \, \text{V} \).

11. Values based on design and/or characterization.

12. Not guaranteed in dropout.
NCV47821

TYPICAL CHARACTERISTICS

Figure 4. Reference Voltage vs. Temperature

Figure 5. Quiescent Current vs. Input Voltage

Figure 6. Reference Voltage vs. Input Voltage

Figure 7. Input Current vs. Input Voltage (Reverse Input Voltage)

Figure 8. Dropout Voltage vs. Output Current

Figure 9. Output Current Limit vs. Input Voltage

V_{in} = 13.5 \, \text{V}
\quad \text{I}_{out1,2} = 5 \, \text{mA}

T_{J} = 25^\circ \text{C}
\quad \text{I}_{out1,2} = 500 \, \mu\text{A}
\quad V_{out\_nom1,2} = 5 \, \text{V}

V_{in} = 13.5 \, \text{V}
\quad \text{I}_{out1,2} = 5 \, \text{mA}

T_{J} = 25^\circ \text{C}
\quad \text{I}_{out1,2} = 5 \, \text{mA}

T_{J} = 150^\circ \text{C}

T_{J} = 25^\circ \text{C}

T_{J} = -40^\circ \text{C}

V_{out\_nom1,2} = 5 \, \text{V}

T_{J} = 150^\circ \text{C}

T_{J} = 25^\circ \text{C}

T_{J} = -40^\circ \text{C}

V_{out\_nom1,2} = 5 \, \text{V}

V_{out\_nom1,2} = 3.3 \, \text{V}

T_{J} = 25^\circ \text{C}

T_{J} = -40^\circ \text{C}

T_{J} = 150^\circ \text{C}

V_{out\_nom1,2} = 3.3 \, \text{V}

V_{out\_nom1,2} = 5 \, \text{V}

V_{out\_nom1,2} = 3.3 \, \text{V}

V_{out\_nom1,2} = 5 \, \text{V}
TYPICAL CHARACTERISTICS

Figure 10. Output Current Limit vs. RCSO

Figure 11. Output Current (% of ILIM) vs. CSO Voltage

Figure 12. Quiescent Current vs. Output Current (Low Load)

Figure 13. Quiescent Current vs. Output Current (High Load)

Figure 14. Output Current to CSO Current Ratio vs. Output Current

Figure 15. Output Current to CSO Current Ratio vs. Output Current (in dropout)
TYPICAL CHARACTERISTICS

Figure 16. Output Capacitor Stability Region vs. Output Current

Figure 17. Noise vs. Frequency

Figure 18. PSRR vs. Frequency
DEFINITIONS

General
All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage
The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation
The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation
The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage
The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 2% of $V_{out\_nom}$ below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents
Quiescent Current ($I_q$) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current ($I_{DIS}$).

Current Limit
Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

PSRR
Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response
Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response
Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

Thermal Protection
Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation
The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.
Circuit Description
The NCV47821 is an integrated dual low dropout regulator that provides a regulated voltage at 200 mA to each output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability of the LDO is 200 mA per output and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator
The error amplifier compares the reference voltage to a sample of the output voltage (Vout1,2) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations
The input capacitor (Cin) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor (Cout1,2) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information. The value for the output capacitor Cout1,2, shown in Figure 1 should work for most applications; see also Figure 16 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 16 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage wavering is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Calculating Bypass Capacitor
If improved stability (reducing output voltage ringing during transients) is demanded, connect the bypass capacitor Cb1,2 between Adjustable Input pin and Vout1,2 pin according to Applications circuit at Figure 1. Parallel combination of bypass capacitor Cb1,2 with the feedback resistor Rn1 contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information. Optimal value of bypass capacitor is given by following expression

\[ C_{in} = \frac{1}{2 \times \pi \times f_z \times R_{n1}} \]  

(eq. 1)

where

- \( R_{n1} \) the upper feedback resistor
- \( f_z \) the frequency of the zero added into the device transfer function by \( R_{n1} \) and \( C_{b1} \) external components.

Set the \( R_{n1} \) resistor according to output voltage requirement. Chose the \( f_z \) with regard on the output capacitance Cout1,2, refer to the table below.

<table>
<thead>
<tr>
<th>Cout1,2 (μF)</th>
<th>10</th>
<th>22</th>
<th>47</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>fz range (kHz)</td>
<td>max 19</td>
<td>max 19</td>
<td>N/A*</td>
<td>N/A*</td>
</tr>
</tbody>
</table>

NOTE: * For Cout1,2 = 47 μF and higher, Cb1,2 capacitors are not needed for stability improvement. Cb1,2 capacitors are useful for reduction start up overshoot and noise reduction. See electrical characteristic table.

Ceramic capacitors and its part numbers listed bellow have been used as low ESR output capacitors Cout1,2 from the table above to define the frequency ranges of additional zero required for stability:

- GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206)
- GRM32ER71C226KE18 (10 μF, 16 V, X7R, 1210)
- GRM32ER61C476ME15 (47 μF, 16 V, X5R, 1210)
- GRM32ER60J107ME20 (100 μF, 6.3 V, X5R, 1210)

Enable Inputs
An enable pin is used to turn a channel on or off. By holding the pin down to a voltage less than 0.99 V, the output of the channel will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the channel will be enabled to power its output to the regulated output voltage. The enable pins may be connected directly to the input pin to give constant enable to the output channel.
Setting the Output Voltage

The output voltage range can be set between 3.3 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin ADJ. The internal reference voltage is set to a temperature stable reference (VREF1) of 1.265 V. The output voltage is calculated from the following formula. Ignoring the bias current into the ADJ pin:

\[
V_{\text{out,nom,n}} = V_{\text{REF1}} \left( 1 + \frac{R_{n1}}{R_{n2}} \right) 
\]  
(eq. 2)

Use \( R_{n2} < 50 \, \text{k} \Omega \) to avoid significant voltage output errors due to ADJ bias current.

Designers should consider the tolerance of \( R_{n1} \) and \( R_{n2} \) during the design phase.

Setting the Output Current Limit

The output current limit can be set up to 300 mA by external resistor \( R_{\text{CSO1,2}} \) (see Figure 1). Capacitor \( C_{\text{CSO}} \) of 1 \( \mu \text{F} \) in parallel with \( R_{\text{CSO}} \) is required for stability of current limit control circuitry (see Figure 1).

\[
V_{\text{CSO1,2}} = I_{\text{out,1,2}} \left( R_{\text{CSO1,2}} \times \frac{1}{100} \right) 
\]  
(eq. 3)

\[
I_{\text{LIM,1,2}} = \frac{100 \times 2.55}{R_{\text{CSO1,2}}} 
\]  
(eq. 4)

\[
R_{\text{CSO1,2}} = \frac{100 \times 2.55}{I_{\text{LIM,1,2}}} 
\]  
(eq. 5)

where

- \( R_{\text{CSO1,2}} \) - current limit setting resistor
- \( V_{\text{CSO1,2}} \) - voltage at CSO pin proportional to \( I_{\text{out,1,2}} \)
- \( I_{\text{LIM,1,2}} \) - current limit value
- \( I_{\text{out,1,2}} \) - output current actual value

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 3.

Once output current reaches its limit value (\( I_{\text{LIM,1,2}} \)) set by external resistor \( R_{\text{CSO}} \) than voltage at CSO pin is typically 2.55 V. Calculations of \( I_{\text{LIM,1,2}} \) or \( R_{\text{CSO1,2}} \) values can be done using Equation 4 and Equation 5, respectively. Minimum and maximum value of Output Current Limit can be calculated according Equation 6 and 7.

\[
I_{\text{LIM,1,2}} = \text{RATIO}_{\text{min}} \times \frac{V_{\text{CSO1,2, min}}}{R_{\text{CSO1,2, max}}} 
\]  
(eq. 6)

\[
I_{\text{LIM,1,2}} = \text{RATIO}_{\text{max}} \times \frac{V_{\text{CSO1,2, max}}}{R_{\text{CSO1,2, min}}} 
\]  
(eq. 7)

where

- \( \text{RATIO}_{\text{min}} \) - minimum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range
- \( V_{\text{CSO1,2, min}} \) - minimum value of CSO Voltage Level at Current Limit from electrical characteristics table
- \( V_{\text{CSO1,2, max}} \) - maximum value of CSO Voltage Level at Current Limit from electrical characteristics table
- \( R_{\text{CSO1,2, min}} \) - minimum value of \( R_{\text{CSO1,2}} \) with respect its accuracy
- \( R_{\text{CSO1,2, max}} \) - maximum value of \( R_{\text{CSO1,2}} \) with respect its accuracy

Designers should consider the tolerance of \( R_{\text{CSO1,2}} \) during the design phase.

Diagnostic in OFF State

The NCV47821 contains also circuitry for OFF state diagnostics for Short to Battery (STB) and Open Load (OL). There are internal current sources, Pull-Up and Pull Down resistors which provide additional cost savings for overall application by excluding external components and their assembly cost and saving PCB space and safe control IOs of a Microcontroller Unit (MCU).

Simplified functional schematic and truth table is shown in Figure 19 and related flowchart in Figure 20.
The diagnostics in OFF state shall be performed for each channel separately. For diagnostics of Channel 1 the input CS pin has to be put logic low, for diagnostics of Channel 2 the input CS pin has to be put logic high. Corresponding EN pin has to be used for control (EN1 for Channel 1 and EN2 for Channel 2). For detailed information see Diagnostic Features Truth Table in Figure 21.

**Diagnostic in ON State**

Diagnostic in ON State provides information about Overcurrent or Short to Ground failures, during which the EF output is in logic low state. The diagnostics in ON state shall be performed for each channel separately. For diagnostics of Channel 1 the input CS pin has to be put logic low, for diagnostics of Channel 2 the input CS pin has to be put logic high. For detailed information see Diagnostic Features Truth Table in Figure 21.

**Figure 20. Flowchart for Diagnostics in OFF State**

**Figure 21. Diagnostic Features Truth Table**

<table>
<thead>
<tr>
<th>Operational Status</th>
<th>EN</th>
<th>DE</th>
<th>CS</th>
<th>Output Voltage (V_{out1}, V_{out2})</th>
<th>Diagnostic Output (CS01, CS02)</th>
<th>Error Flag (EF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Low (~0 V)</td>
<td>Low (~0 V)</td>
<td>HZ</td>
</tr>
<tr>
<td>Short to Battery</td>
<td>L</td>
<td>H</td>
<td>L/H</td>
<td>High (V_{out} ~ V_{in})</td>
<td>Low (~0 V)</td>
<td>L 13</td>
</tr>
<tr>
<td>Open Load (OFF)</td>
<td>H</td>
<td>H</td>
<td>L/H</td>
<td>High (V_{out} ~ V_{in})</td>
<td>Low (~0 V)</td>
<td>L 15</td>
</tr>
<tr>
<td>Normal (OFF)</td>
<td>H</td>
<td>H</td>
<td>L/H</td>
<td>Low (~0 V)</td>
<td>Low (~0 V)</td>
<td>HZ 15</td>
</tr>
<tr>
<td>Open Load (ON)</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>V_{out,nom}</td>
<td>Low (~0 V)</td>
<td>HZ</td>
</tr>
<tr>
<td>Normal (ON)</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>V_{out,nom}</td>
<td>Proportional to I_{out} (±10 %)</td>
<td>HZ</td>
</tr>
<tr>
<td>Over Current</td>
<td>H</td>
<td>L</td>
<td>L/H</td>
<td>≤ 90 % of V_{out,nom}</td>
<td>High (~2.55 V)</td>
<td>L</td>
</tr>
<tr>
<td>Short to Ground</td>
<td>H</td>
<td>L</td>
<td>L/H</td>
<td>Low (~0 V)</td>
<td>High (~2.55 V)</td>
<td>L</td>
</tr>
</tbody>
</table>

13. State of EN pin of appropriate channel
14. CS = L means CH1 diagnostics and CS = H means CH2 diagnostics in OFF state (DE = H) via EF output, appropriate EN pin is used for turning internal switch ON and OFF (e.g. when DE = H and CS = L and EN1 = L then IPU1 is OFF, when DE = H and CS = L and EN1 = H then IPU1 is ON)
15. Internal current source turned OFF (between V_{out} and V_{in} of appropriate channel)
16. Internal current source turned ON (between V_{out} and V_{in} of appropriate channel)
17. CS = L means CH1 diagnostics and CS = H means CH2 diagnostics in ON state (e.g. when CS = L and EF = L then CH1 has Overcurrent or Short to Ground failure, when CS = H and EF = L then CH1 has Overcurrent or Short to Ground failure)
Thermal Considerations

As power in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the device can handle is given by:

\[ P_{D(MAX)} = \frac{[T_J(MAX) - T_A]}{R_{JUA}} \]  
(eq. 8)

Since \( T_J \) is not recommended to exceed 150°C, then the device soldered on 645 mm\(^2\), 1 oz copper area, FR4 can dissipate up to 2.38 W when the ambient temperature (\( T_A \)) is 25°C. See Figure 22 for \( R_{JUA} \) versus PCB area. The power dissipated by the device can be calculated from the following equations:

\[ P_D = V_{in}(I_q@I_{out1,2}) + I_{out1}(V_{in} - V_{out1}) + I_{out2}(V_{in} - V_{out2}) \]  
(eq. 9)

or

\[ V_{in(MAX)} = \frac{P_{D(MAX)} + (V_{out1} \times I_{out1}) + (V_{out2} \times I_{out2})}{I_{out1} + I_{out2} + I_q} \]  
(eq. 10)

**Figure 22. Thermal Resistance vs. PCB Copper Area**

Hints

\( V_{in} \) and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Output Voltage</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCV47821PAAJR2G</td>
<td>Adjustable</td>
<td>Line1: NCV4</td>
<td>TSSOP–14 Exposed Pad</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Line2: 7821</td>
<td>(Pb–Free)</td>
<td></td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D
NCV47821

PACKAGE DIMENSIONS

TSSOP–14 EP
CASE 948AW
ISSUE C

NOTE 8: 303
NOTE 7: 303
NOTE 6: 303
NOTE 5: 303
NOTE 4: 303
NOTE 3: 303
NOTE 2: 303
NOTE 1: 303

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSIONS. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADI- US OF THE FOOT. MINIMUM SPACE BETWEEN PRO- TRUSIONS AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B–B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application or use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19502 E. 32nd Pl., Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5817–1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

0 NCV47821/D