NCV4274, NCV4274A

Regulator Family, 400 mA, 2% and 4% Voltage

Description
The NCV4274 and NCV4274A is a precision micro–power voltage regulator with an output current capability of 400 mA available in the DPAK, D2PAK and SOT–223 packages.

The output voltage is accurate within ±2.0% or ±4.0% depending on the version with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 150 μA with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

Features
- 2.5, 3.3 V, 5.0 V, 8.5 V, ±2.0% Output Options
- 2.5, 3.3 V, 5.0 V, ±4.0% Output Options
- Low 150 μA Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Very Low Dropout Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These are Pb–Free Devices

MARKING DIAGRAMS

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.
NCV4274, NCV4274A

Figure 1. Block Diagram

Pin Definitions and Functions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I</td>
<td>Input; Bypass directly at the IC a ceramic capacitor to GND.</td>
</tr>
<tr>
<td>2, 4</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>Q</td>
<td>Output; Bypass with a capacitor to GND.</td>
</tr>
</tbody>
</table>

1. DPAK 3LD package code 6025
2. D2PAK 3LD package code 6083

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Pin Symbol, Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I, Input to Regulator Voltage</td>
<td>V_I</td>
<td>−42</td>
<td>45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>I_I</td>
<td>Internally Limited</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_I</td>
<td></td>
<td>Internally Limited</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I, Input peak Transient Voltage to Regulator with Respect to GND</td>
<td>V_I</td>
<td>60</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q, Regulated Output Voltage</td>
<td>V_Q</td>
<td>−1.0</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>I_Q</td>
<td>Internally Limited</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND, Ground Current</td>
<td>I_GND</td>
<td>−</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>T_J</td>
<td>−50</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T_Sig</td>
<td>−50</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>ESD Capability, Human Body Model</td>
<td>ESD_HB</td>
<td>4</td>
<td></td>
<td>kV</td>
<td></td>
</tr>
<tr>
<td>ESD Capability, Machine Model</td>
<td>ESD_MM</td>
<td>200</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>ESD Capability, Charged Device Model</td>
<td>ESD_CDM</td>
<td>1</td>
<td></td>
<td>kV</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. This device series incorporates ESD protection and is tested by the following methods:
   - ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A114)
   - ESD MM tested per AEC-Q100-003 (EIA/JESD22-A115)
   - ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model
### OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (8.5 V Version)</td>
<td>$V_I$</td>
<td></td>
<td>9.0</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (5.0 V Version)</td>
<td>$V_I$</td>
<td></td>
<td>5.5</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (3.3 V, and 2.5 V Version)</td>
<td>$V_I$</td>
<td></td>
<td>4.5</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_J$</td>
<td></td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### THERMAL RESISTANCE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction–to–Ambient</td>
<td>DPAK</td>
<td>$R_{thja}$</td>
<td>–</td>
<td>70 (Note 4)</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Ambient</td>
<td>D2PAK</td>
<td>$R_{thja}$</td>
<td>–</td>
<td>60 (Note 4)</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Case</td>
<td>DPAK</td>
<td>$R_{thjc}$</td>
<td>–</td>
<td>4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Case</td>
<td>D2PAK</td>
<td>$R_{thjc}$</td>
<td>–</td>
<td>3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Tab</td>
<td>SOT–223 $\Psi_{−JLX}$, $\Psi_{LX}$</td>
<td></td>
<td>–</td>
<td>14.5 (Note 5)</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Ambient</td>
<td>SOT–223</td>
<td>$R_{thua, \theta JA}$</td>
<td>–</td>
<td>169.7 (Note 5)</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

4. Soldered in, minimal footprint, FR4
5. 1 oz copper, 5 mm² copper area, FR4

### LEAD FREE SOLDERING TEMPERATURE AND MSL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead Free Soldering, (Note 6) Reflow (SMD styles only), Pb–Free</td>
<td>$T_{slid}$</td>
<td>60s – 150s Above 217s 40s Max at Peak</td>
<td>–</td>
<td>265 pk</td>
<td>°C</td>
</tr>
<tr>
<td>Moisture Sensitivity Level</td>
<td>MSL</td>
<td>DPAK and D2PAK SOT–223</td>
<td>1</td>
<td>3</td>
<td>–</td>
</tr>
</tbody>
</table>

6. Per IPC/JEDEC J–STD–020C


## ELECTRICAL CHARACTERISTICS

$-40^\circ\text{C} < T_J < 150^\circ\text{C};\ V_I = 13.5\ \text{V}$ unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>NCV4274A</th>
<th>NCV4274</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>REGULATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage (8.5 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 200\ mA$</td>
<td>8.33</td>
<td>8.5</td>
<td>8.67</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Output Voltage (8.5 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 400\ mA$</td>
<td>8.33</td>
<td>8.5</td>
<td>8.67</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Output Voltage (5.0 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 200\ mA$</td>
<td>4.9</td>
<td>5.0</td>
<td>5.1</td>
<td>4.8</td>
<td>5.0</td>
</tr>
<tr>
<td>Output Voltage (5.0 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 200\ mA$</td>
<td>4.9</td>
<td>5.0</td>
<td>5.1</td>
<td>4.8</td>
<td>5.0</td>
</tr>
<tr>
<td>Output Voltage (3.3 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 400\ mA$</td>
<td>3.23</td>
<td>3.3</td>
<td>3.37</td>
<td>3.17</td>
<td>3.3</td>
</tr>
<tr>
<td>Output Voltage (3.3 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 400\ mA$</td>
<td>3.23</td>
<td>3.3</td>
<td>3.37</td>
<td>3.17</td>
<td>3.3</td>
</tr>
<tr>
<td>Output Voltage (2.5 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 400\ mA$</td>
<td>2.45</td>
<td>2.5</td>
<td>2.55</td>
<td>2.4</td>
<td>2.5</td>
</tr>
<tr>
<td>Output Voltage (2.5 V Version)</td>
<td>$V_Q$</td>
<td>$5\ mA &lt; I_Q &lt; 200\ mA$</td>
<td>2.45</td>
<td>2.5</td>
<td>2.55</td>
<td>2.4</td>
<td>2.5</td>
</tr>
<tr>
<td>Current Limit</td>
<td>$I_Q$</td>
<td>−</td>
<td>400</td>
<td>600</td>
<td>−</td>
<td>400</td>
<td>600</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_Q$</td>
<td>$1\ mA$</td>
<td>−</td>
<td>195</td>
<td>250</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$I_Q = 1\ mA$</td>
<td>−</td>
<td>190</td>
<td>250</td>
<td>−</td>
<td>190</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 8.5\ V$</td>
<td>−</td>
<td>145</td>
<td>250</td>
<td>−</td>
<td>145</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 5.0\ V$</td>
<td>−</td>
<td>140</td>
<td>250</td>
<td>−</td>
<td>140</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 2.5\ V$</td>
<td>−</td>
<td>10</td>
<td>15</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$I_Q = 250\ mA$</td>
<td>−</td>
<td>10</td>
<td>15</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 8.5\ V$</td>
<td>−</td>
<td>13</td>
<td>20</td>
<td>−</td>
<td>13</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 5.0\ V$</td>
<td>−</td>
<td>12</td>
<td>20</td>
<td>−</td>
<td>12</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 2.5\ V$</td>
<td>−</td>
<td>20</td>
<td>35</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$I_Q = 400\ mA$</td>
<td>−</td>
<td>20</td>
<td>35</td>
<td>−</td>
<td>20</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 8.5\ V$</td>
<td>−</td>
<td>30</td>
<td>45</td>
<td>−</td>
<td>30</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 5.0\ V$</td>
<td>−</td>
<td>28</td>
<td>45</td>
<td>−</td>
<td>28</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_Q$</td>
<td>$V_Q = 2.5\ V$</td>
<td>−</td>
<td>28</td>
<td>45</td>
<td>−</td>
<td>28</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$AV_Q$</td>
<td>$I_Q = 5\ mA$</td>
<td>−</td>
<td>7</td>
<td>20</td>
<td>−</td>
<td>7</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$AV_Q$</td>
<td>$I_Q = 12\ mA$</td>
<td>−</td>
<td>10</td>
<td>25</td>
<td>−</td>
<td>10</td>
</tr>
<tr>
<td>Power Supply Ripple Rejection</td>
<td>$PSRR$</td>
<td>$I_Q = 5\ mA$</td>
<td>−</td>
<td>60</td>
<td>−</td>
<td>−</td>
<td>60</td>
</tr>
<tr>
<td>Temperature output voltage drift</td>
<td>$AV_Q/\Delta T$</td>
<td>$fr = 100\ Hz$</td>
<td>−</td>
<td>0.5</td>
<td>−</td>
<td>−</td>
<td>0.5</td>
</tr>
<tr>
<td>Thermal Shutdown Temperature*</td>
<td>$T_{SD}$</td>
<td>$I_Q = 5\ mA$</td>
<td>165</td>
<td>−</td>
<td>210</td>
<td>165</td>
<td>−</td>
</tr>
</tbody>
</table>

*Guaranteed by design, not tested in production.
NCV4274, NCV4274A

Figure 2. Measuring Circuit

Figure 3. Application Circuit

TYPICAL CHARACTERISTIC CURVES

Figure 4. ESR Characterization – 3.3 V, 5 V and 8.5 V Versions

Figure 5. ESR Characterization – 2.5 V Version
NCV4274, NCV4274A

TYPICAL CHARACTERISTIC CURVES – 8.5 V Version

Figure 6. Output Voltage vs. Junction Temperature

Figure 7. Output Voltage vs. Input Voltage

Figure 8. Output Current vs. Input Voltage

Figure 9. Current Consumption vs. Output Current (High Load)

Figure 10. Current Consumption vs. Output Current (Low Load)

Figure 11. Drop Voltage vs. Output Current
NCV4274, NCV4274A

TYPICAL CHARACTERISTIC CURVES – 8.5 V Version

Figure 12. Current Consumption vs. Input Voltage

Figure 13. Input Current vs. Input Voltage
NCV4274, NCV4274A

TYPICAL CHARACTERISTIC CURVES – 5.0 V Version

Figure 14. Output Voltage vs. Junction Temperature

Figure 15. Output Voltage vs. Input Voltage

Figure 16. Output Current vs. Input Voltage

Figure 17. Current Consumption vs. Output Current (High Load)

Figure 18. Current Consumption vs. Output Current (Low Load)

Figure 19. Drop Voltage vs. Output Current
TYPICAL CHARACTERISTIC CURVES – 5.0 V Version

Figure 20. Current Consumption vs. Input Voltage

Figure 21. Input Current vs. Input Voltage
TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

- Figure 22. Output Voltage vs. Junction Temperature
  - $V_i = 6 \text{ V}$
  - $R_L = 1 \text{ k}\Omega$

- Figure 23. Output Voltage vs. Input Voltage
  - $V_i = 13.5 \text{ V}$

- Figure 24. Output Current vs. Input Voltage
  - $T_J = 25^\circ \text{C}$
  - $V_O = 0 \text{ V}$

- Figure 25. Current Consumption vs. Output Current (High Load)
  - $T_J = 25^\circ \text{C}$
  - $V_i = 13.5 \text{ V}$

- Figure 26. Current Consumption vs. Output Current (Low Load)
  - $T_J = 25^\circ \text{C}$
  - $V_i = 13.5 \text{ V}$

- Figure 27. Voltage Drop vs. Output Current
  - $T_J = 25^\circ \text{C}$
  - $T_J = 125^\circ \text{C}$

VDR = $V_i(\min) - V_O$
TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

Figure 28. Current Consumption vs. Input Voltage

Figure 29. Input Current vs. Input Voltage
NCV4274, NCV4274A

TYPICAL CHARACTERISTIC CURVES – 2.5 V Version

Figure 30. Output Voltage vs. Junction Temperature

Figure 31. Output Voltage vs. Input Voltage

Figure 32. Output Current vs. Input Voltage

Figure 33. Current Consumption vs. Output Current (High Load)

Figure 34. Current Consumption vs. Output Current (Low Load)

Figure 35. Voltage Drop vs. Output Current
Figure 36. Current Consumption vs. Input Voltage

Figure 37. Input Current vs. Input Voltage
Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Stability Considerations

The input capacitor $C_{I1}$ in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with $C_{I2}$.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ($−25°C$ to $−40°C$), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information.

The value for the output capacitor $C_Q$ shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_Q \geq 2.2 \mu F$ and an ESR $\leq 2.5 \Omega$ within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = (V_{I(max)} - V_{Q(min)})I_{Q(max)} + V_{I(max)}I_q \text{ (eq. 1)}$$

Where:

- $V_{I(max)}$ is the maximum input voltage,
- $V_{Q(min)}$ is the minimum output voltage,
- $I_{Q(max)}$ is the maximum output current for the application, and
- $I_q$ is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{JA}$ can be calculated:

$$P_{D(max)} = \frac{150°C - T_A}{R_{JA}} \text{ (eq. 2)}$$

The value of $R_{JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{JA}$’s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{JA}$:

$$R_{JA} = R_{JC} + R_{CS} + R_{SA} \text{ (eq. 3)}$$

Where:

- $R_{JC}$ = the junction–to–case thermal resistance,
- $R_{CS}$ = the case–to–heat sink thermal resistance, and
- $R_{SA}$ = the heat sink–to–ambient thermal resistance.

$R_{JC}$ appears in the package section of the data sheet. Like $R_{JA}$, it too is a function of package type. $R_{CS}$ and $R_{SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.
<table>
<thead>
<tr>
<th>Device*</th>
<th>Output Voltage Accuracy</th>
<th>Output Voltage</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCV4274ADS85R4G</td>
<td>2%</td>
<td>8.5 V</td>
<td>D2PAK (Pb–Free)</td>
<td>800 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV4274DS50G</td>
<td>4%</td>
<td>5.0 V</td>
<td>D2PAK (Pb–Free)</td>
<td>50 Units / Rail</td>
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<tr>
<td>NCV4274DS50R4G</td>
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<td>D2PAK (Pb–Free)</td>
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<tr>
<td>NCV4274DT50RKG</td>
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<tr>
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<tr>
<td>NCV4274ST33T3G</td>
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<td>3.3 V</td>
<td>SOT–223 (Pb–Free)</td>
<td>4000 / Tape &amp; Reel</td>
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<td>NCV4274DT33RKG</td>
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<td>DPAK (Pb–Free)</td>
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<td>SOT–223 (Pb–Free)</td>
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<td>3.3 V</td>
<td>DPAK (Pb–Free)</td>
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<tr>
<td>NCV4274ADS33R4G</td>
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<td>3.3 V</td>
<td>D2PAK (Pb–Free)</td>
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<tr>
<td>NCV4274ST25T3G</td>
<td>4%</td>
<td>2.5 V</td>
<td>SOT–223 (Pb–Free)</td>
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<td>2.5 V</td>
<td>SOT–223 (Pb–Free)</td>
<td>4000 / Tape &amp; Reel</td>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

NOTES:
2. CONTROLLING DIMENSION MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

<table>
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<tr>
<th>MILLIMETERS</th>
<th>DIM</th>
<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
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<td>A</td>
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<td>1.63</td>
<td>1.75</td>
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<tr>
<td>A1</td>
<td>0.02</td>
<td>0.06</td>
<td>0.10</td>
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<tr>
<td>b</td>
<td>0.60</td>
<td>0.75</td>
<td>0.89</td>
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<tr>
<td>b1</td>
<td>2.90</td>
<td>3.06</td>
<td>3.20</td>
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<td>c</td>
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<td>0.29</td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td>D</td>
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<td>6.50</td>
<td>6.70</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>3.30</td>
<td>3.50</td>
<td>3.70</td>
<td></td>
</tr>
<tr>
<td>e</td>
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<td></td>
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</tr>
<tr>
<td>L1</td>
<td>1.50</td>
<td>1.75</td>
<td>2.00</td>
<td></td>
</tr>
<tr>
<td>He</td>
<td>6.70</td>
<td>7.00</td>
<td>7.30</td>
<td></td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>---</td>
<td>10°</td>
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RECOMMENDED MOUNTING FOOTPRINT

SCALE 1:1

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SOT–223 (TO–261)
CASE 318E–04
ISSUE R

DATE 02 OCT 2018

**STYLE 1:**
- PIN 1. BASE
- PIN 2. COLLECTOR
- PIN 3. EMITTER
- PIN 4. COLLECTOR

**STYLE 2:**
- PIN 1. ANODE
- PIN 2. CATHODE
- PIN 3. NC
- PIN 4. CATHODE

**STYLE 3:**
- PIN 1. GATE
- PIN 2. DRAIN
- PIN 3. SOURCE
- PIN 4. DRAIN

**STYLE 4:**
- PIN 1. SOURCE
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. SOURCE

**STYLE 5:**
- PIN 1. DRAIN
- PIN 2. GATE
- PIN 3. SOURCE
- PIN 4. DRAIN

**STYLE 6:**
- PIN 1. RETURN
- PIN 2. INPUT
- PIN 3. OUTPUT
- PIN 4. INPUT

**STYLE 7:**
- PIN 1. ANODE 1
- PIN 2. CATHODE
- PIN 3. ANODE 2
- PIN 4. CATHODE

**STYLE 8:** CANCELLED

**STYLE 9:**
- PIN 1. INPUT
- PIN 2. GROUND
- PIN 3. LOGIC
- PIN 4. GROUND

**STYLE 10:**
- PIN 1. CATHODE
- PIN 2. ANODE
- PIN 3. GATE
- PIN 4. ANODE

**STYLE 11:**
- PIN 1. MT 1
- PIN 2. MT 2
- PIN 3. GATE
- PIN 4. MT 2

**STYLE 12:**
- PIN 1. INPUT
- PIN 2. OUTPUT
- PIN 3. NC
- PIN 4. OUTPUT

**STYLE 13:**
- PIN 1. GATE
- PIN 2. COLLECTOR
- PIN 3. EMITTER
- PIN 4. COLLECTOR

**GENERIC MARKING DIAGRAM***

\[
\begin{array}{c}
\text{AYW} \\
\text{XXXXX} \\
\cdot
\end{array}
\]

1

A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
● = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “●”, may or may not be present. Some products may not follow the Generic Marking.

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DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS L3, L4 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

GENERAL MARKING DIAGRAM*

SOLDERING FOOTPRINT*

*This information is generic. Please refer to device data sheet for actual part marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
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<th>REVISION</th>
<th>DATE</th>
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<tr>
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<td>RELEASED FOR PRODUCTION. REQ. BY L. GAN</td>
<td>24 SEP 2001</td>
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<tr>
<td>A</td>
<td>ADDED STYLE 8. REQ. BY S. ALLEN.</td>
<td>06 AUG 2008</td>
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<tr>
<td>B</td>
<td>ADDED STYLE 9. REQ. BY D. WARNER.</td>
<td>16 JAN 2009</td>
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<tr>
<td>C</td>
<td>ADDED STYLE 10. REQ. BY S. ALLEN.</td>
<td>09 JUN 2009</td>
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<td>D</td>
<td>RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.</td>
<td>29 JUN 2010</td>
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<td>ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMPALIZZA.</td>
<td>06 FEB 2014</td>
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<tr>
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<td>ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.</td>
<td>21 JUL 2015</td>
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NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

SOLDERING FOOTPRINT*  

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM**

XX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G”, may or may not be present.