NCV1060, NCV1063

Automotive High-Voltage Switcher for Low Power Offline SMPS

The NCV106X products integrate a fixed frequency current mode controller with a 670 V MOSFET. Available in a SOIC−10 or SOIC−16 package, the NCV106X offer a high level of integration, including soft−start, frequency−jittering, short−circuit protection, skip−cycle, adjustable peak current set point, ramp compensation, and a Dynamic Self−Supply (eliminating the need for an auxiliary winding).

Unlike other monolithic solutions, the NCV106X is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (60 kHz or 100 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to a no load condition.

Protection features include: a timer to detect an overload or a short−circuit event, Overvoltage Protection with auto−recovery and AC input line voltage detection (A version).

The ON proprietary integrated Over Power Protection (OPP) lets you harness the maximum delivered power without affecting your standby performance simply via external resistors.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to reduce input power consumption below 50 mW at high line.

NCV106x can be seamlessly used both in non−isolated and in isolated topologies.

Features

• Built−in 670 V MOSFET with RDS(on) of 34 Ω (NCV1060) and 11.4 Ω (NCV1063)
• Large Creepage Distance Between High−voltage Pins
• Current−Mode Fixed Frequency Operation – 60 kHz or 100 kHz
• Adjustable Peak Current: see below table
• Fixed Ramp Compensation
• Direct Feedback Connection for Non−isolated Converter
• Internal and Adjustable Over Power Protection (OPP) Circuit
• Skip−Cycle Operation at Low Peak Currents Only
• Dynamic Self−Supply: No Need for an Auxiliary Winding
• Internal 4 ms Soft−Start
• Auto−Recovery Output Short Circuit Protection with Timer−Based Detection
• Auto−Recovery Overvoltage Protection with Auxiliary Winding Operation
• Frequency Jittering for Better EMI Signature
• No Load Input Consumption < 50 mW

Typical Applications

• Auxiliary & Standby Isolated Power Supplies for HEV/EV
## Table 1. PRODUCT INFORMATION & INDICATIVE MAXIMUM OUTPUT POWER

<table>
<thead>
<tr>
<th>Product</th>
<th>( R_{\text{DS(on)}} )</th>
<th>( I_{\text{PK}(0)} )</th>
<th>230 Vac ± 15%</th>
<th>85 – 265 Vac</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Adapter</td>
<td>Open Frame</td>
</tr>
<tr>
<td>NCV1060 60 kHz</td>
<td>34 ( \Omega )</td>
<td>300 mA</td>
<td>2.9 W</td>
<td>7.2 W</td>
</tr>
<tr>
<td>NCV1063 100 kHz</td>
<td>11.4 ( \Omega )</td>
<td>780 mA</td>
<td>6.9 W</td>
<td>17.1 W</td>
</tr>
</tbody>
</table>

**NOTE:** Informative values only, with \( T_{\text{amb}} = 25^\circ \text{C} \), \( T_{\text{case}} = 100^\circ \text{C} \), SOIC–10 package for NCV1060 and SOIC–16 package for NCV1063, Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

![Figure 1. Pin Connections](image)

## Table 2. PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Pin Name</th>
<th>Function</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOIC 10</td>
<td>SOIC 16</td>
<td>SOIC 16</td>
<td>SOIC 10</td>
</tr>
<tr>
<td>1</td>
<td>1–4</td>
<td>GND</td>
<td>The IC Ground</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>VCC</td>
<td>Powers the Internal Circuitry</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This pin is connected to an external capacitor. The ( V_{\text{DD}} ) includes an auto–recovery over voltage protection</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>LIM/OPP</td>
<td>Ipeak Set / Over Power Limitation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The current drawn from the pin decreases ( I_{\text{peak}} ) of the primary winding. If resistive divider from the auxiliary winding is connected to this pin it sets the OPP compensation level (it diminishes the peak current.)</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>FB</td>
<td>Feedback Signal Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This is the inverting input of the trans conductance error amplifier. It is normally connected to the switching power supply output through a resistor divider</td>
</tr>
<tr>
<td>5</td>
<td>8</td>
<td>Comp</td>
<td>Compensation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth. Also, by connecting an opto–coupler to this pin, the peak current set point is adjusted accordingly to the output power demand</td>
</tr>
<tr>
<td>9–12</td>
<td></td>
<td></td>
<td>This un–connected pin ensures adequate creepage distance</td>
</tr>
<tr>
<td>6–10</td>
<td>13–16</td>
<td>Drain</td>
<td>Drain Connection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The internal drain MOSFET connection</td>
</tr>
</tbody>
</table>
### Table 3. TYPICAL APPLICATIONS

<table>
<thead>
<tr>
<th>Circuit Diagram</th>
<th>Description</th>
</tr>
</thead>
</table>
| ![Diagram](image1) | • If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and $V_{OVP}$ level) $V_{CC}$ is supplied from output via D2  
• If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS  
• $R_2$ limits maximum output power (can be omitted if not required)  
• Direct feedback, resistive divider formed by $R_3$, $R_4$ sets output voltage |
| ![Diagram](image2) | • If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and $V_{OVP}$ level) $V_{CC}$ is supplied from output via D3  
• If the output voltage is below 9.0 V, $D_3$ and $C_5$ are redundant, the IC is supplied from DSS  
• $R_2$ limits maximum output power (can be omitted if not required)  
• Optocoupler feedback |
| ![Diagram](image3) | • If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and $V_{OVP}$ level) $V_{CC}$ is supplied from output via $D_2$  
• $R_2$ limits maximal output power  
• Direct feedback, resistive divider formed by $R_3$, $R_4$ sets output voltage |
| ![Diagram](image4) | • $V_{CC}$ supplied from DSS  
• Output voltage is below 9.0 V typ.  
• LIM/OPP pin floating – no limit output power  
• Direct feedback, resistive divider formed by $R_2$, $R_3$ sets output voltage |

**Typical Non–isolated Application – Buck Converter**

**Typical Non–isolated Application – Buck–Boost Converter**
### Table 3. TYPICAL APPLICATIONS (continued)

**Typical Non-isolated Application – Flyback Converter**

- VCC supplied from auxiliary winding
- Resistive divider formed by R2, R3 sets output power limit and over power protection
- Optocoupler feedback, resistive divider formed by R6, R7 sets output voltage

**Typical Isolated Application – Flyback Converter**

- VCC supplied from DSS
- Output voltage is below 9.0 V typ.
- LIM/OPP pin floating – no limit output power
- Resistive divider formed by R2, R3 sets output voltage

- If the output voltage is above 9.0 V typ. between $V_{CC(ON)}$ level and $V_{DVP}$ level – VCC supplied from output via D4
- LIM/OPP pin floating – no limit output power
- Resistive divider formed by R2, R3 sets output voltage
Figure 2. Simplified Internal Circuit Architecture
Table 4. MAXIMUM RATING TABLE (All voltages related to GND terminal)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage, $V_{CC}$ pin, continuous voltage</td>
<td>$V_{CC}$</td>
<td>$-0.3$ to $20$</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on all pins, except Drain and $V_{CC}$ pin</td>
<td>$V_{inmax}$</td>
<td>$-0.3$ to $10$</td>
<td>V</td>
</tr>
<tr>
<td>Drain voltage</td>
<td>$BVDss$</td>
<td>$-0.3$ to $670$</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Current into $V_{CC}$ pin</td>
<td>$I_{CC}$</td>
<td>$10$</td>
<td>mA</td>
</tr>
<tr>
<td>Drain Current Peak during Transformer Saturation ($T_J = 150 \degree C$, Note 2):</td>
<td>$I_{DS(pk)}$</td>
<td>$300$</td>
<td>mA</td>
</tr>
<tr>
<td>NCV1060</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCV1063</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Current Peak during Transformer Saturation ($T_J = 125 \degree C$, Note 2):</td>
<td>$I_{DS(pk)}$</td>
<td>$335$</td>
<td>mA</td>
</tr>
<tr>
<td>NCV1060</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCV1063</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Current Peak during Transformer Saturation ($T_J = 25 \degree C$, Note 2):</td>
<td>$I_{DS(pk)}$</td>
<td>$520$</td>
<td>mA</td>
</tr>
<tr>
<td>NCV1060</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCV1063</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance Junction--to--Air -- SOIC10 with 200 mm$^2$ of 35-$\mu$ copper area</td>
<td>$R_{\theta JA}$</td>
<td>$132$</td>
<td>$\degree$C/W</td>
</tr>
<tr>
<td>Thermal Resistance Junction--to--Air -- SOIC16 with 200 mm$^2$ of 35-$\mu$ copper area</td>
<td>$R_{\theta JA}$</td>
<td>$104$</td>
<td>$\degree$C/W</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td>$T_J$</td>
<td>$-40$ to $+150$</td>
<td>$\degree$C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>$-60$ to $+150$</td>
<td>$\degree$C</td>
</tr>
<tr>
<td>Human Body Model ESD Capability (All pins except HV pin) per AEC--Q100--002 (JESD22--A114F)</td>
<td>HBM</td>
<td>$2$</td>
<td>kV</td>
</tr>
<tr>
<td>Charged--Device Model ESD Capability per AEC--Q100--11(JESD22--C101E)</td>
<td>CDM</td>
<td>$1$</td>
<td>kV</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Maximum drain current $I_{DS(pk)}$ is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 3 below provides spike limits the device can tolerate.
# ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ C$, for min/max values $T_J = -40^\circ C$ to $+125^\circ C$, $V_{CC} = 14$ V unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC(on)}$</td>
<td>$V_{CC}$ increasing level at which the switcher starts operation</td>
<td>2 (5)</td>
<td>8.4</td>
<td>9.0</td>
<td>9.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC(min)}$</td>
<td>$V_{CC}$ decreasing level at which the HV current source restarts</td>
<td>2 (5)</td>
<td>7.0</td>
<td>7.5</td>
<td>7.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC(off)}$</td>
<td>$V_{CC}$ decreasing level at which the switcher stops operation (UVLO)</td>
<td>2 (5)</td>
<td>6.7</td>
<td>7.0</td>
<td>7.2</td>
<td>V</td>
</tr>
<tr>
<td>$I_{CC1}$</td>
<td>Internal IC consumption, NCV1060 switching at 60 kHz, LIM/OPP = 0 A</td>
<td>2 (5)</td>
<td>–</td>
<td>0.92</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Internal IC consumption, NCV1060 switching at 100 kHz, LIM/OPP = 0 A</td>
<td>2 (5)</td>
<td>–</td>
<td>0.97</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Internal IC consumption, NCV1063 switching at 60 kHz, LIM/OPP = 0 A</td>
<td>2 (5)</td>
<td>–</td>
<td>0.99</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Internal IC consumption, NCV1063 switching at 100 kHz, LIM/OPP = 0 A</td>
<td>2 (5)</td>
<td>–</td>
<td>1.07</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CCskip}$</td>
<td>Internal IC consumption, COMP is 0 V (No switching on MOSFET)</td>
<td>2 (5)</td>
<td>–</td>
<td>340</td>
<td>–</td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

## POWER SWITCH CIRCUIT

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(on)}$</td>
<td>Power Switch Circuit on–state resistance $N_{CV1060}$ ($I_d = 50$ mA)</td>
<td>7, 8</td>
<td>–</td>
<td>34</td>
<td>41</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td>7, 8</td>
<td>–</td>
<td>65</td>
<td>72</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td>$T_J = 125^\circ C$</td>
<td>7, 8</td>
<td>–</td>
<td>11.4</td>
<td>14.0</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td>$N_{CV1063}$ ($I_d = 50$ mA)</td>
<td>7, 8</td>
<td>–</td>
<td>22</td>
<td>24</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$B_{DSS}$</td>
<td>Power Switch Circuit &amp; Startup breakdown voltage $I_{D(off)} = 120 \mu$A, $T_J = 25^\circ C$</td>
<td>7, 8</td>
<td>670</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS(off)}$</td>
<td>Power Switch &amp; Startup breakdown voltage off–state leakage current $T_J = 125^\circ C$ ($V_{DS} = 670$ V)</td>
<td>7, 8</td>
<td>–</td>
<td>84</td>
<td>–</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Switching characteristics ($R_L = 50 \Omega$, $V_{DS}$ set for $I_{drain} = 0.7 \times I_{lim}$)</td>
<td>7, 8</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$I_{drain}$ $90% - 10%$</td>
<td>7, 8</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{on(min)}$</td>
<td>Minimum on time $N_{CV1060}$, $N_{CV1063}$</td>
<td>7, 8</td>
<td>–</td>
<td>200</td>
<td>–</td>
<td>ns</td>
</tr>
</tbody>
</table>

## INTERNAL START–UP CURRENT SOURCE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{start1}$</td>
<td>High–voltage current source, $V_{CC} = V_{CC(on)} - 200$ mV</td>
<td>7, 8</td>
<td>5</td>
<td>8</td>
<td>12</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>($6–10$) $(13–16)$</td>
<td>7, 8</td>
<td>6–10</td>
<td>13–16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{start2}$</td>
<td>High–voltage current source, $V_{CC} = 0$ V</td>
<td>7, 8</td>
<td>–</td>
<td>0.5</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>($6–10$) $(13–16)$</td>
<td>7, 8</td>
<td>–</td>
<td>0.5</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{CCTH}$</td>
<td>$V_{CC}$ Transient level for $I_{start1}$ to $I_{start2}$ toggling point</td>
<td>2 (5)</td>
<td>–</td>
<td>1.4</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>$V_{start(min)}$</td>
<td>Minimum startup voltage, $V_{CC} = 0$ V</td>
<td>7, 8</td>
<td>–</td>
<td>21</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>($6–10$) $(13–16)$</td>
<td>7, 8</td>
<td>–</td>
<td>21</td>
<td>–</td>
<td>V</td>
</tr>
</tbody>
</table>

## CURRENT COMPARATOR

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IPK}$</td>
<td>Maximum internal current setpoint at 50% duty cycle $FB = 2$ V, LIM/OPP = 0 $\mu$A, $T_J = 25^\circ C$</td>
<td>7, 8</td>
<td>–</td>
<td>250</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$N_{CV1060}$</td>
<td>–</td>
<td>–</td>
<td>250</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$N_{CV1063}$</td>
<td>–</td>
<td>–</td>
<td>650</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IPK(0)}$</td>
<td>Maximum internal current setpoint at beginning of switching cycle $FB = 2$ V, LIM/OPP pin open $T_J = 25^\circ C$</td>
<td>7, 8</td>
<td>–</td>
<td>268</td>
<td>300</td>
<td>332</td>
</tr>
<tr>
<td></td>
<td>$N_{CV1060}$</td>
<td>–</td>
<td>268</td>
<td>300</td>
<td>332</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$N_{CV1063}$</td>
<td>–</td>
<td>702</td>
<td>780</td>
<td>858</td>
<td>mA</td>
</tr>
</tbody>
</table>

3. The final switch current is: $I_{IPK(0)} / (V_{in}/L_P + S_B) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with $S_B$ the built–in slope compensation, $V_{in}$ the input voltage, $L_P$ the primary inductor in a flyback, and $t_{prop}$ the propagation delay.
4. Oscillator frequency is measured with disabled jittering.
Table 5. ELECTRICAL CHARACTERISTICS (continued)
(For typical values $T_J = 25^\circ C$, for min/max values $T_J = -40^\circ C$ to $+125^\circ C$, $V_{CC} = 14$ V unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CURRENT COMPARATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IPKSW}$</td>
<td>Final switch current with a primary slope of 200 mA/μs, $F_{SW} = 60$ kHz (Note 3), LIM/OPP pin open</td>
<td>NCV1060</td>
<td>–</td>
<td>330</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NCV1063</td>
<td>–</td>
<td>740</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$I_{IPKSW}$</td>
<td>Final switch current with a primary slope of 200 mA/μs, $F_{SW} = 100$ kHz (Note 3), LIM/OPP pin open</td>
<td>NCV1060</td>
<td>–</td>
<td>320</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NCV1063</td>
<td>–</td>
<td>710</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$I_{LMDEC}$</td>
<td>Maximum internal current setpoint at beginning of switching cycle</td>
<td>NCV1060</td>
<td>–</td>
<td>128</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NCV1063</td>
<td>–</td>
<td>312</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$t_{SS}$</td>
<td>Soft-start duration (guaranteed by design)</td>
<td>–</td>
<td>4</td>
<td>–</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>$t_{PROP}$</td>
<td>Propagation delay from current detection to drain OFF state</td>
<td>–</td>
<td>70</td>
<td>–</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{LEB}$</td>
<td>Leading Edge Blanking Duration</td>
<td>NCV1060</td>
<td>–</td>
<td>130</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NCV1063</td>
<td>–</td>
<td>160</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>INTERNAL OSCILLATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{OSC}$</td>
<td>Oscillation frequency, 60 kHz version, $T_J = 25^\circ C$ (Note 4)</td>
<td>–</td>
<td>54</td>
<td>60</td>
<td>66</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{Jitter}$</td>
<td>Frequency jittering in percentage of $f_{OSC}$</td>
<td>–</td>
<td>–</td>
<td>±6</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>$f_{Swing}$</td>
<td>Jittering swing frequency</td>
<td>–</td>
<td>–</td>
<td>300</td>
<td>–</td>
<td>Hz</td>
</tr>
<tr>
<td>$D_{MAX}$</td>
<td>Maximum duty–cycle</td>
<td>–</td>
<td>62</td>
<td>66</td>
<td>72</td>
<td>%</td>
</tr>
<tr>
<td>ERROR AMPLIFIER SECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Voltage Feedback Input ($V_{COMP} = 2.5$ V)</td>
<td>4</td>
<td>3.2</td>
<td>3.3</td>
<td>3.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Input Bias Current ($V_{FB} = 3.3$ V)</td>
<td>4</td>
<td>–</td>
<td>1</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>$G_{M}$</td>
<td>Transconductance</td>
<td>5</td>
<td>2</td>
<td>–</td>
<td>–</td>
<td>mS</td>
</tr>
<tr>
<td>$I_{OTAlim}$</td>
<td>OTA maximum current capability ($V_{FB} &gt; V_{OTAen}$)</td>
<td>5</td>
<td>±150</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{OTAen}$</td>
<td>FB voltage to disable OTA</td>
<td>4</td>
<td>0.7</td>
<td>1.3</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>COMPENSATION SECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{COMPfault}$</td>
<td>COMP current for which Fault is detected</td>
<td>5</td>
<td>–</td>
<td>–40</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{COMP100%}$</td>
<td>COMP current for which internal current set–point is 100% ($I_{IPK(0)}$)</td>
<td>5</td>
<td>–</td>
<td>–44</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{COMPfreeze}$</td>
<td>COMP current for which internal current setpoint is:</td>
<td>5</td>
<td>–</td>
<td>–80</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$I_{Freeze1}$ or $I_{Freeze2}$ (NCV1060/3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{COMP(REF)}$</td>
<td>Equivalent pull–up voltage in linear regulation range</td>
<td>5</td>
<td>2.7</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(Guaranteed by design)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{COMP(up)}$</td>
<td>Equivalent feedback resistor in linear regulation range</td>
<td>5</td>
<td>17.7</td>
<td>–</td>
<td>–</td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td>(Guaranteed by design)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{LMOP}$</td>
<td>Voltage on LIM/OPP pin @ $I_{LMOP} = -35$ μA</td>
<td>3</td>
<td>1.40</td>
<td>1.50</td>
<td>1.60</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Voltage on LIM/OPP pin @ $I_{LMOP} = -250$ μA, $T_J = 25^\circ C$</td>
<td></td>
<td>1.28</td>
<td>1.35</td>
<td>1.42</td>
<td></td>
</tr>
<tr>
<td>$I_{LMOP}$</td>
<td>Maximum current from LIM/OPP pin</td>
<td>3</td>
<td>–</td>
<td>330</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{LMOP(min)}$</td>
<td>Current at which LIM/OPP starts to decrease $I_{PEAK}$</td>
<td>3</td>
<td>–20</td>
<td>–26</td>
<td>–32</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{LMOP(max)}$</td>
<td>Current at which LIM/OPP stops to decrease $I_{PEAK}$</td>
<td>3</td>
<td>–</td>
<td>–285</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{LMOP(neg)}$</td>
<td>Negative Active Clamp Voltage ($I_{LMOP} = -2.5$ mA)</td>
<td>3</td>
<td>–</td>
<td>–0.7</td>
<td>–</td>
<td>V</td>
</tr>
</tbody>
</table>

3. The final switch current is: $I_{IPK(0)} / (V_{Vin}/L_P + S_A) \times V_{Vin}/L_P + V_{Vin}/L_P \times t_{PROP}$, with $S_A$ the built–in slope compensation, $V_{Vin}$ the input voltage, $L_P$ the primary inductor in a flyback, and $t_{PROP}$ the propagation delay.
4. Oscillator frequency is measured with disabled jittering.
Table 5. ELECTRICAL CHARACTERISTICS (continued)  
(For typical values $T_J = 25^\circ C$, for min/max values $T_J = -40^\circ C$ to $+125^\circ C$, $V_{CC} = 14$ V unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>COMPENSATION SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LMOP(pos)}$</td>
<td>Positive Active Clamp (Guaranteed by design)</td>
<td>3 (6)</td>
<td>2.5</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FREQUENCY FOLDBACK &amp; SKIP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{COMPFold}$</td>
<td>Start of frequency foldback COMP pin current level</td>
<td>5 (8)</td>
<td>-768</td>
<td>-</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{COMPFold(end)}$</td>
<td>End of frequency foldback COMP pin current level, $f_{sw} = f_{min}$</td>
<td>5 (8)</td>
<td>-100</td>
<td>-</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$f_{min}$</td>
<td>The frequency below which skip-cycle occurs</td>
<td>-</td>
<td>21</td>
<td>25</td>
<td>29</td>
<td>kHz</td>
</tr>
<tr>
<td>$I_{COMPSkip}$</td>
<td>The COMP pin current level to enter skip mode</td>
<td>5 (8)</td>
<td>-120</td>
<td>-</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{Freeze1}$</td>
<td>Internal minimum current setpoint ($I_{COMP} = I_{COMPfreeze}$) in NCV1060</td>
<td>-</td>
<td>110</td>
<td>-</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{Freeze2}$</td>
<td>Internal minimum current setpoint ($I_{COMP} = I_{COMPfreeze}$) in NCV1063</td>
<td>-</td>
<td>270</td>
<td>-</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>RAMP COMPENSATION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$S_a(60)$</td>
<td>The internal ramp compensation @ 60 kHz: NCV1060 NCV1063</td>
<td>-</td>
<td>8.4</td>
<td>15.6</td>
<td>mA/µs</td>
<td></td>
</tr>
<tr>
<td>$S_a(100)$</td>
<td>The internal ramp compensation @ 100 kHz: NCV1060 NCV1063</td>
<td>-</td>
<td>14</td>
<td>26</td>
<td>mA/µs</td>
<td></td>
</tr>
<tr>
<td><strong>PROTECTIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SCP}$</td>
<td>Fault validation further to error flag assertion</td>
<td>-</td>
<td>35</td>
<td>48</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td>$I_{recovery}$</td>
<td>OFF phase in fault mode</td>
<td>-</td>
<td>400</td>
<td>-</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>$V_{OVP}$</td>
<td>$V_{CC}$ voltage at which the switcher stops pulsing</td>
<td>2 (5)</td>
<td>17.0</td>
<td>18.0</td>
<td>18.8</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OVP}$</td>
<td>The filter of $V_{CC}$ OVP comparator</td>
<td>-</td>
<td>80</td>
<td>-</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$V_{HV(EN)}$</td>
<td>The drain pin voltage above which allows MOSFET operate, which is detected after TSD, UVLO, SCP, or $V_{CC}$ OVP mode. (A version only)</td>
<td>7.8</td>
<td>67</td>
<td>87</td>
<td>110</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(6–10)</td>
<td></td>
<td>(13–16)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>TEMPERATURE MANAGEMENT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSD</td>
<td>Temperature shutdown (Guaranteed by design)</td>
<td>-</td>
<td>150</td>
<td>163</td>
<td>-</td>
<td>°C</td>
</tr>
<tr>
<td>TSD$_{hyst}$</td>
<td>Hysteresis in shutdown (Guaranteed by design)</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

3. The final switch current is: $I_{IPK(0)} / (V_{Vin}/L_P + S_a) \times V_{Vin}/L_P + V_{Vin}/L_P \times t_{prop}$, with $S_a$ the built-in slope compensation, $V_{Vin}$ the input voltage, $L_P$ the primary inductor in a flyback, and $t_{prop}$ the propagation delay.

4. Oscillator frequency is measured with disabled jittering.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
TYPICAL CHARACTERISTICS

Figure 4. $V_{CC(on)}$ vs. Temperature

Figure 5. $V_{CC(min)}$ vs. Temperature

Figure 6. $V_{CC(off)}$ vs. Temperature

Figure 7. $I_{DSS(off)}$ vs. Temperature

Figure 8. $I_{CC1}$ 60 kHz vs. Temperature

Figure 9. $I_{CC1}$ 100 kHz vs. Temperature
TYPICAL CHARACTERISTICS

Figure 10. $I_{PK(0)1060}$ vs. Temperature

Figure 11. $I_{PK(0)1063}$ vs. Temperature

Figure 12. $I_{start1}$ vs. Temperature

Figure 13. $I_{start2}$ vs. Temperature

Figure 14. $R_{DS(on)1060}$ vs. Temperature

Figure 15. $R_{DS(on)1063}$ vs. Temperature
NCV1060, NCV1063

TYPICAL CHARACTERISTICS

Figure 16. $f_{OSC_{60}}$ vs. Temperature

Figure 17. $f_{OSC_{100}}$ vs. Temperature

Figure 18. $I_{freeze1060}$ vs. Temperature

Figure 19. $I_{freeze1063}$ vs. Temperature

Figure 20. $D_{(max)}$ vs. Temperature

Figure 21. $f_{min}$ vs. Temperature
TYPICAL CHARACTERISTICS

Figure 22. $t_{\text{recovery}}$ vs. Temperature

Figure 23. $t_{\text{SCP}}$ vs. Temperature

Figure 24. $V_{\text{OVP}}$ vs. Temperature

Figure 25. $V_{\text{HV(EN)}}$ vs. Temperature

Figure 26. $V_{\text{REF}}$ vs. Temperature

Figure 27. $V_{\text{OTAen}}$ vs. Temperature

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TYPICAL CHARACTERISTICS

Figure 28. Drain Current Peak during Transformer Saturation vs. Junction Temperature

Figure 29. Breakdown Voltage vs. Temperature
NCV1060, NCV1063

APPLICATION INFORMATION

Introduction

The NCV106X offers a complete current–mode control solution. The component integrates everything needed to build a rugged and cost effective Switch–Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table, Table 6, details the differences between references, mainly peak current setpoints, $R_{DS(on)}$ value and operating frequency.

- **Current–mode Operation:** The controller uses current–mode control architecture.

- **670 V – Power MOSFET:** Due to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high–voltage power MOSFET featuring a 34 Ω or 11.4 Ω $R_{DS(on)} – T_j = 25^\circ C$. This value lets the designer build a power supply up to 8.6 W or 17.1 W operated on universal mains. An internal current source delivers the startup current, necessary to crank the power supply.

- **Dynamic Self–supply:** Due to the internal high voltage current source, this device could be used in the application without the auxiliary winding to provide supply voltage.

- **Short Circuit Protection:** by permanently monitoring the COMP line activity, the IC is able to detect the presence of a short–circuit, immediately reducing the output power for a total system protection. A tSCP timer is started as soon as the COMP current is below threshold, $I_{COMP\text{fault}}$, which indicates the maximum peak current. If at the end of this timer the fault is still present, then the device enters a safe, auto–recovery burst mode, affected by a fixed timer recurrence, $t_{\text{recovery}}$. Once the short has disappeared, the controller resumes and goes back to normal operation.

- **Built–in VCC Over Voltage Protection:** when the auxiliary winding is used to bias the VCC pin (no DSS), an internal comparator is connected to VCC pin. In case the voltage on the pin exceeds a level of $V_{OVP}$ (18 V typically), the controller immediately stops switching and waits a full timer period ($t_{\text{recovery}}$) before attempting to restart. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. a broken opto–coupler, the controller protects the load through a safe burst mode.

- **Line Detection:** An internal comparator monitors the drain voltage as recovering from one of the following situations:
  - Short Circuit Protection,
  - $V_{CC}$ OVP is confirmed,
  - UVLO,
  - TSD

- **Frequency Jittering:** an internal low–frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.

- **Soft–start:** a 4 ms soft–start ensures a smooth startup sequence, reducing output overshoots.

- **Frequency Foldback Capability:** a continuous flow of pulses is not compatible with no–load/light–load standby power requirements. To excel in this domain, the controller observes the COMP pin current information and when it reaches a level of $I_{COMP\text{fold}}$, the oscillator then starts to reduce its switching frequency as the feedback current continues to increase (the power demand continues to reduce). It can go down to 25 kHz (typical) reached for a feedback level of $I_{COMP\text{fold}}$ (100 µA roughly). At this point, if the power continues to drop, the controller enters classical skip–cycle mode.

- **Skip:** if SMPS naturally exhibits a good efficiency at nominal load, it begins to be less efficient when the output power demand diminishes. By skipping un–needed switching cycles, the NCV106X drastically reduces the power wasted during light load conditions.

- **Ipeak Set:** If current in range 26 µA and 285 µA is drawn from the pin, the peak current is proportionally reduced down to 40% of its original value. This feature enables to designer to set up the peak current to the value which is ideal for the application.

By routing a portion of the negative voltage present during the on–time on the auxiliary winding to the LIM/OPP pin, the user has a simple and non–dissipative means to alter the maximum peak current setpoint as the bulk voltage increases.
Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 8.0 mA) is biased and charges up the \( V_{CC} \) capacitor from the drain pin. Once the voltage on this \( V_{CC} \) capacitor reaches the \( V_{CC(on)} \) level (typically 9.0 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET if the bulk voltage is above \( V_{HV(EN)} \) level (87 V typically) for A version and if bulk voltage is above \( V_{start(min)} \) (21 V dc) for B version. There is no disable level for drain pin voltage, the device will stop switching when the input voltage is removed and sub-sequentially the \( V_{CC} \) reaches the \( V_{CC(OFF)} \) level, or \( t_{SCP} \) timer elapses. Figure 30 details the simplified internal circuitry.

Being loaded by the circuit consumption, the voltage on the \( V_{CC} \) capacitor goes down. When \( V_{CC} \) is below \( V_{CC(min)} \) level (7.5 V typically), it activates the internal current source to bring \( V_{CC} \) toward \( V_{CC(on)} \) level and stops again: a cycle takes place whose low frequency depends on the \( V_{CC} \) capacitor and the IC consumption. A 1.5 V ripple takes place on the \( V_{CC} \) pin whose average value equals \( (V_{CC(on)} + V_{CC(min)})/2 \). Figure 31 portrays a typical operation of the DSS.

Figure 30. The Internal Arrangement of the Start-up Circuitry
As one can see, even if there is auxiliary winding to provide energy for $V_{CC}$, it happens that the device is still biased by DSS during start-up time or some fault mode when the voltage on auxiliary winding is not ready yet. The $V_{CC}$ capacitor shall be dimensioned to avoid $V_{CC}$ crosses $V_{CC\text{off}}$ level, which stops operation. The $\Delta V$ between $V_{CC\text{(min)}}$ and $V_{CC\text{(off)}}$ is 0.5 V. There is no current source to charge $V_{CC}$ capacitor when driver is on, i.e. drain voltage is close to zero. Hence the $V_{CC}$ capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CCI} \cdot P_{\text{max}}}{f_{OSC} \cdot \Delta V} \quad \text{(eq. 1)}$$

Take the 60 kHz device as an example. $C_{VCC}$ should be above

$$\frac{0.8 \text{ m} \cdot 72\%}{54 \text{ kHz} \cdot 0.5} = 21 \text{ nF}.$$ 

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 $\mu$F is appropriate.

The $V_{CC}$ capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 30, an internal OVP comparator, protects the switcher against lethal $V_{CC}$ runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the over voltage protection (OVP) circuit and immediately stops the output pulses for $t_{\text{recovery}}$ duration (400 ms typically). Then a new start-up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

**Fault Condition – Short-circuit on $V_{CC}$**

In some fault situations, a short-circuit can purposely occur between $V_{CC}$ and GND. In high line conditions ($V_{HV} = 370 \text{ VDC}$) the current delivered by the startup device will seriously increase the junction temperature. For instance, since $I_{\text{start1}}$ equals 5 mA (the min corresponds to the highest $T_j$), the device would dissipate 370 x 5 m = 1.85 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, $I_{\text{start1}}$ and $I_{\text{start2}}$. At power-up, as long as $V_{CC}$ is below a 1.4 V level, the source delivers $I_{\text{start2}}$ (around 500 mA typical), then, when $V_{CC}$ reaches 1.4 V, the source smoothly transitions to $I_{\text{start1}}$ and delivers its nominal value. As a result, in case of short-circuit between $V_{CC}$ and GND, the power dissipation will drop to $370 \times 500 \mu A = 185 \text{ mW}$. Figure 31 portrays this particular behavior.

The first startup period is calculated by the formula $C \times V = I \times t$, which implies a 1 $\mu$ x 1.4 / 500 $\mu$ = 2.8 ms startup time for the first sequence. The second sequence is obtained by toggling the source to 8 mA with a delta V of $V_{CC\text{(on)}} - V_{CC\text{TH}} = 9.0 - 1.4 = 7.6$ V, which finally leads to a second startup time of 1 $\mu$ x 7.6 / 8 m = 0.95 ms. The total startup time becomes 2.8 m + 0.95 m = 3.75 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.
NCV1060, NCV1063

Fault Condition – Output Short–circuit
As soon as VCC reaches VCC(on), drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the VCC pin as the output voltage rises. During the start–sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. IIPK, which is reached after a typical period of 4 ms. When the output voltage is not regulated, the current coming through COMP pin is below ICOMPfault level (40 μA typically), which is not only during the startup period but also anytime an overload occurs, an internal error flag is asserted, IpFlag, indicating that the system has reached its maximum current limit set point. The assertion of this flag triggers a fault counter tSCP (48 ms typically). If at counter completion, IpFlag remains asserted, all driving pulses are stopped and the part stays off in trecovery duration (about 400 ms). A new attempt to re–start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty–cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 32 depicts this particular mode:

Auto–recovery Over Voltage Protection
The particular NCV106X arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 33 shows, a comparator monitors the VCC pin. If the auxiliary pushes too much voltage into the CVCC capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After trecovery delay, it resumes the internal drivers. If the failure symptom still exists, e.g. feedback opto–coupler fails, the device keeps the auto–recovery OVP mode. It is recommended insertion of a resistor (Rlimit) between the auxiliary dc level and the VCC pin to protect the IC against high voltage spikes, which can damage the IC, and to filter out the Vcc line to avoid undesired OVP activation. Rlimit should be carefully selected to avoid triggering the OVP as we discussed, but also to avoid disturbing the VCC in low / light load conditions.

Self–supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (Vnom), this voltage can drop below 10 V (Vstby) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re–fueling rate of the VCC capacitor is not enough to keep a proper auxiliary voltage.
**Soft-start**

The NCV106X features a 4 ms soft-start which reduces the power-on stress but also contributes to lower the output overshoot. Figure 35 shows a typical operating waveform.

The NCV106X features a novel patented structure which offers a better soft-start ramp, almost ignoring the start-up pedestal inherent to traditional current-mode supplies.
Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCV106X offers a ±6% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 36 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

Line Detection (for A version only)

An internal comparator monitors the drain voltage as recovering from one of the following situations:

- Short Circuit Protection,
- $V_{CC}$ OVP is confirmed,
- UVLO
- TSD

If the drain voltage is lower than the internal threshold $V_{HV(EN)}$ (87 Vdc typically), the internal power switch is inhibited. This avoids operating at too low ac input.

Figure 35. The 4 ms Soft-start Sequence

Figure 36. Modulation Effects on the Clock Signal by the Jittering Sawtooth
Frequency Foldback

The reduction of no–load standby power associated with the need for improving the efficiency, requires to change the traditional fixed–frequency type of operation. This device implements a switching frequency foldback when the COMP current passes above a certain level, $I_{\text{COMP}}^{\text{fold}}$, set around 68 $\mu$A. At this point, the oscillator enters frequency foldback and reduces its switching frequency.

The internal peak current set–point is following the COMP current information until its level reaches $I_{\text{freeze}}$. Below this value, the peak current setpoint is frozen to 30% of the $I_{PK(0)}$. The only way to further reduce the transmitted power is to diminish the operating frequency down to $F_{\text{min}}$ (25 kHz typically). This value is reached at a COMP current level of $I_{\text{COMP}}^{\text{fold}(end)}$ (100 $\mu$A typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise–free performance in no–load conditions. Figure 37 and Figure 38 depict the adopted scheme for the part.

![Figure 37](image1.png)

**Figure 37.** By Observing the Current on the COMP Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

![Figure 38](image2.png)

**Figure 38.** Ipk Set–point is Frozen at Lower Power Demand
Feedback and Skip

Figure 40 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current ($I_{COMP}$) is above 40 μA. In this linear operating range, the dynamic resistance is 17.7 kΩ typically ($R_{COMP(up)}$) and the effective pull up voltage is 2.7 V typically ($V_{COMP(REF)}$). When $I_{COMP}$ decreases, the COMP voltage will increase to 3.2 V.

Figure 41 depicts the skip mode block diagram. When the COMP current information reaches $I_{COMPskip}$, the internal clock setting the flip–flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for $V_{CC}$ pin and $V_{OUT}$ of power supply during skip mode. It eases the design of $V_{CC}$ over load range.
There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip-cycle disturbance brought by the current-sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the power switch on-time, this point dips to \( -N V_{in} \), \( N \) being the turns ratio between the primary winding and the auxiliary winding. The negative plateau on auxiliary winding will have an amplitude dependant on the input voltage. Resistors \( R_{OPPU} \) and \( R_{OPPL} \) (Figure 43) define current drawn from LIM/OPP and the negative voltage on auxiliary winding. The negative voltage is tied up with bulk voltage, so the higher the bulk voltage is, the deeper is the negative voltage on auxiliary winding, the higher current is drawn from LIM/OPP pin and the lower the peak current is. During the internal MOSFET off period, voltage on auxiliary winding is positive, but the IC ignores the LIM/OPP current. The positive LIM/OPP current has no influence on proper IC function.
Figure 43. The OPP Circuitry Affects the Maximum Peak Current Set Point

Ramp Compensation and Ipk Set-point
In order to allow the NCV106X to operate in CCM with a duty cycle above 50%, a fixed slope compensation is internally applied to the current-mode control.

Here we got a table of the ramp compensation, the initial current set point, and the final current set point of different versions of switcher.

<table>
<thead>
<tr>
<th></th>
<th>NCV1060</th>
<th>NCV1063</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SW}$</td>
<td>60 kHz</td>
<td>100 kHz</td>
</tr>
<tr>
<td>$S_a$</td>
<td>8.4 mA/μs</td>
<td>14 mA/μs</td>
</tr>
<tr>
<td>$I_{pk}(\text{Duty}=50%)$</td>
<td>250 mA</td>
<td>650 mA</td>
</tr>
<tr>
<td>$I_{pk}(0)$</td>
<td>300 mA</td>
<td>780 mA</td>
</tr>
</tbody>
</table>

Figure 44 depicts the variation of Ipk set-point vs. the power switcher duty ratio, which is caused by the internal ramp compensation.

FB Pin Function
The FB pin is used in non isolated SMPS application only. Portion of the output voltage is connected into the pin. The voltage is compared with internal $V_{REF}$ (3.3 V) using Operation Transconductance Amplifier (Figure 45). The OTAs output is connected to COMP pin. The OTA output is accessible through the COMP pin and is used for the loop compensation, usually an RC network. The current capability of OTA is limited to $-150 \ \mu A$ typically. The positive current is defined by internal $R_{COMP(\text{up})}$ resistor and $V_{COMP(\text{ref})}$ voltage. If FB path loop is broken (i.e. the FB pin is disconnected), an internal current $I_{FB}$ (1 μA typ.) will pull up the FB pin and the IC stops switching to avoid uncontrolled output voltage increasing.

In isolated topology, the FB pin should be connected to GND pin. In this configuration no current flows from OTA to COMP pin (OTA is disabled) so the OTA has no influence on regulation at all.
**NCV1060, NCV1063**

![Figure 45. FB Pin Connection](image)

**Design Procedure**

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

1. $V_{in\,min} = 90$ Vac or $127$ Vdc once rectified, assuming a low bulk ripple

   $V_{in\,max} = 265$ Vac or $375$ Vdc

   $V_{out} = 12$ V

   $P_{out} = 5$ W

   Operating mode is CCM

   $\eta = 0.8$

   1. The lateral MOSFET body–diode shall never be forward biased, either during start–up (because of a large leakage inductance) or in normal operation as shown in Figure 46. This condition sets the maximum voltage that can be reflected during toff. As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

   \[ N \cdot \left( V_{out} + V_f \right) < V_{in\,min} \] (eq. 2)

   2. In our case, since we operate from a $127$ V DC rail while delivering $12$ V, we can select a reflected voltage of $120$ V dc maximum. Therefore, the turn ratio $N_p:N_s$ must be smaller than

   \[ \frac{V_{reflect}}{V_{out} + V_f} = \frac{120}{12 + 0.5} \approx 9.6 \] or $N_p : N_s < 9.6$.

   Here we choose $N = 8$ in this case. We will see later on how it affects the calculation.

![Figure 46. The Drain–source Wave Shall always be Positive](image)
3. Lateral MOSFETs have a poorly doped body–diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

\[
V_{\text{drain,max}} = V_{\text{in}} + N \cdot (V_{\text{out}} + V_t) + I_{\text{peak}} \cdot \sqrt{\frac{L_f}{C_{\text{tot}}}} \quad \text{(eq. 3)}
\]

where \( L_f \) is the leakage inductance, \( C_{\text{tot}} \) the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), \( N \) the NP:NS turn ratio, \( V_{\text{out}} \) the output voltage, \( V_t \) the secondary diode forward drop and finally, \( I_{\text{peak}} \) the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the \( V_{\text{out}} \) target is almost reached and \( I_{\text{peak}} \) is still pushed to the maximum. For this design, we have selected our maximum voltage around 650 V (at \( V_{\text{in}} = 375 \text{ Vdc} \)). This voltage is given by the RCD clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating duty–cycle for this flyback converter operated in CCM:

\[
d_{\text{max}} = \frac{N \cdot (V_{\text{out}} + V_t)}{N \cdot (V_{\text{out}} \cdot V_t) + V_{\text{in,min}}} \quad \text{(eq. 4)}
\]

where \( \frac{1}{1 + \frac{V_{\text{in,min}}}{N \cdot (V_{\text{out}} \cdot V_t)}} = 0.44 \)

5. To obtain the primary inductance, we have the choice between two equations:

\[
L = \frac{\left(\frac{V_{\text{in}} \cdot d}{f_{\text{sw}}} \cdot K \cdot P_{\text{in}}\right)^2}{L_f \cdot C_{\text{tot}}} \quad \text{(eq. 5)}
\]

and defines the amount of ripple we want in CCM (see Figure 47).

- Small \( K \): deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- Large \( K \): approaching DCM where the RMS losses are worse, but smaller inductance, leading to a better leakage inductance.

From Equation 6, a \( K \) factor of 1 (50% ripple), gives an inductance of:

\[
L = \frac{(127 \cdot 0.44)^2}{60 \cdot 1 \cdot 5} = 10.04 \text{ mH}
\]

where \( K = \frac{\Delta I_L}{I_{L_{\text{avg}}}} \)

The peak current can be evaluated to be:

\[
I_{\text{peak}} = I_{\text{avg}} + \frac{\Delta I_L}{2} = 49.2 \text{ mA} + \frac{92.8 \text{ mA}}{2} = 158 \text{ mA}
\]

On \( I_L \), \( I_{L_{\text{avg}}} \) can also be calculated:

\[
I_{L_{\text{avg}}} = I_{\text{peak}} - \frac{\Delta I_L}{2} = 158 \text{ mA} - \frac{92.8 \text{ mA}}{2} = 111.6 \text{ mA}
\]

6. Based on the above numbers, we can now evaluate the conduction losses:

\[
I_{d_{\text{rms}}} = \sqrt{d \cdot \left(I_{\text{peak}}^2 - I_{\text{peak}}^2 \cdot \frac{\Delta I_L^2}{3}\right)}
\]

\[
= \sqrt{0.44 \cdot \left(0.158^2 - 0.158 \cdot 0.0928 + 0.0928^2\right)}
\]

\[
= 57 \text{ mA}
\]

If we take the maximum \( R_{DS(on)} \) for a 125°C junction temperature, i.e. 34 \( \Omega \), then conduction losses worse case are:

\[
P_{\text{cond}} = I_{d_{\text{rms}}}^2 \cdot R_{DS(on)} = 110 \text{ mW}
\]

7. Off–time and on–time switching losses can be estimated based on the following calculations:

\[
P_{\text{off}} = \frac{I_{\text{peak}} \cdot (V_{\text{bulk}} + V_{\text{clamp}}) \cdot t_{\text{off}}}{2T_{\text{sw}}}
\]

\[
= \frac{0.158 \cdot (127 + 100 \cdot 2) \cdot 10n}{2 \cdot 16.7 \mu} = 15.5 \text{ mW}
\]

Where, assume the \( V_{\text{clamp}} \) is equal to 2 times of reflected voltage.
\[ P_{on} = \frac{I_{valley} \cdot (V_{bulk} + N \cdot (V_{out} + V_f)) \cdot t_{on}}{6 \cdot T_{SW}} \] (eq. 7)

\[ = \frac{0.0464 \cdot (127 + 100) \cdot 10 \text{ n}}{6 \cdot 16.7 \mu} \]

\[ = 2.1 \text{ mW} \]

It is noted that the overlap of voltage and current seen on MOSFET during turning on and off duration is dependent on the snubber and parasitic capacitance seen from drain pin. Therefore the \( t_{off} \) and \( t_{on} \) in Equation 7 and Equation 8 have to be modified after measuring on the bench.

8. The theoretical total power is then
\[ 117 + 15.5 + 2.1 = 127.6 \text{ mW} \]

9. If the NCV106X operates at DSS mode, then the losses caused by DSS mode should be counted as losses of this device on the following calculation:
\[ P_{DSS} = I_{CC1} \cdot V_{in,max} = 0.8m \cdot 375 = 300 \text{ mW} \] (eq. 8)

**MOSFET Protection**

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BVdss which is 670 V. Figure 48 a–b–c present possible implementations:

**Figure 48. a, b, c: Different Options to Clamp the Leakage Spike**

Figure 48a: the simple capacitor limits the voltage according to the lateral MOSFET body–diode shall never be forward biased, either during start–up (because of a large leakage inductance) or in normal operation as shown by Figure 46. This condition sets the maximum voltage that can be reflected during \( t_{off} \). As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you must adopt a turn ratio which adheres to the following Equation 3. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with (Equation 4). Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses...

Figure 48b: the most standard circuitry is called the RCD network. You calculate \( R_{clamp} \) and \( C_{clamp} \) using the following formulæ:

\[ R_{clamp} = \frac{2 \cdot V_{clamp} \cdot (V_{clamp} + N \cdot (V_{out} + V_f))}{I_{leak} \cdot I_{leak}^2 \cdot f_{sw}} \] (eq. 9)

\[ C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot f_{sw} \cdot R_{clamp}} \]

\( V_{clamp} \) is usually selected 50–80 V above the reflected value \( N \cdot (V_{out} + V_f) \). The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when \( I_{peak} \) and \( V_{in} \) are maximum and \( V_{out} \) is close to reach the steady–state value.

Figure 48c: this option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worst case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded. As a good design practice, it is recommended to implement one of this protection to make sure Drain pin voltage doesn’t go above 650 V (to have some margin between Drain pin voltage and BVdss) during most stringent operating conditions (high \( V_{in} \) and peak power).
Power Dissipation and Heatsinking

The NCV106X welcomes two dissipating terms, the DSS current–source (when active) and the MOSFET. Thus, \( P_{\text{tot}} = P_{\text{DSS}} + P_{\text{MOSFET}} \). It is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the package. Take the SOIC–10 package as an example, when surrounded by a surface approximately 200 mm\(^2\) of 35 \( \mu \)m copper, the maximum power the device can thus evacuate is:

\[
P_{\text{max}} = \frac{T_{\text{jmax}} - T_{\text{ambmax}}}{R_{\theta JA}}
\]

(eq. 10)

which gives around 760 mW for an ambient of 50°C and a maximum junction of 150°C. If the surface is not large enough, the \( R_{\theta JA} \) is growing and the maximum power the device can evacuate decreases. Figure 49 gives a possible layout to help drop the thermal resistance.

![Figure 49. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction–to–Ambient](image)

Bill of material:
- C1 Bulk capacitor, input DC voltage is connected to the capacitor
- C2, R1, D1 Clamping elements
- C3 Vcc capacitor
- OK1 Optocoupler
- R2 Resistor to setting \( I_{\text{PEAK}} \) current

Table 6. ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Frequency</th>
<th>( R_{\text{DS(on)}} )</th>
<th>Brown In</th>
<th>Package Type</th>
<th>Shipping(^\dagger)</th>
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</thead>
<tbody>
<tr>
<td>NCV1060BD060R2G*</td>
<td>60 kHz</td>
<td>34</td>
<td>No</td>
<td>SOIC–10 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
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<tr>
<td>NCV1060BD100R2G*</td>
<td>100 kHz</td>
<td>34</td>
<td>No</td>
<td>SOIC–10 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
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<tr>
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<td>2500 / Tape &amp; Reel</td>
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<td>Yes</td>
<td>SOIC–16 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

\(^\dagger\) For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
# SOIC-16

## Mechanical Case Outline

**Case 751B-05**  
**Issue K**

**Date:** 29 Dec 2006

**Notes:**
2. Controlling dimension: Millimeter.
3. Dimensions A and B do not include mold protrusion.
4. Maximum mold protrusion: 0.15 (0.006) per side.
5. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall be 0.127 (0.005) total in excess of the D dimension at maximum material condition.

## Package Dimensions

### Notes:
- All dimensions are in millimeters
- All tolerances are ±0.025 (±0.001)

### Soldering Footprint

<table>
<thead>
<tr>
<th>Dim.</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>9.80</td>
<td>10.00</td>
<td>0.386</td>
<td>0.393</td>
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<tr>
<td>B</td>
<td>3.80</td>
<td>4.00</td>
<td>0.150</td>
<td>0.157</td>
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<tr>
<td>C</td>
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<td>1.75</td>
<td>0.054</td>
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<tr>
<td>D</td>
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</table>

## Soldering Footprint

- **Style 1:** Pin 1. Collector, Dye #1  
  2. Base, #1  
  3. Emitter, #1  
  4. Collector, #1  
  5. Collector, #2  
  6. Collector, #3  
  7. Collector, #4  
  8. Collector, #5  
  9. Collector, #6  
  10. Collector, #7  
  11. Collector, #8  
  12. Collector, #9  
  13. Collector, #10  
  14. Collector, #11  
  15. Collector, #12  
  16. Collector, #13

- **Style 2:** Pin 1. Cathode  
  2. Anode  
  3. Cathode  
  4. Cathode  
  5. Cathode  
  6. Cathode  
  7. Cathode  
  8. Cathode  
  9. Cathode  
  10. Cathode  
  11. Cathode  
  12. Cathode  
  13. Cathode  
  14. Cathode  
  15. Cathode  
  16. Cathode

- **Style 3:** Pin 1. Collector, Dye #1  
  2. Base, #1  
  3. Emitter, #1  
  4. Collector, #1  
  5. Collector, #2  
  6. Collector, #3  
  7. Collector, #4  
  8. Collector, #5  
  9. Collector, #6  
  10. Collector, #7  
  11. Collector, #8  
  12. Collector, #9  
  13. Collector, #10  
  14. Collector, #11  
  15. Collector, #12  
  16. Collector, #13

- **Style 4:** Pin 1. Collector, Dye #1  
  2. Collector, #1  
  3. Collector, #2  
  4. Collector, #3  
  5. Collector, #4  
  6. Collector, #5  
  7. Collector, #6  
  8. Collector, #7  
  9. Collector, #8  
  10. Collector, #9  
  11. Collector, #10  
  12. Collector, #11  
  13. Collector, #12  
  14. Collector, #13  
  15. Collector, #14  
  16. Collector, #15

- **Style 5:** Pin 1. Drain, Dye #1  
  2. Drain, #1  
  3. Drain, #2  
  4. Drain, #3  
  5. Drain, #4  
  6. Drain, #5  
  7. Drain, #6  
  8. Drain, #7  
  9. Drain, #8  
  10. Drain, #9  
  11. Drain, #10  
  12. Drain, #11  
  13. Drain, #12  
  14. Drain, #13  
  15. Drain, #14  
  16. Drain, #15

- **Style 6:** Pin 1. Cathode  
  2. Cathode  
  3. Cathode  
  4. Cathode  
  5. Cathode  
  6. Cathode  
  7. Cathode  
  8. Cathode  
  9. Cathode  
  10. Cathode  
  11. Cathode  
  12. Cathode  
  13. Cathode  
  14. Cathode  
  15. Cathode  
  16. Cathode

- **Style 7:** Pin 1. Source N-CH  
  2. Common Drain (Output)  
  3. Common Drain (Output)  
  4. GATE P-CH  
  5. Common Drain (Output)  
  6. Common Drain (Output)  
  7. Common Drain (Output)  
  8. Source P-CH  
  9. Source N-CH  
  10. Source #4  
  11. Source #5  
  12. Source #6  
  13. Source #7  
  14. Source #8  
  15. Source #9  
  16. Source #10

### Description:
- **98ASB42566B**

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SOIC-10 NB
CASE 751BQ
ISSUE B

DATE 26 NOV 2013

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIMENSIONING:

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.25</td>
<td>1.75</td>
</tr>
<tr>
<td>A1</td>
<td>0.10</td>
<td>0.25</td>
</tr>
<tr>
<td>A3</td>
<td>0.17</td>
<td>0.25</td>
</tr>
<tr>
<td>b</td>
<td>0.31</td>
<td>0.51</td>
</tr>
<tr>
<td>D</td>
<td>4.80</td>
<td>5.00</td>
</tr>
<tr>
<td>e</td>
<td>1.00</td>
<td>BSC</td>
</tr>
<tr>
<td>h</td>
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<td>BSC</td>
</tr>
<tr>
<td>L</td>
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</tr>
<tr>
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<tr>
<td>M</td>
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<td>8</td>
</tr>
</tbody>
</table>

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G”, may or not be present.

**For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.