

# NCP81045

## Product Preview

# Single Synchronous Step-Down Controller

The NCP81045 is a synchronous stepdown controller for high performance systems battery-power systems. The NCP81045 includes a high efficiency PWM controller. A pin is provided to allow two devices in interleaved operation. An internal power good voltage monitor tracks the SMPS output. NCP81045 also features soft-start sequence, UVLO for  $V_{CC}$  and switcher, overvoltage protection, overcurrent protection, undervoltage protection and thermal shutdown. The IC is packaged in QFN16.

### Features

- 0.8% accuracy 0.8 V Reference
- 4.5 V to 27 V Battery/Adaptor Voltage Range
- Adjustable Output Voltage Range: 0.8 V to 3.3 V
- Synchronization Interleaving between Two NCP81045s
- Skip Mode for Power Saving Operation at Light Load
- Lossless Inductor Current Sensing
- Programmable Transient-Response-Enhancement (TRE) Control
- Programmable Adaptive Voltage Positioning (AVP)
- Input Supply Feedforward Control
- Internal Soft-Start
- Integrated Output Discharge (Soft-Stop)
- Build-in Adaptive Gate Drivers
- PGOOD Indication
- Overvoltage, Undervoltage and Overcurrent Protections
- Thermal Shutdown
- QFN16 Package
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Notebook Application
- System Power

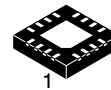
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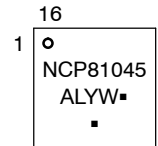
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### MARKING DIAGRAM

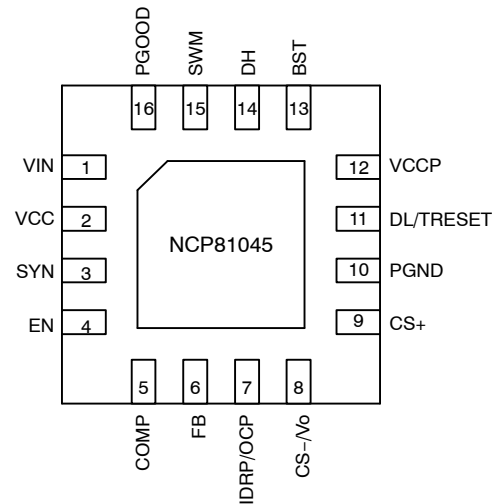


QFN16  
CASE 485AP



NCP81045 Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)



QFN16  
(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NCP81045MNTXG	QFN16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NCP81045

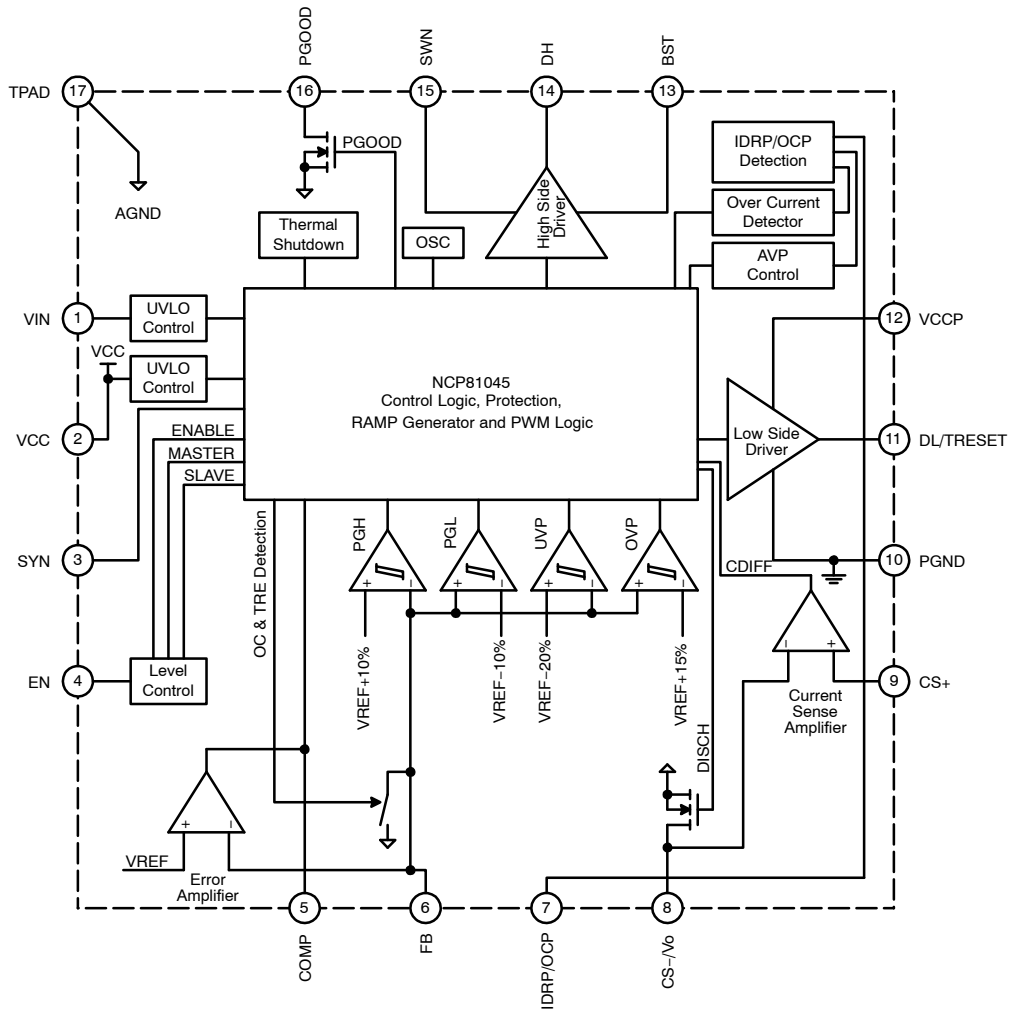


Figure 1. Detail Block Diagram

# NCP81045

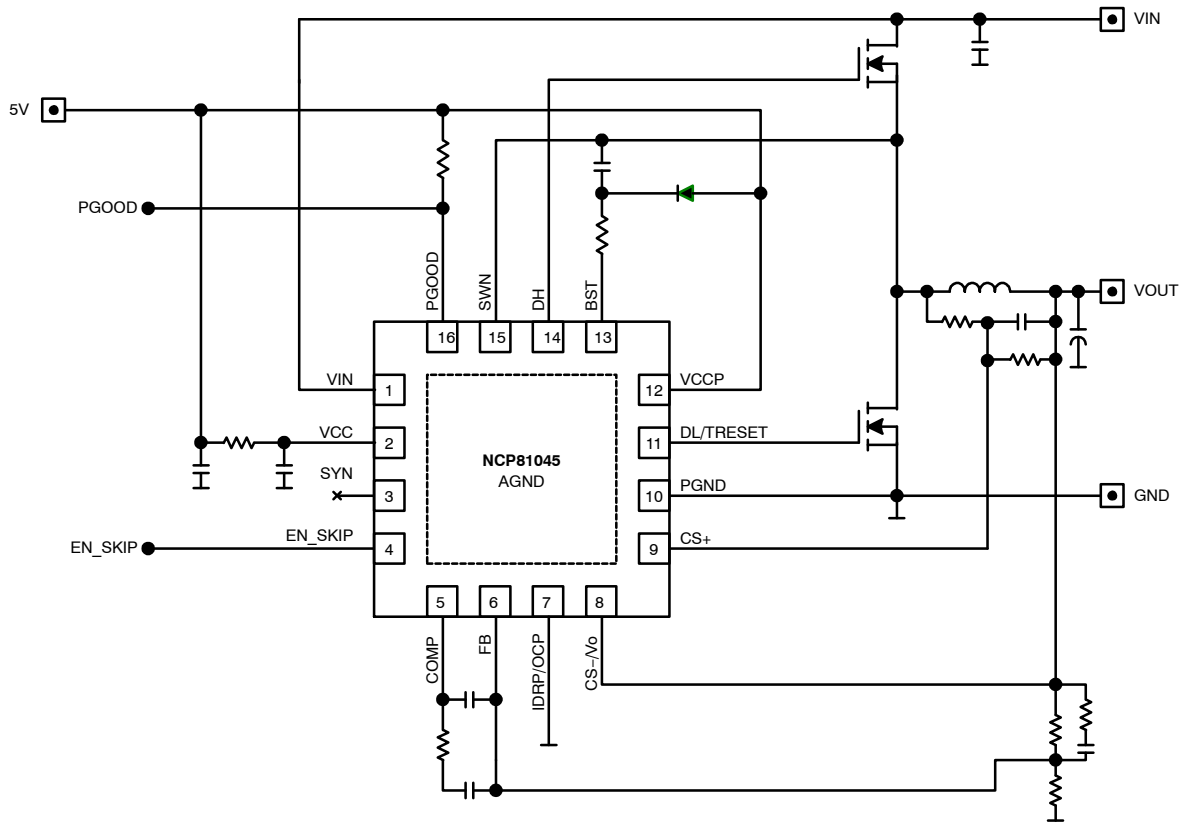


Figure 2. Typical Application Circuit (Single Device Operation)

# NCP81045

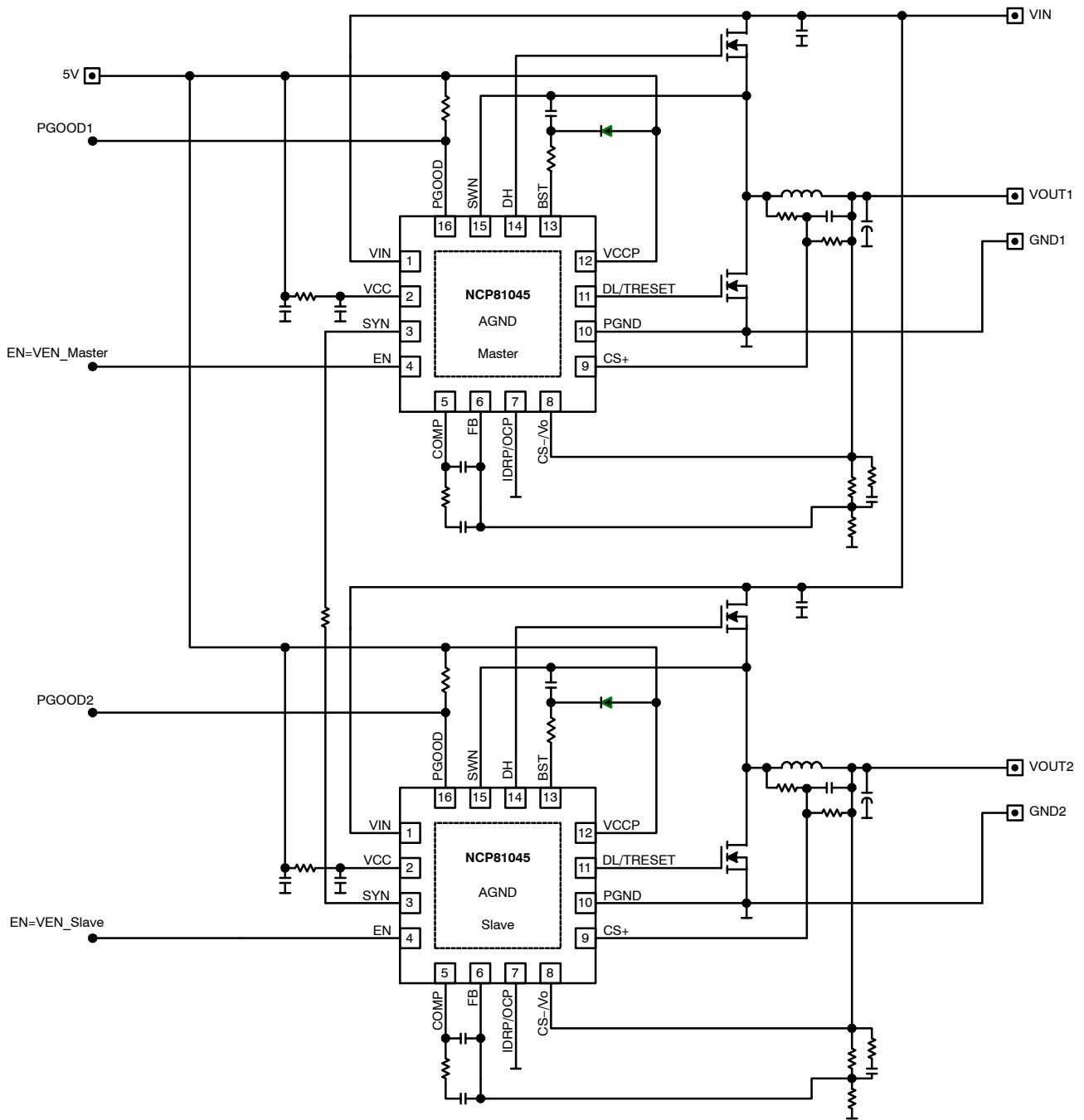


Figure 3. Typical Application Circuit (Dual Device Operation)

# NCP81045

## PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	VIN	Input voltage used for feed forward in switcher operation.
2	VCC	Supply for analog circuit
3	SYN	Synchronization interleaving use.
4	EN	This pin serves as two functions. Enable: Logic control for enabling the switcher. MASTER/SLAVE: To program the device as MASTER or SLAVE mode at dual device operation.
5	COMP	Output of the error amplifier.
6	FB	Output voltage feed back.
7	IDRP/OCP	Current limit programmable and setting for AVP.
8	CS-/Vo	Inductor current differential sense inverting input.
9	CS+	Inductor current differential sense non-inverting input.
10	PGND	Ground reference and high-current return path for the bottom gate driver.
11	DL/TRESET	Gate driver output of bottom N-channel MOSFET. It also has the function for TRE threshold setting.
12	VCCP	Supply for bottom gate driver.
13	BST	Top gate driver input supply, a bootstrap capacitor connection between SWN and this pin.
14	DH	Gate driver output of top N-channel MOSFET.
15	SWN	Switch node between top MOSFET and bottom MOSFET.
16	PGOOD	Power good indicator of the output voltage. High impedance if power good (in regulation). Low impedance if power not good.
17	TPAD	Copper pad on bottom of IC used for heat sinking. This pin should be connected to the analog ground plane under the IC.

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VCC Power Supply Voltage to AGND	$V_{CC}$	-0.3, 6.0	V
VIN Supply to AGND	$V_{IN}$	-0.3, 30	V
High-side Gate Drive Supply: BST to SWN High-side Gate Drive Voltage: DH to SWN Low-side Gate Drive Supply: VCCP to PGND Low-side Gate Drive Voltage: DL to PGND	$V_{BST-V_{SWN}}$ , $V_{DH-V_{SWN}}$ , $V_{CCP-V_{PGND}}$ , $V_{DL-V_{PGND}}$ ,	-0.3, 6.0	V
Input / Output Pins to AGND	$V_{IO}$	-0.3, 6.0	V
Switch Node SWN-PGND	$V_{SWN}$	-5 V (< 100 ns) 30 V	V
High-Side Gate Drive/Low-Side Gate Drive Outputs	DH, DL	-3(DC)	V
PGND	$V_{PGND}$	-0.3, 0.3	V
Thermal Characteristics Thermal Resistance Junction-to-Ambient (QFN16 Package)	$R_{\theta JA}$	48	°C/W
Operating Junction Temperature Range (Note 1)	$T_J$	-40 to +150	°C
Operating Ambient Temperature Range	$T_A$	-40 to +85	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C
Moisture Sensitivity Level	MSL	1	-

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

1. Internally limited by thermal shutdown, 150°C min.

# NCP81045

## ELECTRICAL CHARACTERISTICS ( $V_{IN} = 12\text{ V}$ , $V_{CC} = V_{CCP} = 5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
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### SUPPLY VOLTAGE

Input Voltage	$V_{IN}$		4.5	–	27	V
$V_{CC}$ Operating Voltage	$V_{CC}$		4.5	5.0	5.5	V

### SUPPLY CURRENT

$V_{CC}$ Quiescent Supply Current in Master operation	IVCC_Master	EN = VEN_Master, $V_{FB}$ forced above regulation point. DH, DL are open		1.5	2.5	mA
$V_{CC}$ Quiescent Supply Current in Slave Operation	IVCC_Slave	EN = VEN_Slave, $V_{FB}$ forced above regulation point, DH, DL are open		1.5	2.5	mA
$V_{CC}$ Shutdown Current	IVCC_SD	EN = VEN_Disable, $V_{CC} = 5\text{ V}$ , True Shutdown			1	$\mu\text{A}$
BST Quiescent Supply Current in Master Operation	IBST_Master	EN = VEN_Master, $V_{FB}$ forced above regulation point, DH and DL are open, No boost trap diode			0.3	mA
BST Quiescent Supply Current in Slave Operation	IBST_Slave	EN = VEN_Slave, $V_{FB}$ forced above regulation point, DH and DL are open, No boost trap diode			0.3	mA
BST Shutdown Current	IBST_SD	EN = 0 V			1	$\mu\text{A}$
VCCP Shutdown Current	IVCCP_SD	EN = 0 V, $V_{CCP} = 5\text{ V}$			1	$\mu\text{A}$
$V_{IN}$ Supply Current	IVIN	EN = 5V, $V_{IN} = 27\text{ V}$			35	$\mu\text{A}$
$V_{IN}$ Shutdown Current	IVIN_SD	EN = 0 V, $V_{IN} = 27\text{ V}$			1	$\mu\text{A}$

### VOLTAGE-MONITOR

Rising VCC Threshold	VCcTh+	Wake Up	4.05	4.25	4.48	V
VCC UVLO Hysteresis	VCcHYS		200	275	400	mV
Rising $V_{IN}$ Threshold	VINth+	Wake Up, Design Spec. (Note 2)	3.4	3.8	4.2	V
$V_{IN}$ UVLO Hysteresis	VINHYS	(Note 2)	200	500	800	mV
Power Good High Threshold	VPGH	PGOOD in from higher $V_o$ (PGOOD goes high)	120	125	130	%
Power Good High Hysteresis	VPGH_HYS	PGOOD high hysteresis (PGOOD goes low)		5		%
Power Good Low Threshold	VPGL	PGOOD in from lower $V_o$ (PGOOD goes high)	80	85	90	%
Power Good Low Hysteresis	VPGL_HYS	PGOOD low hysteresis (PGOOD goes low)		–5		%
Power Good High Delay	Td_PGH	After Tss, (Note 2)		1.25		ms
Power Good Low Delay	Td_PGL	(Note 2)		1.5		$\mu\text{s}$
Output Overvoltage Rising Threshold	OVpTh+	With respect to Error Comparator Threshold of 0.8 V	125	130	135	%
Overvoltage Fault Propagation Delay	OVPTblk	FB forced 2% above trip threshold (Note 2)		1.5		$\mu\text{s}$
Output Undervoltage Trip Threshold	UVpTh	With respect to Error Comparator Threshold of 0.8 V	75	80	85	%
Output Undervoltage Protection Blanking Time	UVPTblk	(Note 2)	–	8/fsw	–	s

### REFERENCE OUTPUT

Internal Reference Voltage	$V_{ref}$		0.7936	0.8	0.8064	V
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2. Guaranteed by design, not tested in production.

# NCP81045

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Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
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## OSCILLATOR

Operation Frequency	$F_{SW}$		270	300	330	kHz
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## OVERCURRENT THRESHOLD

Total Detection Time	$T_{DETECT}$	Period of FB shorts to ground before SS	1.26	1.92	2.21	ms
OCSET Detection Time	$T_{OCDET}$	(Note 2)	1.09		1.47	ms

## INTERNAL SOFT-START

Soft-Start Time	TSS		0.9	1.1	1.3	ms
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## VOLTAGE ERROR AMPLIFIER

DC Gain	GAIN_VEA	(Note 2)		88		dB
Unity Gain Bandwidth	BW_VEA	(Note 2)		15		MHz
Slew Rate	SR_VEA	COMP PIN TO GND = 100 pF (Note 2)		2.5		V/ $\mu$ s
FB Bias Current	Ibias_FB				0.1	$\mu$ A
Output Voltage Swing	Vmax_EA	Isource_EA = 2 mA	3.3	3.5		V
	Vmin_EA	Isink_EA = 2 mA		0.15	0.3	V

## DIFFERENTIAL CURRENT SENSE AMPLIFIER

CS+ and CS- Common-mode Input Signal Range	VCSCOM_MAX	Refer to AGND			3.5	V
Input Bias Current	CS_IIB		-100		100	nA
Input Signal Range	CS_range		-70		70	mV
Offset Current at IDRP	IDRP_offset	(CS+) - (CS-) = 0 V	-1.0		1.0	$\mu$ A
[(CS+) - (CS-)] to IDRP Gain	IDRP_GAIN (IDRP/((CS+) - (CS-)))	(CS+) - (CS-) = 10 mV, V(IDRP) = 0.8 V	0.475	0.525	0.575	$\mu$ A/mV
			0.425		0.625	$\mu$ A/mV
Current-Sense Bandwidth	BW_CS	At -3dB to DC Gain (Note 2)		20		MHz
Maximum IDRP Output Voltage	IDRP_Max	(CS+) - (CS-) = 70 mV, Isource drops to 95% of the value when V(IDRP) = 0.8 V	2.5			V
Minimum IDRP Output Voltage	IDRP_Min			0		V
IDRP Output current	I_IDRP		-1.0		35	$\mu$ A

## OVERCURRENT PROTECTION SETTING

Overcurrent Threshold (OCTH) Detection Current	I_OCSET	Sourced from OCP before soft-start, Rocset = 16.7 k $\Omega$ is connected from OCP to AGND or FB	21.6	24	26.4	$\mu$ A
Ratio of OC Threshold over OCSET Voltage	K_OCSET	V((CS+) - (CS-)) / V_OCSET (Note 2)		0.1		-
OCSET Voltage for Default Fixed OC Threshold	VOCSET_DFT	Rocset $\leq$ 2 k $\Omega$ is connected from OCP to AGND or FB			100	mV
OCSET Voltage for Adjustable OC Threshold	VOCSET_ADJ	Rocset = 8.3 ~ 25 k $\Omega$ is connected from OCP to AGND or FB	200		600	mV
OCSET Voltage for OC Disable	VOCSET_DIS	Rocset $\geq$ 35 k $\Omega$ is connected from OCP to AGND or FB	720			mV
Default Fixed OC Threshold	V_OCTH_DFT	(CS+) - (CS-), Pin OCP is shorted to AGND or FB	35	40	45	mV

2. Guaranteed by design, not tested in production.

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Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OVERCURRENT PROTECTION SETTING

Adjustable OC Threshold	V_OCTH ((CS+)-(CS-))	(CS+) – (CS-), During OC threshold, set a voltage at pin OCP	15	20	25	mV
			52	60	68	

### GATE DRIVERS

DH Pull-HIGH Resistance	RH_DH	200 mA Source current		1		$\Omega$
DH Pull-LOW Resistance	RL_DH	200 mA Sink current		1		$\Omega$
DL Pull-HIGH Resistance	RH_DL	200 mA Source current		1		$\Omega$
DL Pull-LOW Resistance	RL_DL	200 mA Sink current		0.5		$\Omega$
DH Source Current	Isource_DH	(Note 2)		2.5		A
DH Sink Current	Isink_DH	(Note 2)		2.5		A
DL Source Current	Isource_DL	(Note 2)		2.5		A
DL Sink Current	Isink_DL	(Note 2)		5		A
Dead Time	TD_LH	DL-off to DH-on (Note 2)		20		ns
	TD_HL	DH-off to DL-on (Note 2)		20		ns
Negative Current Detection Threshold	NCD_TH	SWN – PGND, at EN = 5 V		-1		mV
SWN source leakage	ISWN_SD	EN = 0 V, SWN = 0 V			1	$\mu\text{A}$
Internal Resistor from DH to SWN	R_DH_SWN	(Note 2)		100		k $\Omega$

### CONTROL SECTION

EN Logic Input Voltage for Disable	VEN_Disable	Set as Disable	0.7	1.0	1.3	V
		Hysteresis	150	200	250	mV
EN Logic Input Voltage for MASTER Mode	VEN_Master	Set as Master Mode	1.7	1.95	2.25	V
EN Logic Input Voltage for SLAVE Mode	VEN_Slave	Set as Slave Mode	2.4	2.65	2.9	V
		Hysteresis	100	175	250	mV
EN Source Current	IEN_SOURCE	VEN = 0 V			0.1	$\mu\text{A}$
EN Sink Current	IEN_SINK	VEN = 5 V			0.1	$\mu\text{A}$
PGOOD Pin ON Resistance	PGOOD_R	I_PGOOD = 5 mA		100		$\Omega$
PGOOD Pin OFF Current	PGOOD_LK				1	$\mu\text{A}$

### SYNC CONTROL

SYNC pin leakage	ISYNC_LK	Set as Slave Mode, SYNC = 5 V			1	$\mu\text{A}$
SYNC frequency	F_SYNC	(Note 2)		1.2		MHz
Pulse Width	PW_SYNC	(Note 2)		416		ns
Clock Level Low	V_CLKL	(Note 2)		0		V
Clock Level High	V_CLKH	(Note 2)		5		V
SYNC Driving Capability	SYNC_CL	Set as Master Mode, load capacitor between SYNC and GND (Note 2)			20	pF
SYNC Source Current	ISYNC	SYNC shorts to ground			20	mApp

### OUTPUT DISCHARGE MODE

Output Discharge On-Resistance	Rdischarge	EN = 0 V		20	35	$\Omega$
Threshold for Discharge Off	Vth_DisOff		0.2	0.3	0.4	V

2. Guaranteed by design, not tested in production.



# NCP81045

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Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
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## TRE SETTING

TRE Threshold Detection Current	I_TRESET	Sourced from DL in the short period before soft-start. (Rtre = 47 k $\Omega$ is connected from DL to GND)	7.2	8	8.8	$\mu\text{A}$
Detection Voltage for TRE Threshold Selection	VDL_TRE_1 (Default)	Internal TRE_TH is set to 300 mV	500	600	700	mV
	VDL_TRE_2	Internal TRE_TH is set to 500 mV	300		450	
	VDL_TRE_3	TRE is Disabled	0		250	
TRE Comparator Offset	TRE_OS	(Note 2)		10		mV
Propagation Delay of TRE Comparator	TD_PWM	(Note 2)		20		ns

## THERMAL SHUTDOWN

Thermal Shutdown	Tsd	(Note 2)		150		$^\circ\text{C}$
Thermal Shutdown Hysteresis	Tsdhys	(Note 2)		25		$^\circ\text{C}$

2. Guaranteed by design, not tested in production.

TYPICAL OPERATING CHARACTERISTICS

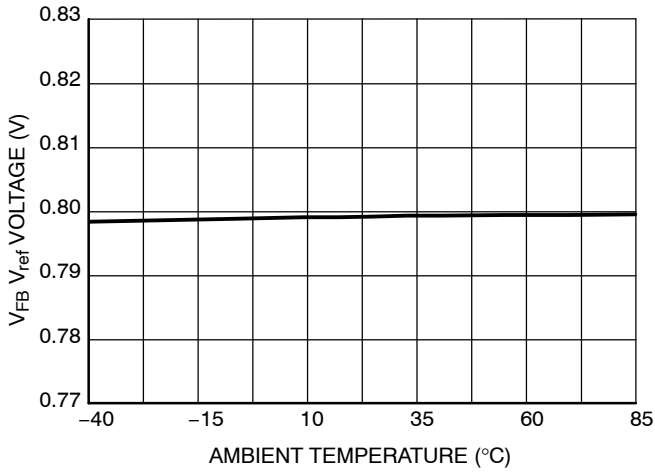


Figure 4. V<sub>ref</sub> Voltage vs Ambient Temperature

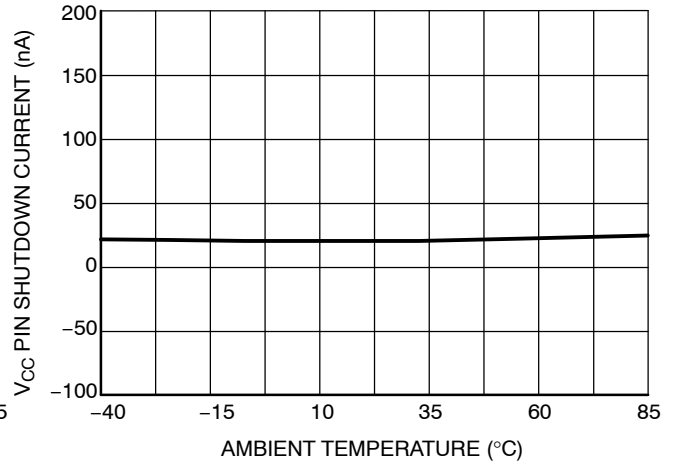


Figure 5. V<sub>CC</sub> Shutdown Current vs Ambient Temperature

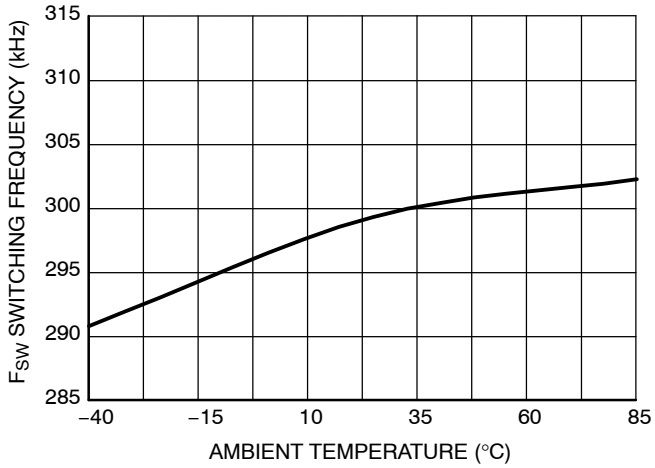


Figure 6. Switching Frequency vs Ambient Temperature

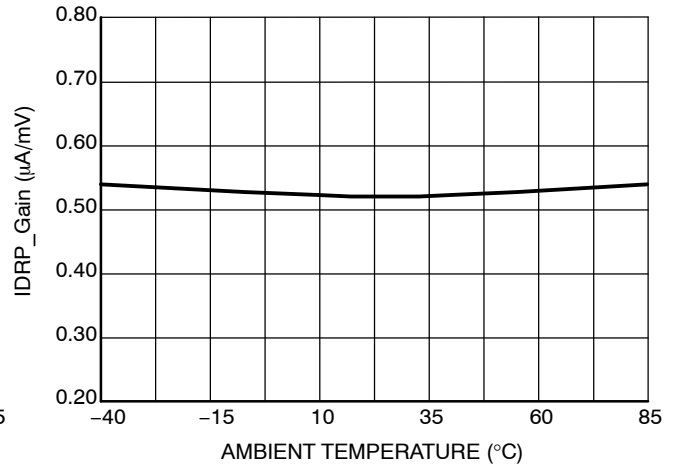


Figure 7. IDR Gain vs Ambient Temperature

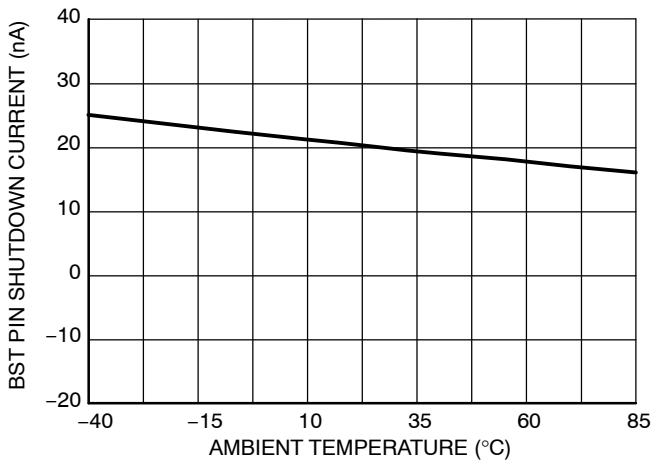


Figure 8. BST Shutdown Current vs Ambient Temperature

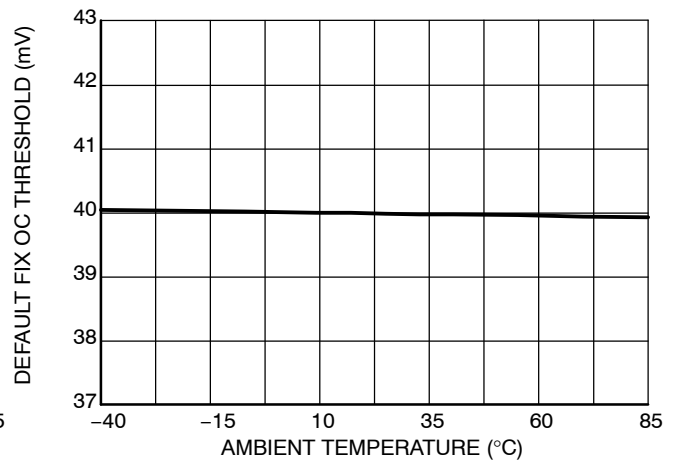
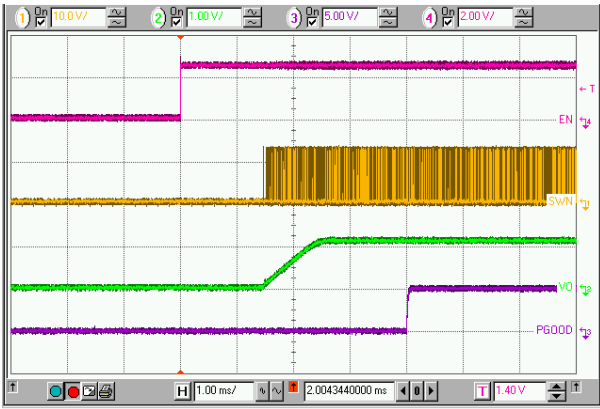
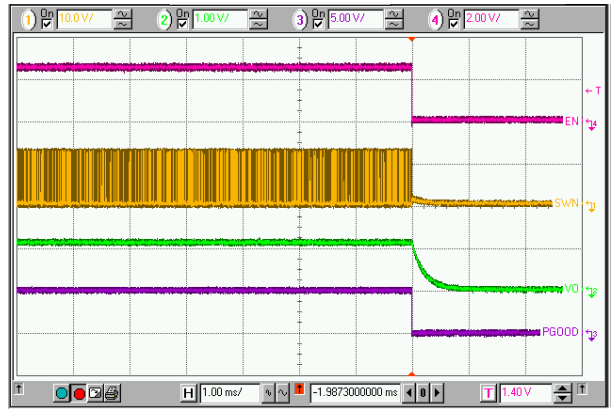


Figure 9. Default Fix OC Threshold vs Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS



Top to Bottom: EN, SWN, Vo, PGOOD  
**Figure 10. Powerup Sequence**



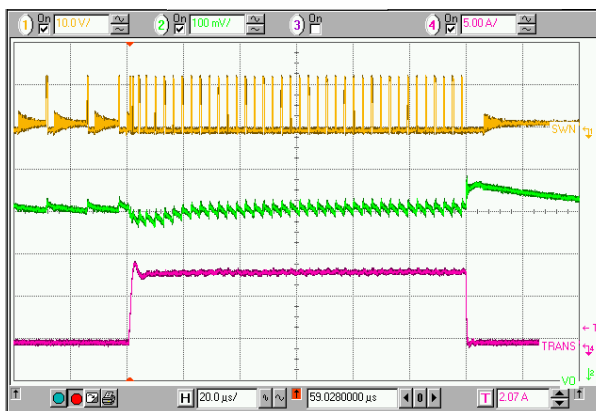
Top to Bottom: EN, SWN, Vo, PGOOD  
**Figure 11. Powerdown Sequence**



Top to Bottom: SWN\_Slave, Vo\_Slave, SWN\_Master, Sync\_clk  
**Figure 12. From Unsync to Sync**



Top to Bottom: SWN\_Slave, Vo\_Slave, SWN\_Master, Sync\_clk  
**Figure 13. From Sync to Unsync**



Top to Bottom: SWN, Vo, Io  
**Figure 14. Typical Transient**

DETAILED OPERATING DESCRIPTION

**General**

The NCP81045 synchronous stepdown power controller contains a PWM controller for wide battery/adaptor voltage range applications

The NCP81045 includes power good voltage monitor, soft-start, overcurrent protection, undervoltage protection, overvoltage protection and thermal shutdown. The NCP81045 features power saving function which can increase the efficiency at light load. It is ideal for battery operated systems. The IC is packaged in QFN16.

**Control Logic**

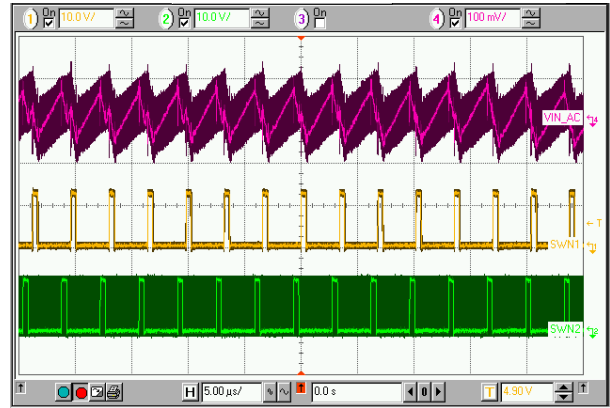
The internal control logic is powered by  $V_{CC}$ . The device is controlled by an EN pin. The EN pin serves two functions. When voltage of EN is below  $V_{EN\_Disable}$ , it shuts down the device. When the voltage of EN is at the level of  $V_{EN\_Master}$ , the device is operating as Master mode. When voltage level of EN is at  $V_{EN\_Slave}$ , the device is operating as Slave mode. It should be noted that no matter the device is operating either at Master or Slave mode, the device is operating in the manner of auto power saving condition such that it operates as skip mode automatically at light load. When EN is above  $V_{EN\_Disable}$ , the internal  $V_{ref}$  is activated and power-on reset occurs which resets all the protection faults. Once  $V_{ref}$  reaches its regulation voltage, an internal signal will wake up the supply undervoltage monitor which will assert a “GOOD” condition. In addition, the NCP81045 continuously monitors  $V_{CC}$  and  $V_{IN}$  levels with undervoltage lockout (UVLO) function.

**Single Device Operation**

The device is operating as single device operation when the SYNC pin is pull to ground. Under this configuration, the device will use the internal clock for normal PWM operation.

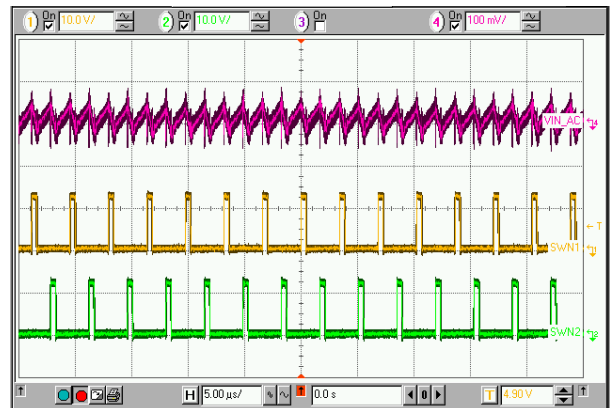
**Dual Device Operation (Master/Slave Mode)**

The device is operating as Master/Slave mode if two devices are tied up together. (Detail configuration please see the application schematic) One device is served as Master and another one is served as Slave. Once they already, they are synchronized to each other and they are operating as “interleaved” mode such that the phase shift of their switching clocks is 180°. It has the benefit that the amount of ripple current at the  $V_{IN}$  will be lower and hence lesser bulk capacitors at  $V_{IN}$  to save the confined PCB space and material cost. Figure 15 and Figure 16 show the difference when the devices are operating independently (unsynchronized) and operating at interleaved mode (Synchronized). It can be seen that at the unsynchronized condition, the system is obviously noisy because of high ripple voltage at  $V_{IN}$  (ripple voltage directly reflects the amount of ripple current at  $V_{IN}$ ). Once the devices are operating at interleaving mode, the overall  $V_{IN}$  ripple current is significantly reduced.



Top to Bottom: VIN AC Voltage, SWN\_Slave, SWN\_Master

**Figure 15. Two Devices are Unsynchronized**

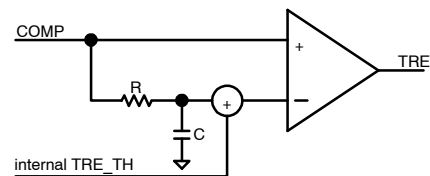


Top to Bottom: VIN AC Voltage, SWN\_Slave, SWN\_Master

**Figure 16. Two Devices are in Interleaved Operation**

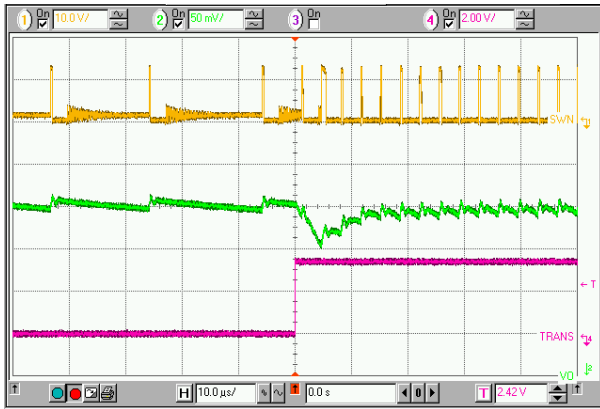
**Transient Response Enhancement (TRE)**

For the conventional PWM controller in CCM, the fastest response time is one switching cycle in the worst case. To further improve transient response in CCM, a transient response enhancement circuitry is implemented inside the NCP81045. In CCM operation, the controller is continuously monitoring the COMP pin output voltage of the error amplifier to detect the load transient events. The functional block diagram of TRE is shown below.



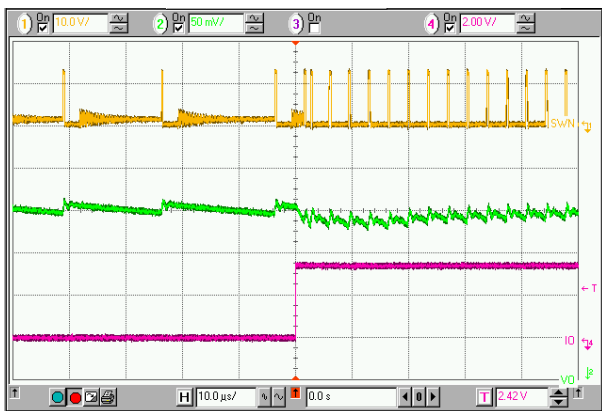
**Figure 17. Block Diagram of TRE Circuit**

Once the large transient occurs, the COMP signal may be large enough to exceed the threshold and then TRE “flag” signal will be asserted in a short period which is typically around one normal switching cycle. In this short period, the controller will be running at high frequency and hence has faster response. After that the controller comes back to normal switching frequency operation. We can program the internal TRE threshold (TRE\_TH). For detail please see the electrical table of “TRE Setting” section. Basically, the recommend internal TRE threshold value is around 1.5 times of peak-to-peak value of the COMP signal at CCM operation. The higher the internal TRE\_TH, the lower sensitivity to load transient. The TRE function can be disable by setting the Rtre which is connecting to DL/TRE pin to less than 25 kΩ. For system component saving, it is usually set as default value, that is, Rtre is open (≥ 75 kΩ) and internal TRE\_TH is 300 mV typical.



Top to Bottom SWN, Vo, Transient Signal

Figure 18. Transient Response with TRE Disable



Top to Bottom SWN, Vo, Transient Signal

Figure 19. Transient Response with TRE Enable

**Adaptive Voltage Positioning (AVP)**

For applications with fast transient currents, adaptive voltage positioning can reduce peak-to-peak output voltage deviations due to load transients. With the use of AVP, the output voltage allows to have some controlled sag when load current is applied. Upon removal of the load, the output voltage returns no higher than the original level, just allowing one output transient peak to be cancelled over a load step up and release cycle. The amount of AVP is adjustable.

The behaviors of the Vo waveforms with or without AVP are depicted at Figure 20.

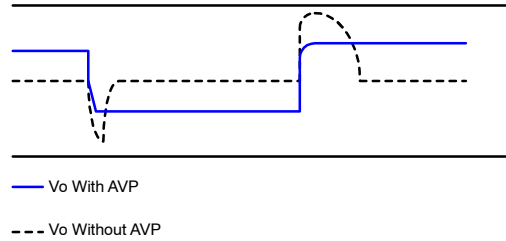


Figure 20. Adaptive Voltage Positioning

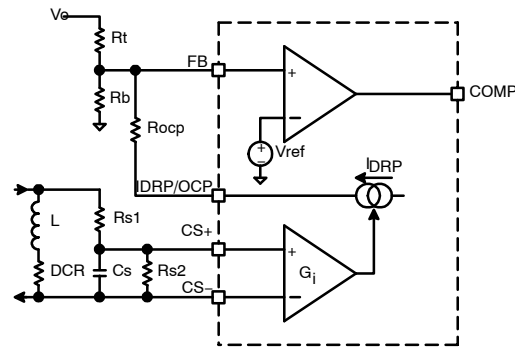


Figure 21. Configuration for AVP Function

The Figure 21 shows how to realize the AVP function. A current path is connecting to the FB pin via R<sub>ocp</sub> resistor. R<sub>ocp</sub> is not actually for AVP function, indeed, R<sub>ocp</sub> is used for OCP threshold value programming. The IDR/OCP pin has dual functions: OCP programming and AVP. At the IDR/OCP pin, conceptually there is a current source which is modulated by current sensing amplifier.

The output voltage V<sub>o</sub> with AVP is:

$$V_o = V_{o0} - I_o * R_{LL} \tag{eq. 1}$$

Where I<sub>o</sub> is the load current, no load output voltage V<sub>o0</sub> is set by the external divider that is:

$$V_{o0} = \left( 1 + \frac{R_t}{R_b} \right) * V_{ref} \tag{eq. 2}$$

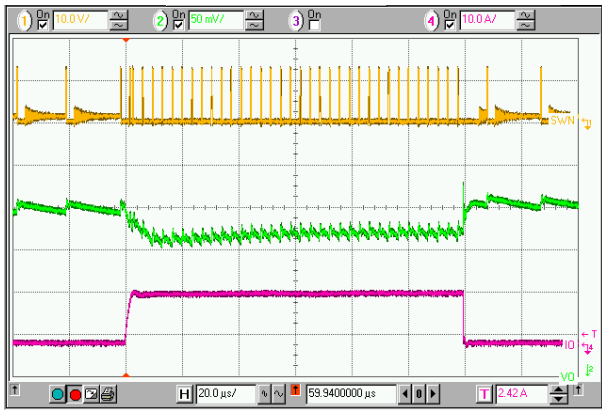
The load line impedance  $R_{LL}$  is given by:

$$R_{LL} = DCR * Gain\_CS * R_t * \frac{R_{s2}}{R_{s1} + R_{s2}} \quad (\text{eq. 3})$$

Where DCR is inductor DC resistance. Gain\_CS is a gain from [(CS+)-(CS-)] to IDRPin Gain (At electrical table, the symbol is IDRPin\_GAIN), the typical value is 0.525  $\mu\text{A}/\text{mV}$ .

The AVP function can be easily disabled by shorting the R<sub>ocp</sub> resistor into ground.

From the equation we can see that the value of “top” resistor R<sub>t</sub> can affect the amount of R<sub>LL</sub>, so it is recommended to define the amount of R<sub>LL</sub> FIRST before defining the compensation component value. And if the user wants to fine tune the compensation network for optimizing the transient performance, it is NOT recommend to adjust the value of R<sub>t</sub>. Otherwise, both transient performance and AVP amount will be affected. The following diagram shows the typical waveform of AVP. Note that the R<sub>t</sub> typical value should be above 1 k $\Omega$ .



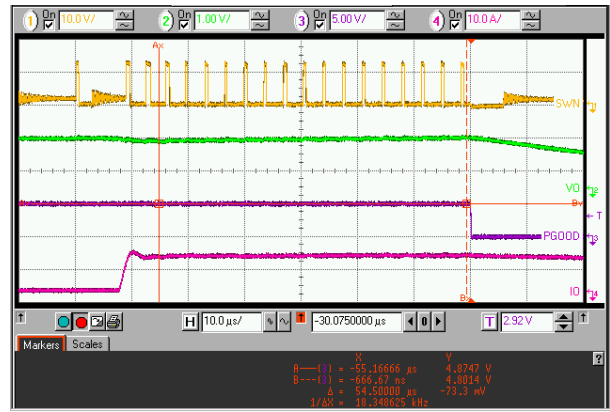
Top to Bottom: SWN, Vo, Transient Signal

Figure 22. Typical waveform of AVP

**Over Current Protection (OCP)**

The NCP81045 protects power system if over current event occurs. The current is continuously monitored by the differential current sensing circuit. The current limit threshold voltage VOCSET can be programmed by resistor ROCSET connecting at the IDRPin/OCP pin. However, fixed default VOCSET can be achieved if ROCSET is less than 2 k $\Omega$ .

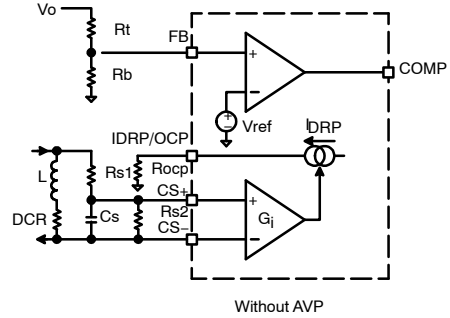
If the inductor current exceeds the current threshold continuously, the top gate driver will be turned off cycle by cycle. If it happens over consecutive 16 clock cycles time (16 x 1/f<sub>SW</sub>), the device is latched off such that top and bottom gate drivers are off. EN resets or power recycle the device can exit the fault. The following diagram shows the typical behavior of OCP.



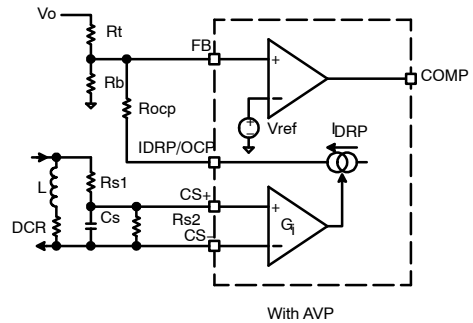
Top to Bottom : SWN, Vo, PGOOD, Io

Figure 23. Overcurrent Protection

The NCP81045 uses lossless inductor current sensing for acquiring current information. In addition, the threshold OCP voltage can be programmed to some desired value by setting the programming resistor R<sub>ocp</sub>.



Without AVP



With AVP

Figure 24. OCP Configuration

It should be noted that there are two configurations for R<sub>ocp</sub> resistor. If Adaptor Voltage Position (AVP) is used, the R<sub>ocp</sub> should be connected to FB pin. If AVP is not used, the R<sub>ocp</sub> should be connected to ground. At the IDRPin/OCP pin, there is a constant current(24  $\mu\text{A}$  typ.) flowing out during the programming stage at system start up. This is used to sense

the voltage level which is developed by a resistor  $R_{ocp}$  so as to program the overcurrent detection threshold voltage. For typical application, the  $V_{octh}$  is set as default value(40 mV typ) by setting  $R_{ocp} = 0 \Omega$ , or directly short the IDRPO/OC pin to ground. It has the benefit of saving one component at application board. For other programming values of  $V_{octh}$ , please refer to the electrical table of “Overcurrent Protection Setting” section.

**Guidelines for selecting OCP Trip Component**

1. Choose the value of  $R_{ocp}$  for  $V_{octh}$  selection.
2. Define the DC value of OCP trip point( $I_{ocp\_DC}$ ) that you want. The typical value is 1.5 to 1.8 times of maximum loading current. For example, if maximum loading is 10 A, then set OCP trip point at 15 A to 18 A.
3. Calculate the inductor peak current ( $I_{pk}$ )which is estimated by the equation:

$$I_{pk} = I_{ocp\_DC} + \frac{V_o * (V_{IN} - V_o)}{2 * V_{IN} * f_{SW} * L_o} \quad (eq. 4)$$

4. Check with inductor datasheet to find out the value of inductor DC resistance DCR, then calculate the RS1, RS2 dividing factor k based on the equation:

$$k = \frac{V_{octh}}{I_{pk} * DCR} \quad (eq. 5)$$

5. Select  $C_S$  value between 100 nF to 200 nF. Typically, 100 nF will be used.
6. Calculate Rs1 value by the equation:

$$Rs1 = \frac{L}{k * DCR * C_s} \quad (eq. 6)$$

7. Calculate Rs2 value by the equation:

$$Rs2 = \frac{k * Rs1}{1 - k} \quad (eq. 7)$$

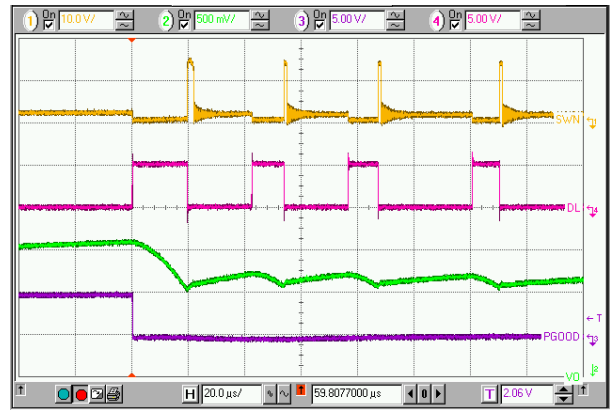
8. Hence, all the current sense components Rs1, Rs2, Cs had been found for target  $I_{ocp\_DC}$ .
9. If Rs2 is not used (open), set  $k = 1$ , at that moment, the  $I_{pk}$  will be restricted by:

$$I_{pk} = \frac{V_{octh}}{DCR} \quad (eq. 8)$$

**Overvoltage Protection (OVP)**

When  $V_{FB}$  voltage is above  $OVP_{th+}$  of the nominal  $V_{FB}$  voltage for over 1.5  $\mu s$  blanking time, an OV fault is set. At that moment, the top gate drive is turned off and the bottom gate drive is turned on until the  $V_{FB}$  below lower under voltage (UV) threshold and bottom gate drive is turned on again whenever  $V_{FB}$  goes above upper UV threshold. EN resets or power recycle the device can exit the fault. The

following diagram shows the typical waveform when OVP event occurs.

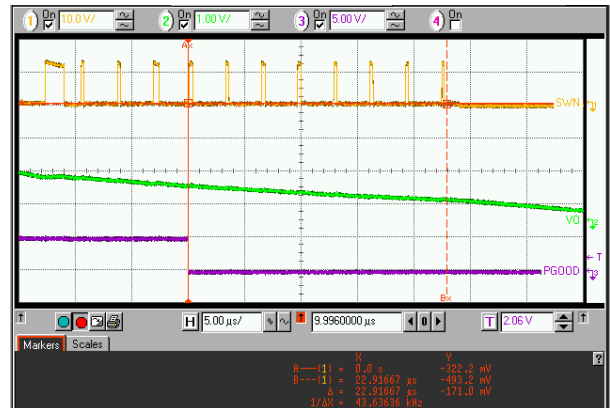


Top to Bottom : SWN, DL, Vo, PGOOD

**Figure 25. Overvoltage Protection**

**Undervoltage Protection (UVP)**

An UVP circuit monitors the  $V_{FB}$  voltage to detect under voltage event. The under voltage limit is 80% (typical) of the nominal  $V_{FB}$  voltage. If the  $V_{FB}$  voltage is below this threshold over consecutive 8 clock cycles, an UV fault is set and the device is latched off such that both top and bottom gate drives are off. EN resets or power recycle the device can exit the fault.



Top to Bottom : SWN, Vo, PGOOD

**Figure 26. Undervoltage Protection**

**Thermal Shutdown**

The IC will shutdown if the die temperature exceeds 150°C. The IC restarts operation only after the junction temperature drops below 125°C.

# NCP81045

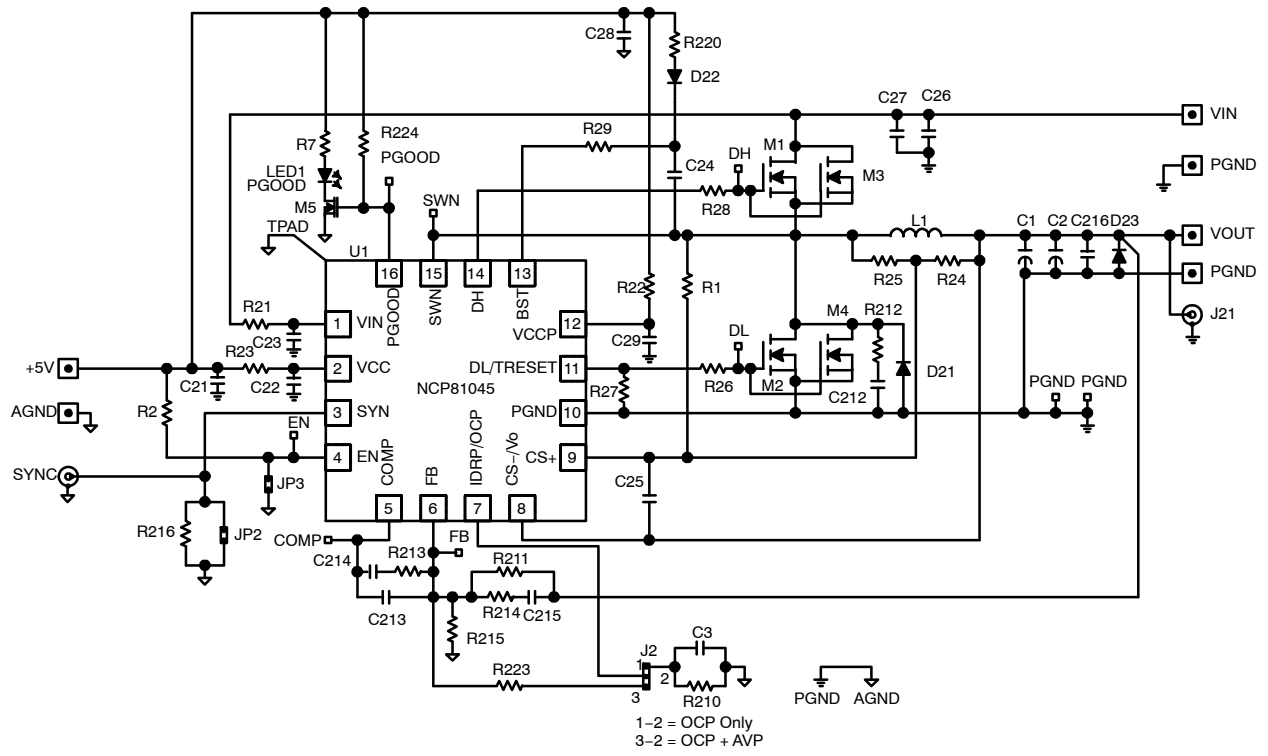
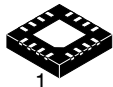
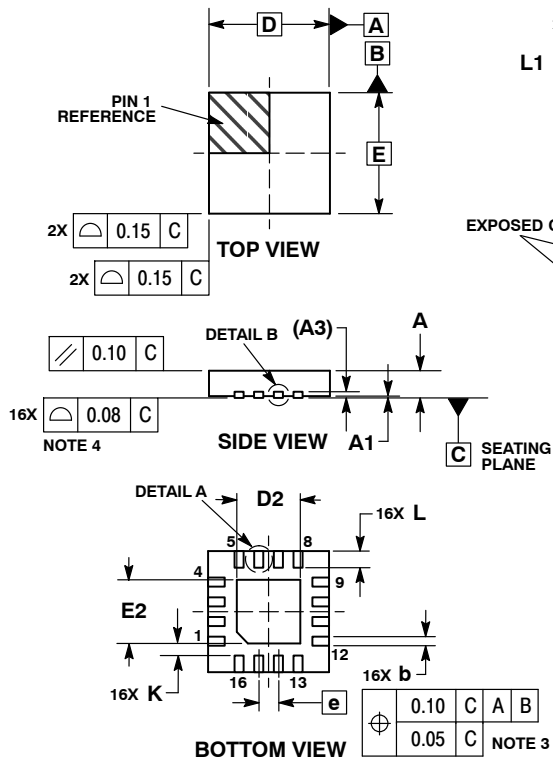


Figure 27. Demo Board Schematic





SCALE 2:1



**QFN16 4x4, 0.65P**  
CASE 485AP-01  
ISSUE A

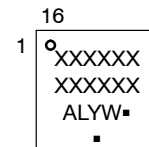
DATE 20 MAY 2009

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.25	0.35
D	4.00	BSC
D2	2.00	2.20
E	4.00	BSC
E2	2.00	2.20
e	0.65	BSC
K	0.20	---
L	0.45	0.65
L1	---	0.15

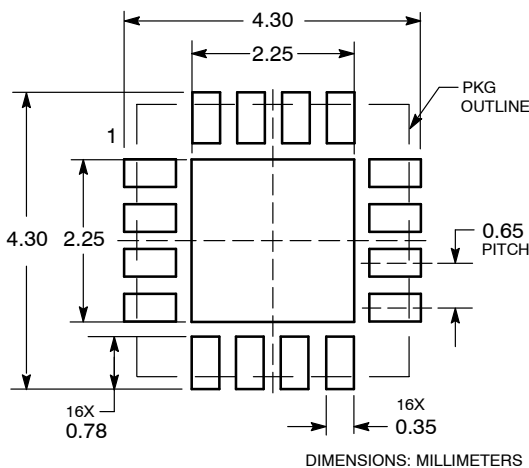
**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

**MOUNTING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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