NCP6133

Advance Information

Dual Output 1/2/3 Phase +1/0 Phase Controller with Single SVID Interface for Desktop and Notebook CPU Applications

The NCP6133 dual output 1/2/3 phase plus 1/0 buck solution is optimized for Intel VR12 compatible CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed-forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook applications. The control system is based on Dual–Edge pulse–width modulation (PWM) combined with DCR current sensing providing the fastest initial response to dynamic load events and reduced system cost. It also sheds to single phase during light load operation and can auto frequency scale in light load while maintaining excellent transient performance.

Dual high performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed–loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.

Features

- Meets Intel VR12/IMVP7 Specifications
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- Dual High Performance Operational Error Amplifier
- One Digital Soft Start Ramp for Both Rails
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- DAC with Droop Feed–forward Injection
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase–to–Phase Dynamic Current Balancing
- “Lossless” DCR Current Sensing for Current Balancing
- Summed Thermally Compensated Inductor Current Sensing for Droop
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 200 kHz – 1.0 MHz
- Startup into Pre–Charged Loads While Avoiding False OVP
- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Pin Programming for Internal SVID Parameters
- Over Voltage Protection (OVP) and Under Voltage Protection (UV)
- Over Current Protection (OCP)
- Dual Power Good Output with Internal Delays
- These Devices are Pb–Free and are RoHS Compliant

Applications

- Desktop & Notebook Processors
- Server Processors and Memory Power

This document contains information on a new product. Specifications and information herein are subject to change without notice.
Figure 1. Block Diagram
### NCP6133 QFN52 SINGLE ROW PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VSP</td>
<td>Non–inverting input to the core differential remote sense amplifier.</td>
</tr>
<tr>
<td>2</td>
<td>TSENSE</td>
<td>Temp Sense input for the multiphase converter</td>
</tr>
<tr>
<td>3</td>
<td>VR_HOT#</td>
<td>Thermal logic output for over temperature.</td>
</tr>
<tr>
<td>4</td>
<td>SDIO</td>
<td>Serial VID data interface.</td>
</tr>
<tr>
<td>5</td>
<td>SCLK</td>
<td>Serial VID clock.</td>
</tr>
<tr>
<td>6</td>
<td>ALERT#</td>
<td>Serial VID ALERT#.</td>
</tr>
<tr>
<td>7</td>
<td>VR_RDY</td>
<td>Open drain output. High indicates that the core output is regulating.</td>
</tr>
<tr>
<td>8</td>
<td>VR_RDYA</td>
<td>Open drain output. High indicates that the aux output is regulating.</td>
</tr>
<tr>
<td>9</td>
<td>ENABLE</td>
<td>Logic input. Logic high enables both outputs and logic low disables both outputs.</td>
</tr>
<tr>
<td>10</td>
<td>VCC</td>
<td>Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground.</td>
</tr>
<tr>
<td>11</td>
<td>ROSC</td>
<td>A resistance from this pin to ground programs the oscillator frequency. This pin supplies a trimmed output voltage of 2 V.</td>
</tr>
<tr>
<td>12</td>
<td>VRMP</td>
<td>Feed–forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control the ramp of PWM slope</td>
</tr>
<tr>
<td>13</td>
<td>TSENSEA</td>
<td>Temp Sense input for the single phase converter</td>
</tr>
<tr>
<td>14</td>
<td>VSPA</td>
<td>Inverting input to the aux differential remote sense amplifier</td>
</tr>
<tr>
<td>15</td>
<td>VSP</td>
<td>Non–inverting input to the aux differential remote sense amplifier</td>
</tr>
</tbody>
</table>

![Figure 2. Pinout (Top View)](image-url)
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>FBA</td>
<td>Error amplifier voltage feedback for aux output</td>
</tr>
<tr>
<td>17</td>
<td>DIFFOUTA</td>
<td>Output of the aux differential remote sense amplifier</td>
</tr>
<tr>
<td>18</td>
<td>TRBSTA</td>
<td>Compensation pin for aux rail load transient boost.</td>
</tr>
<tr>
<td>19</td>
<td>COMPA</td>
<td>Output of the aux error amplifier and the inverting input of the PWM comparator for aux output</td>
</tr>
<tr>
<td>20</td>
<td>ILIMA</td>
<td>Over current shutdown threshold setting for aux output. A resistor to CSCOMPA sets the threshold.</td>
</tr>
<tr>
<td>21</td>
<td>DROOPA</td>
<td>Used to program droop function for aux output. It's connected to the resistor divider placed between CSCOMPA and CSREFA.</td>
</tr>
<tr>
<td>22</td>
<td>CSCOMPA</td>
<td>Output of total current sense amplifier for aux output</td>
</tr>
<tr>
<td>23</td>
<td>IOUTA</td>
<td>Total output current monitor for aux output</td>
</tr>
<tr>
<td>24</td>
<td>CSSUMA</td>
<td>Inverting input of total current sense amplifier for aux output</td>
</tr>
<tr>
<td>25</td>
<td>CSPA</td>
<td>Non−Inverting input to aux current sense amplifier</td>
</tr>
<tr>
<td>26</td>
<td>CSNA</td>
<td>Inverting input to aux current sense amplifier</td>
</tr>
<tr>
<td>27</td>
<td>VBOOTA</td>
<td>VBOOTA Voltage input pin. Set to adjust the aux boot−up voltage</td>
</tr>
<tr>
<td>28</td>
<td>PWMA / IMAXA</td>
<td>Aux PWM output to gate driver. Also as ICC_MAXA input pin for aux rail. During start up it is used to program ICC_MAXA with a resistor to ground</td>
</tr>
<tr>
<td>29</td>
<td>IMAX</td>
<td>ICC_MAX Input Pin for core rail. During start up it is used to program ICC_MAX with a resistor to ground</td>
</tr>
<tr>
<td>30</td>
<td>PWM2</td>
<td>Phase 2 PWM output only. Pull to VCC will configure as 2−phase operation.</td>
</tr>
<tr>
<td>31</td>
<td>PWM3 / VBOOT</td>
<td>Phase 3 PWM output. Also as VBOOT input pin to adjust the core rail boot−up voltage. During start up it is used to program VBOOT with a resistor to ground.</td>
</tr>
<tr>
<td>32</td>
<td>PWM1 / ADDR</td>
<td>Phase 1 PWM output. Also as Address program pin. A resistor to ground on this pin programs the SVID address of the device.</td>
</tr>
<tr>
<td>33</td>
<td>DRON</td>
<td>Bidirectional gate drive enable for core output.</td>
</tr>
<tr>
<td>34</td>
<td>CSP1</td>
<td>Non−inverting input to current balance sense amplifier for phase 1</td>
</tr>
<tr>
<td>35</td>
<td>CSN1</td>
<td>Inverting input to current balance sense amplifier for phase 1</td>
</tr>
<tr>
<td>36</td>
<td>CSP3</td>
<td>Non−inverting input to current balance sense amplifier for phase 3</td>
</tr>
<tr>
<td>37</td>
<td>CSN3</td>
<td>Inverting input to current balance sense amplifier for phase 3</td>
</tr>
<tr>
<td>38</td>
<td>CSP2</td>
<td>Non−inverting input to current balance sense amplifier for phase 2</td>
</tr>
<tr>
<td>39</td>
<td>CSN2</td>
<td>Inverting input to current balance sense amplifier for phase 2</td>
</tr>
<tr>
<td>40</td>
<td>SPHN</td>
<td>Core rail single phase or multiphase selection, need to be tied to either VCC or ground</td>
</tr>
<tr>
<td>41</td>
<td>SPHP</td>
<td>Core rail single phase or multiphase selection, need to be tied to either VCC or ground</td>
</tr>
<tr>
<td>42</td>
<td>CSREF</td>
<td>Total output current sense amplifier reference voltage input.</td>
</tr>
<tr>
<td>43</td>
<td>IOUT</td>
<td>Total output current monitor for core output</td>
</tr>
<tr>
<td>44</td>
<td>CSSUM</td>
<td>Inverting input of total current sense amplifier for core output</td>
</tr>
<tr>
<td>45</td>
<td>CSCOMP</td>
<td>Output of total current sense amplifier for core output</td>
</tr>
<tr>
<td>46</td>
<td>DROOP</td>
<td>Used to program droop function for core output. It's connected to the resistor divider placed between CSCOMPA and CSREF summing node.</td>
</tr>
<tr>
<td>47</td>
<td>ILIM</td>
<td>Over current shutdown threshold setting for core output. Resistor to CSCOMPA to set threshold.</td>
</tr>
<tr>
<td>48</td>
<td>COMP</td>
<td>Output of the error amplifier and the inverting inputs of the PWM comparators for the core output.</td>
</tr>
<tr>
<td>49</td>
<td>FB</td>
<td>Error amplifier voltage feedback for core output</td>
</tr>
<tr>
<td>50</td>
<td>TRBST</td>
<td>Compensation pin for core rail load transient boost.</td>
</tr>
<tr>
<td>51</td>
<td>VSN</td>
<td>Inverting input to the core differential remote sense amplifier.</td>
</tr>
<tr>
<td>52</td>
<td>DIFFOUT</td>
<td>Output of the core differential remote sense amplifier.</td>
</tr>
<tr>
<td>53</td>
<td>FLAG / GND</td>
<td>Power supply return (QFN Flag)</td>
</tr>
</tbody>
</table>
Figure 3. NCP6133 VCCP and GT Regulator
## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Pin Symbol</th>
<th>$V_{\text{MAX}}$</th>
<th>$V_{\text{MIN}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP, COMPA</td>
<td>$V_{\text{CC}} + 0.3 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>CSCOMP, CSCOMPA</td>
<td>$V_{\text{CC}} + 0.3 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>VSN</td>
<td>$\text{GND} + 300 \text{ mV}$</td>
<td>$\text{GND} - 300 \text{ mV}$</td>
</tr>
<tr>
<td>DIFFOUT, DIFFOUTA</td>
<td>$V_{\text{CC}} + 0.3 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>VR_RDY, VR_RDYA</td>
<td>$V_{\text{CC}} + 0.3 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>VCC</td>
<td>$6.5 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>ROSC</td>
<td>$V_{\text{CC}} + 0.3 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>IO_OUT, IO_OUTA</td>
<td>$2.0 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>VRMP</td>
<td>$+25 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
<tr>
<td>All Other Pins</td>
<td>$V_{\text{CC}} + 0.3 \text{ V}$</td>
<td>$-0.3 \text{ V}$</td>
</tr>
</tbody>
</table>

*All signals referenced to GND unless noted otherwise.

## THERMAL INFORMATION

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Characteristic – QFN Package, (Note 1)</td>
<td>$R_{\text{JUA}}$</td>
<td>68</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature Range, (Note 2)</td>
<td>$T_J$</td>
<td>$-10$ to $125$</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td></td>
<td>$-10$ to $100$</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Storage Temperature Range</td>
<td>$T_{\text{STG}}$</td>
<td>$-40$ to $+150$</td>
<td>°C</td>
</tr>
<tr>
<td>Moisture Sensitivity Level – QFN Package</td>
<td>MSL</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*The maximum package power dissipation must be observed.

1. JESD 51–5 (1S2P Direct–Attach Method) with 0 LFM
2. JESD 51–7 (1S2P Direct–Attach Method) with 0 LFM

## NCP6133 ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $-10^\circ \text{C} < T_A < 100^\circ \text{C}$; $V_{\text{CC}} = 5 \text{ V}$; $C_{\text{VCC}} = 0.1 \mu\text{F}$

### ERROR AMPLIFIER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>@ $1.3 \text{ V}$</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Bias Current</td>
<td>$-400$</td>
<td>400</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open Loop DC Gain</td>
<td>$C_L = 20 \mu\text{F}$ to GND, $R_L = 10 \text{k}\Omega$ to GND</td>
<td>80</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open Loop Unity Gain Bandwidth</td>
<td>$C_L = 20 \mu\text{F}$ to GND, $R_L = 10 \text{k}\Omega$ to GND</td>
<td>50</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>$\Delta V_{\text{in}} = 100 \text{ mV}$, $G = 10 \text{ V/V}$, $\Delta V_{\text{out}} = 1.5 \text{ V} - 2.5 \text{ V}$, $C_L = 20 \mu\text{F}$ to GND, DC Load = $10 \text{k}\Omega$ to GND</td>
<td>20</td>
<td>V/μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Output Voltage</td>
<td>$I_{\text{SOURCE}} = 2.0 \text{ mA}$</td>
<td>3.5</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Output Voltage</td>
<td>$I_{\text{SINK}} = 2.0 \text{ mA}$</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>V</td>
</tr>
</tbody>
</table>

### DIFFERENTIAL SUMMING AMPLIFIER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VSP, VSPA, VSN, VSNA = $1.3 \text{ V}$</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Bias Current</td>
<td>$-400$</td>
<td>–</td>
<td>400</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>VSP Input Voltage Range</td>
<td>$-0.3$</td>
<td>–</td>
<td>3.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VSN Input Voltage Range</td>
<td>$-0.3$</td>
<td>–</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

3. Guaranteed by design or characterization data, not in production test.
# NCP6133 Electrical Characteristics

Unless otherwise stated: $-10^\circ C < T_A < 100^\circ C$; $V_{CC} = 5$ V; $C_{VCC} = 0.1 \mu F$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Differential Summing Amplifier</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$-3$ dB Bandwidth</td>
<td>$C_L = 20$ pF to GND, $R_L = 10$ kΩ to GND</td>
<td>21</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Closed Loop DC gain</td>
<td>$V_{S+} \text{ to } V_{S-} = 0.5 \text{ to } 1.3$ V</td>
<td>1.0</td>
<td>V/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Droop Accuracy</td>
<td>$CSREF - DROOP = 80$ mV DAC = 0.8 V to 1.2 V</td>
<td>$-81.5$</td>
<td>$-78.5$</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>Current Summing Amplifier</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage ($V_{os}$) (Note 3)</td>
<td>$-10^\circ C &lt; T_A &lt; 85^\circ C$</td>
<td>$-500$</td>
<td>$500$</td>
<td>μV</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$CSSUM = CSSUMA = 1$ V</td>
<td>$-7.5$</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Open Loop Gain</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>80 dB</td>
</tr>
<tr>
<td>Current Sense Unity Gain Bandwidth</td>
<td>$C_I = 20$ pF to GND, $R_L = 10$ kΩ to GND</td>
<td>10</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum CSCOMP (A) Output Voltage</td>
<td>$I_{source} = 2$ mA $CSSUM(A) = CSCOMP(A)$</td>
<td>3.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Minimum CSCOMP(A) Output Voltage</td>
<td>$I_{sink} = 2$ mA $CSSUM(A) = CSCOMP(A)$</td>
<td></td>
<td></td>
<td>0.35 V</td>
<td></td>
</tr>
<tr>
<td><strong>Current Balance Amplifier</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$CSP_{1,-3} = CSN_{1,-3} = 1.2$ V $CSPA = CSNA = 1.2$ V</td>
<td>$-50$</td>
<td>$50$</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Common Mode Input Voltage Range</td>
<td>$CSPx = CSNx$</td>
<td>0</td>
<td>2.0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Mode Input Voltage Range</td>
<td>$CSNx = 1.2$ V</td>
<td>$-100$</td>
<td>100 mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage Matching</td>
<td>$CSPx = CSNx = 1.2$ V, Measured from the average $-10^\circ C &lt; T_A &lt; 85^\circ C$</td>
<td>$-1.5$</td>
<td>1.5</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Current Sense Amplifier Gain</td>
<td>$0$ V &lt; $CSPx – CSNx$ &lt; 0.1 V</td>
<td>$5.6$</td>
<td>$6.0$</td>
<td>$6.4$</td>
<td>V/V</td>
</tr>
<tr>
<td>Multiphase Current Sense Gain Matching</td>
<td>$10$ mV &lt; $CSNx = CSPx &lt; 30$ mV</td>
<td>$-3$</td>
<td>3</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$-3$ dB Bandwidth</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8 MHz</td>
</tr>
<tr>
<td><strong>Input Supply</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.75</td>
</tr>
<tr>
<td>VCC Quiescent Current</td>
<td>$EN = \text{high}$</td>
<td>28</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EN = \text{low}$</td>
<td>0.01</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>UVLO Threshold</td>
<td>$V_{CC \text{ rising}}$</td>
<td>4.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{CC \text{ falling}}$</td>
<td>4.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC UVLO Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>80</td>
</tr>
<tr>
<td><strong>DAC Slew Rate</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft Start Slew Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
</tr>
<tr>
<td>Slew Rate Slow</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>Slew Rate Fast</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>AUX Soft Start Slew Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
</tr>
<tr>
<td>AUX Slew Rate Slow</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
</tr>
<tr>
<td>AUX Slew Rate Fast</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td><strong>Enable Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable High Input Leakage Current</td>
<td>External 1 K pull–up to 3.3 V</td>
<td>–</td>
<td>1.0</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Upper Threshold</td>
<td>$V_{UPPER}$</td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

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## NCP6133 ELECTRICAL CHARACTERISTICS

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### ENABLE INPUT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower Threshold</td>
<td>$V_{LOWER}$</td>
<td>0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Hysteresis</td>
<td>$V_{UPPER} - V_{LOWER}$</td>
<td>90</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable Delay Time</td>
<td>Measure time from Enable transitioning HI to when DRON goes high, $V_{BOOT}$ is not 0 V</td>
<td>5.0</td>
<td>ms</td>
<td></td>
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### DRVON

<table>
<thead>
<tr>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage</td>
<td>Sourcing 500 $\mu$A</td>
<td>3.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>Sinking 500 $\mu$A</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input High Threshold</td>
<td></td>
<td>2.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Threshold</td>
<td></td>
<td>1.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise/Fall Time</td>
<td>$C_L\ (PCB) = 20 \mu\text{F, } \Delta V_0 = 10%$ to 90%</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Internal Pull Down Resistance</td>
<td>$EN = Low$</td>
<td>70</td>
<td>kΩ</td>
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### IOOUT / IOOUTA OUTPUT

<table>
<thead>
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<th>Parameter</th>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Referred Offset Voltage</td>
<td>$I_{limit}$ to CSREF</td>
<td>$-1.5$</td>
<td>mV</td>
<td>$1.5$</td>
<td></td>
</tr>
<tr>
<td>Output Source Current</td>
<td>$I_{limit}$ source current = 80 $\mu$A</td>
<td>820</td>
<td>$\mu$A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Gain</td>
<td>$(I_{OUTCURRENT})/(I_{LIMITCURRENT}), R_{ILIM} = 20 \text{ k}, R_{IOUT} = 5.0 \text{ k}, DAC = 0.8 \text{ V}, 1.25 \text{ V}, 1.52 \text{ V}$</td>
<td>9.5</td>
<td>10</td>
<td>10.5</td>
<td></td>
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</tbody>
</table>

### OSCILLATOR

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Switching Frequency Range</td>
<td></td>
<td>200</td>
<td>–</td>
<td>1000</td>
<td>kHz</td>
</tr>
<tr>
<td>3 Phase Operation</td>
<td>$R_T = 6.98 \text{ k}$</td>
<td>315</td>
<td>350</td>
<td>385</td>
<td>kHz</td>
</tr>
<tr>
<td>Rosc Output Voltage</td>
<td>$R_T = 6.98 \text{ k}$</td>
<td>1.95</td>
<td>2.00</td>
<td>2.05</td>
<td>V</td>
</tr>
</tbody>
</table>

### OUTPUT OVER VOLTAGE AND UNDER VOLTAGE PROTECTION (OVP & UVP)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absolute Over Voltage Threshold During Soft Start</td>
<td>CSREF, CSNA</td>
<td>1.9</td>
<td>2.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Over Voltage Threshold Above DAC</td>
<td>$V_{SP}(A)$ rising, DAC = 1.2 V and 1.52 V</td>
<td>170</td>
<td>300</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Over Voltage Delay</td>
<td>$V_{SP}(A)$ rising to PWMx low</td>
<td>40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Under Voltage Threshold Below DAC</td>
<td>$V_{SP}(A)$ falling, (DAC = 1.2 V and 1.52 V)</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td>Under–voltage Delay</td>
<td></td>
<td>5</td>
<td>$\mu$s</td>
<td></td>
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</table>

### VR12 DAC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Voltage Accuracy</td>
<td>$1.0 \text{ V} &lt; DAC &lt; 1.52 \text{ V}$</td>
<td>$-0.5$</td>
<td>$-5$</td>
<td>$%$</td>
<td>$0.5$</td>
</tr>
<tr>
<td>Droop Feed–Forward Up Current</td>
<td>$0.8 \text{ V} &lt; DAC &lt; 0.995 \text{ V}$</td>
<td>$-0.5$</td>
<td>$-5$</td>
<td>$%$</td>
<td>$0.5$</td>
</tr>
<tr>
<td>Droop Feed–Forward Down current</td>
<td>$0.25 \text{ V} &lt; DAC &lt; 0.795 \text{ V}$</td>
<td>$-8$</td>
<td>$-8$</td>
<td>$%$</td>
<td>$0.5$</td>
</tr>
<tr>
<td>Droop Feed–Forward Pulse On–Time</td>
<td>Measured on DROOP, DROOPA</td>
<td>55</td>
<td>19</td>
<td>65</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>Measured on DROOP, DROPA</td>
<td>19</td>
<td>55</td>
<td>25</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.16</td>
<td>$\mu$s</td>
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### OVERCURRENT PROTECTION (Core Rail)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILIM Threshold Current (OCP shutdown after 50 $\mu$s delay)</td>
<td>$(PS0) R_{lim} = 20k$</td>
<td>9.0</td>
<td>10</td>
<td>11.0</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>ILIM Threshold Current (immediate OCP shutdown)</td>
<td>$(PS0) R_{lim} = 20k$</td>
<td>13.5</td>
<td>15</td>
<td>16.5</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>ILIM Threshold Current (OCP shutdown after 50 $\mu$s delay)</td>
<td>$(PS1, PS2, PS3) R_{lim} = 20k, N =$ number of phases in PS0 mode</td>
<td>10/N</td>
<td>$\mu$A</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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### NCP6133 ELECTRICAL CHARACTERISTICS

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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OVERCURRENT PROTECTION (Core Rail)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIM Threshold Current (immediate OCP shutdown) (PS1, PS2, PS3)</td>
<td>(R_{lim} = 20 \ k, N = ) number of phases in PS0 mode</td>
<td>15/N</td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Maximum Timer for OCP shutdown</td>
<td></td>
<td></td>
<td>55</td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td><strong>OVERCURRENT PROTECTION (+1 Rail)</strong></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ILIM Threshold Current (OCP shutdown after 50 (\mu s) delay) (PS0,1,2,3)</td>
<td>(R_{lim} = 20 \ k)</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>ILIM Threshold Current (immediate OCP shutdown) (PS0,1,2,3)</td>
<td>(R_{lim} = 20 \ k)</td>
<td>12.5</td>
<td>15</td>
<td>16.5</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Maximum Timer for OCP shutdown</td>
<td></td>
<td></td>
<td>55</td>
<td></td>
<td>(\mu s)</td>
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<tr>
<td>CSCOMP OCP Threshold</td>
<td></td>
<td></td>
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<td>220</td>
<td>(mV)</td>
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<tr>
<td><strong>VRMP (VIN Monitor)</strong></td>
<td></td>
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<tr>
<td>UVLO Threshold</td>
<td>VRMP falling</td>
<td>3.0</td>
<td>3.2</td>
<td>3.4</td>
<td>(V)</td>
</tr>
<tr>
<td>UVLO Hysteresis</td>
<td></td>
<td>600</td>
<td>800</td>
<td></td>
<td>(mV)</td>
</tr>
<tr>
<td>Leakage current</td>
<td>(V_{EN} = 0 \ V, V_{VRMP} = 26 \ V)</td>
<td></td>
<td></td>
<td>0.5</td>
<td>(\mu A)</td>
</tr>
<tr>
<td><strong>MODULATORS (PWM COMPARATORS) FOR CORE AND AUX</strong></td>
<td></td>
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</tr>
<tr>
<td>0% Duty Cycle</td>
<td>COMP voltage when the PWM outputs remain LO</td>
<td>1.3</td>
<td></td>
<td></td>
<td>(V)</td>
</tr>
<tr>
<td>100% Duty Cycle</td>
<td>COMP voltage when the PWM outputs remain HI (V_{RMP} = 12.0 \ V)</td>
<td></td>
<td>3.1</td>
<td></td>
<td>(V)</td>
</tr>
<tr>
<td>PWM Ramp Duty Cycle Matching</td>
<td>COMP = 2 (V), PWM (T_{on}) matching</td>
<td></td>
<td>1</td>
<td></td>
<td>(%)</td>
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<tr>
<td>PWM Phase Angle Error</td>
<td>Between adjacent phases</td>
<td></td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td>Ramp Feed–forward Voltage range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(V)</td>
</tr>
<tr>
<td><strong>TRBST, TRBSTA</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRBST/COMP offset</td>
<td>TRBST Starts Sinking Current</td>
<td>350</td>
<td></td>
<td></td>
<td>(mV)</td>
</tr>
<tr>
<td>TRBST Sink Capability</td>
<td></td>
<td></td>
<td>500</td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>TRBSTA/COMPA offset</td>
<td>TRBST Starts Sinking Current</td>
<td>350</td>
<td></td>
<td></td>
<td>(mV)</td>
</tr>
<tr>
<td>TRBSTA Sink Capability</td>
<td></td>
<td></td>
<td>500</td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td><strong>VR_HOT#</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>(I_{VRHOT} = -4 \ mA)</td>
<td></td>
<td></td>
<td></td>
<td>(V)</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>High Impedance State</td>
<td></td>
<td>(-1.0)</td>
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</tr>
<tr>
<td><strong>TSENSE/TSENSEA</strong></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Alert# Assert Threshold</td>
<td></td>
<td></td>
<td>497</td>
<td></td>
<td>(mV)</td>
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<tr>
<td>Alert# De–assert Threshold</td>
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<td>512</td>
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<td>(mV)</td>
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<td>VRHOT Assert Threshold</td>
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<td>477</td>
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<td>(mV)</td>
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<td>VRHOT Rising Threshold</td>
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<td></td>
<td>491</td>
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<td>(mV)</td>
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<td>TSENSE Bias Current</td>
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<td>114</td>
<td>120</td>
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<td><strong>ADC</strong></td>
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<tr>
<td>Voltage Range</td>
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<td>0</td>
<td>2</td>
<td>(V)</td>
</tr>
<tr>
<td>Total Unadjusted Error (TUE)</td>
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<td></td>
<td></td>
<td>(%)</td>
</tr>
<tr>
<td>Differential Nonlinearity (DNL)</td>
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<td>8–bit (%)</td>
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<tr>
<td>Power Supply Sensitivity</td>
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<td></td>
<td></td>
<td></td>
<td>±1 (%)</td>
</tr>
<tr>
<td>Conversion Time</td>
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<td></td>
<td></td>
<td>30</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Round Robin</td>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output Low Saturation Voltage</strong></td>
<td>$I_{VR_RDY(A)} = 4 \text{ mA}$</td>
<td>–</td>
<td>–</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td><strong>Rise Time</strong></td>
<td>External pull–up of 1 kΩ to 3.3 V, $C_{TOT} = 45 \mu \text{F, } \Delta V_o = 10% \text{ to } 90%$</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Fall Time</strong></td>
<td>External pull–up of 1 kΩ to 3.3 V, $C_{TOT} = 45 \mu \text{F, } \Delta V_o = 90% \text{ to } 10%$</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Output Voltage at Power–up</strong></td>
<td>$V_{CC} \text{ via } 2 k\Omega$</td>
<td>–</td>
<td>–</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td><strong>Output Leakage Current When High</strong></td>
<td>$V_{VR_RDY} \text{ and } V_{VR_RDYA} = 5.0 \text{ V}$</td>
<td>–</td>
<td>–</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td><strong>VR_RDY Delay (rising)</strong></td>
<td>$DAC = \text{TARG} \text{ E} \text{T} \text{ A} \text{ R} \text{ D} \text{ Y}$</td>
<td>500</td>
<td>–</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td><strong>VR_RDY Delay (falling)</strong></td>
<td>From OCP or OVP</td>
<td>–</td>
<td>5</td>
<td>–</td>
<td>μs</td>
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### PWM OUTPUTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output High Voltage</strong></td>
<td>Sourcing 500 μA</td>
<td>$V_{CC} - 0.2 \text{ V}$</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td><strong>Output Mid Voltage</strong></td>
<td>No Load, SetPS = 02</td>
<td>1.9</td>
<td>2.0</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td><strong>Output Low Voltage</strong></td>
<td>Sinking 500 μA</td>
<td>–</td>
<td>–</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td><strong>Rise and Fall Time</strong></td>
<td>$CL (\text{PCB}) = 50 \mu \text{F, } \Delta V_o = \text{GND to } V_{CC}$</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td><strong>PWM Pin Source Current</strong></td>
<td>100</td>
<td>μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PWM Pin Threshold Voltage</strong></td>
<td>3.3</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Phase Detect Timer</strong></td>
<td>20</td>
<td>μs</td>
<td></td>
<td></td>
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### 2/3 PHASE DETECTION

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### IMAXA, ADDR, VBOOT INPUTS

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### SPHP/SPHN (TO SELECT 1 PHASE MODE)

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### SCLK, SDIO, ALERT#

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3. Guaranteed by design or characterization data, not in production test.
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Table 1. VR12 VID CODES

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<td>Error AMP Comp(A) Pin</td>
<td>OVP(A) and UVP(A)</td>
<td>DRVON Pin</td>
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<td>Low</td>
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<td>Start up Delay &amp; Calibration</td>
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<td>DRVON Fault</td>
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<td>Resitive pull up</td>
<td>Driver must release DRVON to high</td>
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<td>Soft Start</td>
<td>Low</td>
<td>Operational</td>
<td>Active / No latch</td>
<td>High</td>
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<tr>
<td>EN &gt; threshold UVLO &gt; threshold DRVON &gt; High</td>
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<td>Normal Operation</td>
<td>High</td>
<td>Operational</td>
<td>Active / Latching</td>
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<td>N/A</td>
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<tr>
<td>Over Voltage</td>
<td>Low</td>
<td>N/A</td>
<td>DAC + 150 mV</td>
<td>High</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Over Current</td>
<td>Low</td>
<td>Operational</td>
<td>Last DAC Code</td>
<td>Low</td>
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<td>VID Code = 00h</td>
<td>Low: if Reg34h:bit0 = 0; High: if Reg34h:bit0 = 1</td>
<td>Clamped to 0.9 V</td>
<td>Disabled</td>
<td>High, PWM outputs in low state</td>
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</table>
Controller POR

VCC > UVLO

VCC < UVLO

Enable

EN = 0

EN = 1

 Disable

 Calibrate

 Drive Off

 Soft Start Ramp

 OVP

 VS > OVP

 VS > OVP

 VCC > UVLO and DRON HIGH

 3.5 ms and CAL DONE

 Phase Detect

 VCCP > UVLO and DRON HIGH

 Soft Start Ramp

 DAC = Vboot

 DAC = VID

 Normal VR_RDY

 VR_RDY

 VS > UVP

 VS < UVP

 UVP

 NO_CPU

 INVALID VID

 DAC = VID

 VDRP > ILIM
 NO_CPU

 VS > UVP

 VS < UVP

 Figure 6. State Diagram
General

The NCP6133 is a dual output one/two/three phases plus one phase dual edge modulated multiphase PWM controller designed to meet the Intel VR12 specifications with a serial SVID control interface. The NCP6133 implements PS0, PS1, PS2 and PS3 power saving states. It is designed to work in notebook, desktop, and server applications.

For Core Rail:

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<th>Power Status</th>
<th>PWM Output Operating Mode</th>
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<td>PS0</td>
<td>Multi-phase PWM interleaving output</td>
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<tr>
<td>PS1</td>
<td>Single-phase COT CCM mode (PWM1 only, PWM2–3 stay in Mid)</td>
</tr>
<tr>
<td>PS2</td>
<td>Single-phase COT DCM mode (PWM1 only, PWM2–3 stay in Mid)</td>
</tr>
<tr>
<td>PS3</td>
<td>Single-phase COT DCM mode (PWM1 only, PWM2–3 stay in Mid)</td>
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For AUX Rail:

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<th>PWM Output Operating Mode</th>
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<td>PWM interleaving with Core Rail / COT CCM mode</td>
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<tr>
<td>PS1</td>
<td>PWM interleaving with Core Rail / COT CCM mode</td>
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<tr>
<td>PS2</td>
<td>Single-phase COT DCM mode</td>
</tr>
<tr>
<td>PS3</td>
<td>Single-phase COT DCM mode</td>
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</table>

VID code change is supported by SVID interface with three options as below:

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<th>Option</th>
<th>SVID Command Code</th>
<th>Feature</th>
<th>Register Address</th>
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</thead>
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<tr>
<td>SetVID_Fast</td>
<td>01h</td>
<td>&gt; 10 mV/µs VID code change slew rate</td>
<td>24h</td>
</tr>
<tr>
<td>SetVID_Slow</td>
<td>02h</td>
<td>= 1/4 of SetVID_Fast VID code change slew rate</td>
<td>25h</td>
</tr>
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<td>SetVID_Decay</td>
<td>03h</td>
<td>No control, VID code down</td>
<td>N/A</td>
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Serial VID

The NCP6133 supports the Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). The table of supported registers is shown below.

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<th>Name</th>
<th>Description</th>
<th>Access</th>
<th>Default</th>
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<td>00h</td>
<td>Vendor ID</td>
<td>Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah</td>
<td>R</td>
<td>0x1Ah</td>
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<tr>
<td>01h</td>
<td>Product ID</td>
<td>Uniquely identifies the VR product. The VR vendor assigns this number.</td>
<td>R</td>
<td>0x51</td>
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<tr>
<td>02h</td>
<td>Product Revision</td>
<td>Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.</td>
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<td>05h</td>
<td>Protocol ID</td>
<td>Identifies the SVID Protocol the controller supports</td>
<td>R</td>
<td>0x01</td>
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<td>06h</td>
<td>Capability</td>
<td>Informs the Master of the controller’s Capabilities. 1 = supported, 0 = not supported Bit 7 = lout_format. Bit 7 = 0 when 1A = 1LSB of Reg 15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1 Bit 6 = ADC Measurement of Temp Supported = 1 Bit 5 = ADC Measurement of Pin Supported = 0 Bit 4 = ADC Measurement of Vin Supported = 0 Bit 3 = ADC Measurement of In supported = 0 Bit 2 = ADC Measurement of Pout Supported = 1 Bit 1 = ADC Measurement of Vout Supported = 1 Bit 0 = ADC Measurement of Iout Supported = 1</td>
<td>R</td>
<td>0xC7</td>
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<td>Generic ID</td>
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<td>51h or 31h</td>
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<td>10h</td>
<td>Status_1</td>
<td>Data register read after the ALERT# signal is asserted. Conveying the status of the VR.</td>
<td>R</td>
<td>00h</td>
</tr>
<tr>
<td>Index</td>
<td>Name</td>
<td>Description</td>
<td>Access</td>
<td>Default</td>
</tr>
<tr>
<td>-------</td>
<td>------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>--------</td>
<td>---------</td>
</tr>
<tr>
<td>11h</td>
<td>Status_2</td>
<td>Data register showing optional status_2 data.</td>
<td>R</td>
<td>00h</td>
</tr>
<tr>
<td>12h</td>
<td>Temp zone</td>
<td>Data register showing temperature zones the system is operating in</td>
<td>R</td>
<td>00h</td>
</tr>
<tr>
<td>15h</td>
<td>I_out</td>
<td>8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max</td>
<td>R</td>
<td>01h</td>
</tr>
<tr>
<td>16h</td>
<td>V_out</td>
<td>8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8 mV</td>
<td>R</td>
<td>01h</td>
</tr>
<tr>
<td>17h</td>
<td>VR_Temp</td>
<td>8 bit binary word ADC of voltage. Binary format in deg C, IE 100°C = 64h. A value of 00h indicates this function is not supported</td>
<td>R</td>
<td>01h</td>
</tr>
<tr>
<td>18h</td>
<td>P_out</td>
<td>8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported</td>
<td>R</td>
<td>01h</td>
</tr>
<tr>
<td>1Ch</td>
<td>Status 2</td>
<td>When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.</td>
<td>R</td>
<td>00h</td>
</tr>
<tr>
<td>21h</td>
<td>Icc_Max</td>
<td>Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.</td>
<td>R</td>
<td>00h</td>
</tr>
<tr>
<td>22h</td>
<td>Temp_Max</td>
<td>Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and programmable over the SVID Interface</td>
<td>R/W</td>
<td>64h</td>
</tr>
<tr>
<td>24h</td>
<td>SR_fast</td>
<td>Slew Rate for SetVID_fast commands. Binary format in mV/μs.</td>
<td>R</td>
<td>0Ah</td>
</tr>
<tr>
<td>25h</td>
<td>SR_slow</td>
<td>Slew Rate for SetVID_slow commands. It is 4X slower than the SR_fast rate. Binary format in mV/μs</td>
<td>R</td>
<td>02h</td>
</tr>
<tr>
<td>26h</td>
<td>Vboot</td>
<td>The Vboot is programmed using resistors on the Vboot pin which is sensed on power up. The controller will ramp to Vboot and hold at Vboot until it receives a new SVID SetVID command to move to a different voltage.</td>
<td>R</td>
<td>00h</td>
</tr>
<tr>
<td>30h</td>
<td>Vout_Max</td>
<td>Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. VR 12 VID format.</td>
<td>RW</td>
<td>FBh</td>
</tr>
<tr>
<td>31h</td>
<td>VID setting</td>
<td>Data register containing currently programmed VID voltage. VID data format.</td>
<td>RW</td>
<td>00h</td>
</tr>
<tr>
<td>32h</td>
<td>Pwr State</td>
<td>Register containing the current programmed power state.</td>
<td>RW</td>
<td>00h</td>
</tr>
<tr>
<td>33h</td>
<td>Offset</td>
<td>Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0 = positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement. 00h = no margin 01h = +1 VID step 02h = +2 VID steps FFh = -1 VID step FEh = -2 VID steps.</td>
<td>RW</td>
<td>00h</td>
</tr>
<tr>
<td>34h</td>
<td>MultiVR Config</td>
<td></td>
<td>RW</td>
<td>00h</td>
</tr>
</tbody>
</table>
Boot Voltage Programming
The NCP6133 has a Vboot voltage register that can be externally programmed for each output. The VBOOTA also provides a feature that allows the “+1” single phase output to be disabled and effectively removed from the SVID bus. If the single phase output is disabled it alters the SVID address setting table to allow the multi-phase rail to show up at an even or odd address. See the Boot Voltage Table below.

Table 3. BOOT VOLTAGE TABLE

<table>
<thead>
<tr>
<th>Boot Voltage (V)</th>
<th>Resistor Value (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10k</td>
</tr>
<tr>
<td>0.9</td>
<td>25k</td>
</tr>
<tr>
<td>1.0</td>
<td>45k</td>
</tr>
<tr>
<td>1.1</td>
<td>70k</td>
</tr>
<tr>
<td>1.2</td>
<td>95k</td>
</tr>
<tr>
<td>1.35</td>
<td>125k</td>
</tr>
<tr>
<td>1.5</td>
<td>165k</td>
</tr>
</tbody>
</table>
Shutting (VBOOTA only) VBOOTA = VCC

Addressing Programming
The NCP6133 supports seven possible dual SVID device addresses and eight possible single device addresses. Pin 32 (PWM1/ADDR) is used to set the SVID address. On power up a 10 μA current is sourced from this pin through a resistor connected to this pin and the resulting voltage is measured. The two tables below provide the resistor values for each corresponding SVID address. For dual addressing follow the Dual SVID Address Table. The address value is latched at startup. If VBOOTA is pulled to VCC the aux rail will be removed from the SVID bus, the address will then follow the Single Address SVID table below.

Table 4. DUAL SVID ADDRESS TABLE

<table>
<thead>
<tr>
<th>Resistor Value</th>
<th>Main Rail SVID Address</th>
<th>Aux Rail SVID Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>10k</td>
<td>0000</td>
<td>0001</td>
</tr>
<tr>
<td>25k</td>
<td>0010</td>
<td>0011</td>
</tr>
<tr>
<td>45k</td>
<td>0100</td>
<td>0101</td>
</tr>
<tr>
<td>70k</td>
<td>0110</td>
<td>0111</td>
</tr>
<tr>
<td>95k</td>
<td>1000</td>
<td>1001</td>
</tr>
<tr>
<td>125k</td>
<td>1010</td>
<td>1011</td>
</tr>
<tr>
<td>165k</td>
<td>1100</td>
<td>1101</td>
</tr>
</tbody>
</table>

Remote Sense Amplifier
A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator’s output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to DIFFOUT:

\[
V_{\text{DIFFOUT}} = (V_{\text{VSP}} - V_{\text{VSN}}) + (1.3\text{ V} - V_{\text{DAC}}) + (V_{\text{DROOP}} - V_{\text{CSREF}}) \quad (eq. 1)
\]

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier
A high performance error amplifier is provided for high bandwidth transient performance. A standard type 3 compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers
Each phase has a low offset differential amplifier to sense that phase current for current balance and per phase OCP protection during soft-start. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for accurate current balance. Fine tuning of this time constant is generally not required.
The individual phase current is summed into the PWM comparator feedback. In this way current is balanced via a current mode control approach.

**Total Current Sense Amplifier**

The NCP6133 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR).

Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

**Programming the Current Limit**

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 mA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 mA. Set the value of the current limit resistor based on the CSCOMP − CSREF voltage as shown below.

\[ R_{\text{LIMIT}} = \frac{\text{VCSCOMP} - \text{CSREF}(\text{ILIMIT})}{10\mu} \] (eq. 5)

or

\[ R_{\text{LIMIT}} = \frac{V_{\text{CSCOMP-CSREF@ILIMIT}}}{10\mu} \] (eq. 6)

**Programming DROOP and DAC Feed−Forward Filter**

The signals DROOP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage. The total current feedback should be filtered before it is applied to the DROOP pin. This filter impedance provides DAC feed−forward during dynamic VID changes. Programming this filter can be made simpler if CSCOMP−CSREF is equal to the droop voltage. \( R_{\text{droop}} \) sets the gain of the DAC feed−forward and \( C_{\text{droop}} \) provides the time constant to cancel the time constant of the system per the following equations. \( C_{\text{out}} \) is the total output capacitance and \( R_{\text{out}} \) is the output impedance of the system.
If the Droop at maximum load is less than 100 mV at ICCMAX we recommend altering this filter into a voltage divider such that a larger signal can be provided to the ILIMIT resistor by increasing the CSCOMP amp gain for better current monitor accuracy. The DROOP pin divider gain should be set to provide a voltage from DROOP to CSREF equal to the amount of voltage droop desired in the output. A current is applied to the DROOP pin during dynamic VID. In this case Rdroop1 in parallel with Rdroop2 should be equal to Rdroop.

**Figure 9.**

**Programming IOUT**

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull–up resistor from 5 V VCC can be used to offset the IOUT signal positively if needed.

\[
R_{IOUT} = \frac{2.0 \text{ V} \times R_{LIMIT}}{10 * \frac{R_{cs2} + R_{cs1} \times Rth}{R_{th} + R_{cs1} + R_{cs2} + Rth} \times (I_{out\_ICCMAX} \times DCR)}
\]

(eq. 7)

**Figure 10.**

**Programming ICC_MAX and ICC_MAXA**

The SVID interface provides the platform ICC_MAX value at register 21h for both the multiphase and the single phase rail. A resistor to ground on the IMAX and IMAXA pins program these registers at the time the part is enabled. 10 µA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10 k.

\[
ICC\_MAX_{21h} = \frac{R \times 10 \mu A \times 256 \text{ A}}{2 \text{ V}}
\]

(eq. 8)

**Programming TSENSE and TSENSEA**

Two temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE and TSENSEA pins to generate a voltage on the temperature sense network. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100 k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.

**Figure 11.**

**Precision Oscillator**

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 200 kHz/phase to 1 MHz/phase. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

NCP6133 Operating Frequency versus Rosc:

\[
\frac{10.5 \text{ kΩ} \times 350 \text{ kHz}}{F_s} = R_{OSC}
\]

(eq. 9)
The oscillator generates triangle ramps that are 0.5 ~ 2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the signal phase rail is set half way between phases 1 and 2 of the multi phase rail for minimum input ripple current.

### Programming the Ramp Feed–Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed–forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following, 

$$ V_{RAMPPk} - p_{pp} = 0.1 \times V_{VRMP} \quad (eq. \ 10) $$

### Programming TRBST

The TRBST pin provides a signal to offset the output after load release overshoot. This network should be fine tuned during the board tuning process and is only necessary in systems with significant load release overshoot. The TRBST network allows maximum boost for low frequency load release events to minimize load release undershoot. The network time constants are set up to provide a TRBST roll off at higher frequencies where it is not needed. Cboost1 * Rbst1 controls the time constant of the load release boost. This should be set to counter the under shoot after load release. Rbst1 + Rbst2 controls the maximum amount of boost during rapid step loading. Rbst2 is generally much larger than Rbst1. The Cboost2 * Rbst2 time constant controls the roll off frequency of the TRBST function.

### PWM Comparators

During steady state operation, the duty cycle is centered on the valley of the triangle ramp waveform and both edges of the PWM signal are modulated. During a transient event the duty will increase rapidly and proportionally turning on all phases as the error amp signal increases with respect to the ramps to provide a highly linear and proportional response to the step load.

### Phase Detection Sequence

During start–up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the PWM outputs and SPHP/SPHN pin connections.

The Aux rail can be disabled by pulling the VBOOTA signal to VCC. This changes the SVID address scheme to allow the multiphase to be programmed to any SVID Address odd or even. See the register resistor programming table.

### Table 6. CORE RAIL SINGLE PHASE OR MULTIPHASE SETTINGS

<table>
<thead>
<tr>
<th>SPHP (Pin 41)</th>
<th>SPHN (Pin 40)</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>GND</td>
<td>Core rail single phase setting</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>Core rail multi–phase setting</td>
</tr>
<tr>
<td>GND</td>
<td>VCC</td>
<td>Core rail multi–phase setting</td>
</tr>
<tr>
<td>VCC</td>
<td>VCC</td>
<td>Core rail multi–phase setting</td>
</tr>
</tbody>
</table>

NOTE: SPHP/SPHN can’t be floated.
### Table 7. PHASE COUNT TABLE

<table>
<thead>
<tr>
<th>Number of Phases</th>
<th>Notes:</th>
</tr>
</thead>
<tbody>
<tr>
<td>3+1</td>
<td>PWM2 connected, VbootA programmed</td>
</tr>
<tr>
<td></td>
<td>Refer to core rail single/multi phase table for SPHP/SPHN connections</td>
</tr>
<tr>
<td>2+1</td>
<td>PWM2 tied to VCC, VbootA programmed</td>
</tr>
<tr>
<td></td>
<td>Refer to core rail single/multi phase table for SPHP/SPHN connections</td>
</tr>
<tr>
<td>3+0</td>
<td>PWM2 connected, VbootA tied to VCC</td>
</tr>
<tr>
<td></td>
<td>Refer to core rail single/multi phase table for SPHP/SPHN connections</td>
</tr>
<tr>
<td>2+0</td>
<td>PWM2 tied to VCC, VbootA tied to VCC</td>
</tr>
<tr>
<td></td>
<td>Refer to core rail single/multi phase table for SPHP/SPHN connections</td>
</tr>
<tr>
<td>1+1</td>
<td>PWM2 floated or connected to VCC, VbootA programmed</td>
</tr>
<tr>
<td></td>
<td>SPHP = VCC, SPHN = GND</td>
</tr>
</tbody>
</table>

### Table 8. 2+1 UNUSED PIN CONNECTION TABLE

<table>
<thead>
<tr>
<th>Unused Pin</th>
<th>Connect to</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM2</td>
<td>VCC</td>
</tr>
<tr>
<td>CSN2</td>
<td>GND or VCC</td>
</tr>
<tr>
<td>CSP2</td>
<td>Same as CSN2</td>
</tr>
</tbody>
</table>

### Table 9. 3+0 UNUSED PIN CONNECTION TABLE

<table>
<thead>
<tr>
<th>Unused Pin</th>
<th>Connect to</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBOOTA</td>
<td>VCC</td>
</tr>
<tr>
<td>VSPA</td>
<td>GND</td>
</tr>
<tr>
<td>VSNA</td>
<td>GND</td>
</tr>
<tr>
<td>DIFFOUTA</td>
<td>float</td>
</tr>
<tr>
<td>FBA</td>
<td>COMPA</td>
</tr>
<tr>
<td>COMPA</td>
<td>FBA</td>
</tr>
<tr>
<td>TRBSTA</td>
<td>float</td>
</tr>
<tr>
<td>CSP2</td>
<td>GND</td>
</tr>
<tr>
<td>CSN3</td>
<td>GND</td>
</tr>
<tr>
<td>CSP2</td>
<td>Same as CSN2</td>
</tr>
<tr>
<td>CSSUMA</td>
<td>CSSUMA</td>
</tr>
<tr>
<td>CSCOMPA</td>
<td>CSCOMPA</td>
</tr>
<tr>
<td>DROOPA</td>
<td>GND or CSCOMPA</td>
</tr>
<tr>
<td>IOUTA</td>
<td>GND</td>
</tr>
<tr>
<td>PWMMA</td>
<td>float</td>
</tr>
</tbody>
</table>

### Table 10. 2+0 UNUSED PIN CONNECTION TABLE

<table>
<thead>
<tr>
<th>Unused Pin</th>
<th>Connect to</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM2</td>
<td>VCC</td>
</tr>
<tr>
<td>CSN2</td>
<td>GND or VCC</td>
</tr>
<tr>
<td>CSP2</td>
<td>Same as CSN2</td>
</tr>
<tr>
<td>VBOOTA</td>
<td>VCC</td>
</tr>
<tr>
<td>VSPA</td>
<td>GND</td>
</tr>
<tr>
<td>VSNA</td>
<td>GND</td>
</tr>
<tr>
<td>DIFFOUTA</td>
<td>float</td>
</tr>
<tr>
<td>FBA</td>
<td>COMPA</td>
</tr>
<tr>
<td>COMPA</td>
<td>FBA</td>
</tr>
<tr>
<td>TRBSTA</td>
<td>float</td>
</tr>
<tr>
<td>CSP2</td>
<td>GND</td>
</tr>
<tr>
<td>CSN3</td>
<td>GND</td>
</tr>
<tr>
<td>CSSUMA</td>
<td>CSSUMA</td>
</tr>
<tr>
<td>CSCOMPA</td>
<td>CSCOMPA</td>
</tr>
<tr>
<td>DROOPA</td>
<td>GND or CSCOMPA</td>
</tr>
<tr>
<td>IOUTA</td>
<td>GND</td>
</tr>
<tr>
<td>PWMMA</td>
<td>float</td>
</tr>
</tbody>
</table>

### Table 11. 1+1 UNUSED PIN CONNECTION TABLE

<table>
<thead>
<tr>
<th>Unused Pin</th>
<th>Connect to</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM2</td>
<td>VCC</td>
</tr>
<tr>
<td>CSN2</td>
<td>GND or VCC</td>
</tr>
<tr>
<td>CSP2</td>
<td>Same as CSN2</td>
</tr>
<tr>
<td>CSN3</td>
<td>GND or VCC</td>
</tr>
<tr>
<td>CSP3</td>
<td>Same as CSN3</td>
</tr>
</tbody>
</table>
Input Under Voltage Protection

NCP6133 monitors the 5 V V_{CC} supply and the VRMP pin for under voltage protection. The gate driver monitors both the gate driver V_{CC} and the BST voltage (12 V drivers only). When the voltage on the gate driver is insufficient it will pull DRVON low and notify the controller the power is not ready. The gate driver will hold DRVON low for a minimum period of time to allow the controller to restart its start-up sequence. In this case the PWM is set back to the MID state and soft-start would begin again. See the figure below.

Over Current Latch–Off Protection

During normal operation a programmable total current limit is provided that scales with the phase count during power saving operation. The level of total current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current of 10 μA and 15 μA. If the current into the ILIM pin exceeds the 10 A level an internal latch–off counter starts. The controller shuts down if the fault is not removed after 50 μs. If the current into the pin exceeds 15 μA the controller will shut down immediately. To recover from an OCP fault the EN pin must be cycled low.

The over–current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equation:

\[ R_{ILIM} = \frac{V_{CSCOMP} - V_{CSREF}}{10 \, \mu A} \]  

(eq. 11)
Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300 mV below the DAC–DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low.

Over Voltage Protection

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If the output voltage exceeds the DAC voltage by approximately 300 mV, PWMs will be forced low until the voltage drops below the OVP threshold. After the first OVP trip the DAC will ramp down to zero to avoid a negative output voltage spike during shutdown. When the DAC gets to zero the PWMs will be forced low and the DRVON will remain high. To reset the part the Enable pin must be cycled low. During soft-start and DVID, the above OVP is disabled. This allows the controller to start up without false triggering the OVP. Meanwhile, there is a second OVP protection which is always enabled. The second OVP monitors CSREF(A) pin voltage with a protection threshold of 2.3 V.

Layout Notes

The NCP6133 has differential voltage and current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To insure proper function there are some general rules to follow. Always place the inductor current sense RC filters as close to the CSN and CSP pins on the controller as possible. Place the VCC decoupling cap as close as possible to the controller VCC pin, the resistor in series should always be no higher than 2.2 Ω to avoid large voltage drop. The high frequency filter cap on CSREF and the 10 Ω CSREF resistors should be placed close to the controller. The small high feed back cap from COMP to FB should be as close to the controller as possible. Please minimize the capacitance to ground of the FB traces by keeping them short. The filter cap from CSCOMP to CSREF should also be close to the controller.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP6133MNTWG</td>
<td>QFN52 - Single Row</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
# NCP6133

## PACKAGE DIMENSIONS

### QFN52 6x6, 0.4P

**CASE 485BE**  
**ISSUE B**

**NOTES:**
1. **DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.**
2. **CONTROLLING DIMENSIONS: MILLIMETERS.**
3. **DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP**
4. **COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.**

### MILLIMETERS

<table>
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<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
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<tbody>
<tr>
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<tr>
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<td>0.05</td>
</tr>
<tr>
<td>A3</td>
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<td>REF</td>
</tr>
<tr>
<td>b</td>
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</tr>
<tr>
<td>D</td>
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<td>BSC</td>
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<tr>
<td>D2</td>
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<td>E</td>
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<tr>
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<tr>
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</tr>
<tr>
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<tr>
<td>L</td>
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<tr>
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</tr>
<tr>
<td>L2</td>
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### DIMENSIONS: MILLIMETERS

<table>
<thead>
<tr>
<th>PKG OUTLINE</th>
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<th>DETAIL D</th>
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<tbody>
<tr>
<td>0.40</td>
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<td>0.49</td>
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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.*