NCP5183, NCV5183

High Voltage High Current
High and Low Side Driver

The NCP5183 is a High Voltage High Current Power MOSFET Driver providing two outputs for direct drive of 2 N-channel power MOSFETs arranged in a half-bridge (or any other high-side + low-side) configuration.

It uses the bootstrap technique to insure a proper drive of the High–side power switch. The driver works with 2 independent inputs to accommodate any topology (including half–bridge, asymmetrical half–bridge, active clamp and full–bridge…).

Features

• Automotive Qualified to AEC Q100
• Voltage Range: up to 600 V
• dV/dt Immunity ±50 V/ns
• Gate Drive Supply Range from 9 V to 18 V
• Output Source / Sink Current Capability 4.3 A / 4.3 A
• 3.3 V and 5 V Input Logic Compatible
• Extended Allowable Negative Bridge Pin Voltage Swing to –10 V
  ♦ Matched Propagation Delays between Both Channels
  ♦ Propagation Delay 120 ns typically
  ♦ Under VCC LockOut (UVLO) for Both Channels
• Pin to Pin Compatible with Industry Standards
• These are Pb–free Devices

Typical Application

• Power Supplies for Telecom and Datacom
• Half–Bridge and Full–Bridge Converters
• Push–Pull Converters
• High Voltage Synchronous–Buck Converters
• Motor Controls
• Electric Power Steering
• Class–D Audio Amplifiers

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MARKING DIAGRAM

PIN CONNECTIONS

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP5183DR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV5183DR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
NCP5183, NCV5183

Figure 1. Application Schematic

Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No. (SOIC8)</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HIN</td>
<td>High Side Logic Input</td>
</tr>
<tr>
<td>2</td>
<td>LIN</td>
<td>Low Side Logic Input</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>DRVL</td>
<td>Low Side Gate Drive Output</td>
</tr>
<tr>
<td>5</td>
<td>VCC</td>
<td>Main Power Supply</td>
</tr>
<tr>
<td>6</td>
<td>HB</td>
<td>Bootstrap Return or High Side Floating Supply Return</td>
</tr>
<tr>
<td>7</td>
<td>DRVH</td>
<td>High Side Gate Drive Output</td>
</tr>
<tr>
<td>8</td>
<td>VB</td>
<td>Bootstrap Power Supply</td>
</tr>
</tbody>
</table>
### Table 2. ABSOLUTE MAXIMUM RATINGS

All voltages are referenced to GND pin

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>$V_{CC}$</td>
<td>−0.3 to 18</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage on LIN and HIN pins</td>
<td>$V_{LIN}, V_{HIN}$</td>
<td>−0.3 to 18</td>
<td>V</td>
</tr>
<tr>
<td>High Side Boot pin Voltage</td>
<td>$V_{B}$</td>
<td>(higher of (−0.3 ; $V_{CC} − 1.5$)) to 618</td>
<td>V</td>
</tr>
<tr>
<td>High Side Bridge pin Voltage</td>
<td>$V_{HB}$</td>
<td>$V_{B} − 18$ to $V_{B} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>High Side Floating Voltage</td>
<td>$V_{B} − V_{HB}$</td>
<td>−0.3 to 18</td>
<td>V</td>
</tr>
<tr>
<td>High Side Output Voltage</td>
<td>$V_{DRVH}$</td>
<td>$V_{HB} − 0.3$ to $V_{B} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Low Side Output Voltage</td>
<td>$V_{DRVL}$</td>
<td>−0.3 to $V_{CC} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Allowable output slew rate</td>
<td>$dV_{HB}/dt$</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>Maximum Operating Junction Temperature</td>
<td>$T_{J,(max)}$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{STG}$</td>
<td>−55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Human Body Model (Note 1)</td>
<td>$ESDHBM$</td>
<td>3</td>
<td>kV</td>
</tr>
<tr>
<td>ESD Capability, Charged Device Model (Note 1)</td>
<td>$ESDCDM$</td>
<td>1</td>
<td>kV</td>
</tr>
<tr>
<td>Lead Temperature Soldering Reflow</td>
<td>$T_{SLD}$</td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)
   ESD Charged Device Model tested per AEC–Q100–11 (EIA/JESD22–C101E)
2. Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

### Table 3. THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Characteristics SO8 (Note 3)</td>
<td>$R_{JUA}$</td>
<td>183</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

### Table 4. RECOMMENDED OPERATING CONDITIONS (Note 5)

All voltages are referenced to GND pin

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>$V_{CC}$</td>
<td>10</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>High Side Floating Voltage</td>
<td>$V_{B} − V_{HB}$</td>
<td>10</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>High Side Bridge pin Voltage</td>
<td>$V_{HB}$</td>
<td>−1</td>
<td>580</td>
<td>V</td>
</tr>
<tr>
<td>High Side Output Voltage</td>
<td>$V_{DRVH}$</td>
<td>$V_{HB}$</td>
<td>$V_{B}$</td>
<td>V</td>
</tr>
<tr>
<td>Low Side Output Voltage</td>
<td>$V_{DRVL}$</td>
<td>GND</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage on LIN and HIN pins</td>
<td>$V_{LIN}, V_{HIN}$</td>
<td>GND</td>
<td>$V_{CC} − 2$</td>
<td>V</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>$T_{J}$</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
### Table 5. ELECTRICAL CHARACTERISTICS

−40°C ≤ TJ ≤ 125°C, VCC = VB = 15 V, VHB = GND, outputs are not loaded, all voltages are referenced to GND; unless otherwise noted. Typical values are at TJ = +25°C. (Notes 6, 7)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>VCC UVLO</td>
<td>VCC rising</td>
<td>VCCon</td>
<td>7.8</td>
<td>8.8</td>
<td>9.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VCC falling</td>
<td>VCCoff</td>
<td>7.2</td>
<td>8.3</td>
<td>9.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VCC hysteresis</td>
<td>VCChyst</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VB UVLO</td>
<td>VB rising</td>
<td>VBon</td>
<td>7.8</td>
<td>8.8</td>
<td>9.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VB falling</td>
<td>VBoff</td>
<td>7.2</td>
<td>8.3</td>
<td>9.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VB hysteresis</td>
<td>VBhyst</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VCC pin operating current</td>
<td>f = 20 kHz, C_L = 1 nF</td>
<td>ICC1</td>
<td>520</td>
<td></td>
<td>700</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>VB pin operating current</td>
<td>IB1</td>
<td>700</td>
<td>800</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>VCC pin quiescent current</td>
<td>ICC2</td>
<td>95</td>
<td>160</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>VB pin quiescent current</td>
<td>IB2</td>
<td>65</td>
<td>100</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>VB to GND quiescent current</td>
<td>IHSleak</td>
<td>50</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>Input Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic High Input Voltage</td>
<td></td>
<td>VINH</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Low Input Voltage</td>
<td></td>
<td>VINL</td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic High Input Current</td>
<td></td>
<td>IXIN+</td>
<td>25</td>
<td></td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td>Logic Low Input Current</td>
<td></td>
<td>IXIN−</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Input Pull Down Resistance</td>
<td></td>
<td>RXIN</td>
<td>100</td>
<td></td>
<td>250</td>
<td>kΩ</td>
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<tr>
<td><strong>Output Section</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>IDRVL = 0 A</td>
<td>VDRVLL</td>
<td>35</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Low Level Output Voltage (HS Driver)</td>
<td>IDRVH = 0 A</td>
<td>VDRVHL</td>
<td>35</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>IDRVL = 0 A, VDRVRL = VCC − VDRVLL</td>
<td>VDRVRL</td>
<td>35</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>High Level Output Voltage (HS Driver)</td>
<td>IDRVH = 0 A, VDRVHH = VB − VDRVHL</td>
<td>VDRVHH</td>
<td>35</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Output Positive Peak current</td>
<td>VDRVRL = 0 V, PW = 10 μs</td>
<td>IDRVL</td>
<td>4.3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Output Negative Peak current</td>
<td>VDRVRL = 15 V, PW = 10 μs</td>
<td>IDRVHL</td>
<td>4.3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Output Positive Peak current (HS Driver)</td>
<td>VDRVHL = 0 V, PW = 10 μs</td>
<td>IDRVH</td>
<td>4.3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Output Negative Peak current (HS Driver)</td>
<td>VDRVHL = 15 V, PW = 10 μs</td>
<td>IDRVHL</td>
<td>4.3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Output Resistance</td>
<td></td>
<td>ROH</td>
<td>1.7</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Output Resistance</td>
<td></td>
<td>ROL</td>
<td>1.1</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td><strong>Dynamic Section</strong></td>
<td></td>
<td></td>
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<tr>
<td>Turn On Propagation Delay</td>
<td></td>
<td>tON</td>
<td>120</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Turn Off Propagation Delay</td>
<td></td>
<td>tOFF</td>
<td>120</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Delay Matching</td>
<td>Pulse width = 1 μs</td>
<td>tMT</td>
<td>0</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum Positive Pulse Width</td>
<td>VIN = 0 V to 5 V</td>
<td>tminH</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum Negative Pulse Width</td>
<td>VIN = 5 V to 0 V</td>
<td>tminL</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

6. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at TJ = TA = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible
Table 5. ELECTRICAL CHARACTERISTICS

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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage Rise Time</td>
<td>10% to 90%, CL = 1 nF</td>
<td>tr</td>
<td>12</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Fall Time</td>
<td>90% to 10%, CL = 1 nF</td>
<td>tf</td>
<td>12</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Negative HB pin Voltage</td>
<td>PW ≤ tON, VCC = VB = 10 V</td>
<td>VHBneg</td>
<td>−8</td>
<td>−7</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

6. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at TJ = TA = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible

![Figure 3. Propagation Delay, Rise Time and Fall Time Timing](image1)

![Figure 4. Delay Matching](image2)
Figure 5. $V_{CCon}$ vs. Temperature

Figure 6. $V_{CCoff}$ vs. Temperature

Figure 7. $V_{CCUVLOHYS}$ vs. Temperature

Figure 8. $V_{Bon}$ vs. Temperature

Figure 9. $V_{Boff}$ vs. Temperature

Figure 10. $V_{Bhyst}$ vs. Temperature
Figure 11. i_{CC1} vs. Temperature

Figure 12. i_{CC2} vs. Temperature

Figure 13. i_{B1} vs. Temperature

Figure 14. i_{B2} vs. Temperature

Figure 15. i_{H{leak}} vs. Temperature

Figure 16. R_{IN} vs. Temperature
Figure 17. t\text{ON} vs. Temperature

Figure 18. t\text{OFF} vs. Temperature

Figure 19. t\text{r} vs. Temperature

Figure 20. t\text{f} vs. Temperature

Figure 21. t\text{r} for 10 nF Load vs. Temperature

Figure 22. t\text{f} for 10 nF Load vs. Temperature

Figure 23. R\text{OH} vs. Temperature

Figure 24. R\text{OL} vs. Temperature
Figure 25. $t_{MT}$ vs. Temperature

Figure 26. $I_{CC}$ and $I_B$ Current Consumption vs. Frequency

Detail of $I_{CC}$ and $I_B$ Consumption to 150 kHz
MOSFET Turn On and Turn Off Current Path

A capacitor connected from VCC (VB) to GND (HB) terminal is source of energy for charging the gate terminal of an external MOSFET(s). For better understanding of this process see Figure 27 (all voltages are related to GND (HB) pin). When there is a request from internal logic to turn on the external MOSFET, then the Qsource is turned on. The current starts to flow from CVCC (Cboot), through Qsource, gate resistor Rg to the gate terminal of the external MOSFET (depicted by red line). The current loop is closed from external MOSFET source terminal back to the CVCC (Cboot) capacitor. After a while the CGS capacitance is fully charged so no current flows this path. When the external MOSFET going to be turned off, the internal Qsource is turned off first and after a short dead time Qsink is turned on. Then CVCC (Cboot) is not a source any more, the source of energy became the CGS (and all capacitance connected to this terminal, like Muller capacitance). Now the current flows from gate terminal, through Rg resistor and Qsink back to the MOSFET (depicted by blue line). In both cases (charging and discharging external MOSFET) there are several parasitic inductances in the path. All of them play a role during switching. In Figure 27 an influence of the inductances in some places is showed. On VCC (VB) pin a drop during turn on and turn off is observed. If too long an UVLO protection can be triggered and the driver can be turned off subsequently, which result in improper operation of the application.

Figure 27. Equivalent Circuit of Power Switch Driver
Layout Recommendation

The NCP5183 is a high-speed, high-current (sink/source 4.3 A/4.3 A) driver suitable for high-power applications. To avoid any damage and/or malfunction during switching (and/or during transients, overloads, shorts, etc.) it is very important to avoid high parasitic inductances in high current paths (see “MOSFET turn on and turn off current path” section). It is recommended to fulfill some rules in layout. One of the possible layouts for the IC is depicted in Figure 28.

- Keep loop HB\textsubscript{pin} – GND\textsubscript{pin} – Q\textsubscript{LO} as small as possible. This loop (parasitic inductance) has potential to increase negative spike on HB pin which can cause malfunction or damage of HB driver. The negative voltage presented on HB pin is added to V\textsubscript{CC} – V\textsubscript{f} voltage so V\textsubscript{Cboot} is increased. In extreme cases the C\textsubscript{boot} voltage can be so high it will reach maximum rating value which can lead to device damage.
- Keep loop VDD\textsubscript{pin} – GND\textsubscript{pin} – CV\textsubscript{CC} as small as possible. The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q\textsubscript{LO} turn on and voltage drop on VCC pin which can result in UVLO activation.
- Keep loop VB\textsubscript{pin} – HB\textsubscript{pin} – C\textsubscript{boot} as small as possible. The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q\textsubscript{HI} turn on and voltage drop on VB pin which can result in UVLO activation.
- Do not let high current flow through trace between GND\textsubscript{pin} and CV\textsubscript{CC} even a small parasitic inductance here will create high voltage drop if high current flows through this path. This voltage is added or subtracted from HIN and LIN signal, which results in incorrect thresholds or device damaging.
- Keep loops DRVL\textsubscript{pin} – Q\textsubscript{LO} – GND\textsubscript{pin} and DRVH\textsubscript{pin} – Q\textsubscript{HI} – HB\textsubscript{pin} as small as possible. A high parasitic inductance in these paths will result in slow MOSFET switching and undesired resonance on gate terminal.

![Figure 28. Recommended Layout](image-url)
C_boot Capacitor Value Calculation

The device featured two independent 4.3 A sink and source drivers. The low side driver (DRVL) supplies a MOSFET whose source is connected to ground. The driver is powered from V_CC line. The high side driver (DRVH) supplies a MOSFET whose source is floating from GND to bulk voltage. The floating driver is powered from C_boot capacitor. The capacitor is charged only when HB pin is pulled to GND (by inductance or the low side MOSFET when turned on). If too small C_boot capacitor is used the high side UVLO protection can disable the high side driver which leads to improper switching.

Expected voltage on C_boot is depicted in Figure 29. The curves are valid for ZVS (Zero Voltage Switching) observed in LLC applications. For hard switch the curves are slightly different, but from charge on C_boot point of view more favorable. Under the hard switch conditions the energy to charge Q_g (from zero voltage to V_th of the MOSFET) is taken from V_CC capacitor (through an external boot strap diode) so the voltage drop on C_boot is smaller. For the calculation of C_boot value the ZVS conditions are taken account.

The switching cycle is divided into two parts, the charging (t_charge) and the discharging (t_discharge) of the C_boot capacitor. The discharging can be divided even more to discharging by floating driver current consumption I_B2 (t_sub) and to discharging by transfering energy from C_boot to gate terminal of the MOSFET (t_dQm). Discharging by I_B2 becoming more dominant when driver runs at lower frequencies and/or during skip mode operation. To calculate C_boot value, follow these steps:

1. For example, let’s have a MOSFET with Q_g = 30 nC, V_DD = 15 V.
2. Charge stored in C_boot necessary to cover the period the C_boot is not supplied from V_CC line (which is basically the period the high side MOSFET is turned on). Let’s say the application is switching at 100 kHz, 50% duty cycle, which means the upper MOSFET is conductive for 5 μs. It means the C_boot is discharged by I_B2 current (65 μA typ) for 5 μs, so the charge consumed by floating driver is:
   \[ Q_b = I_{B2} \cdot t_{discharge} = 65 \mu A \cdot 5 \mu s = 325 \mu C \]  (eq. 1)
3. Total charge loss during one switching cycle is sum of charge to supply the high side driver and MOSFET’s gate charge:
   \[ Q_{tot} = Q_g + Q_b = 30n + 325p = 30.3 nC \]  (eq. 2)
4. Let’s determine acceptable voltage ripple on C_{boot} to 1% of nominal value, which is 150 mV. To cover charge losses from eq. 2

\[ C_{\text{boot}} = \frac{Q_{\text{tot}}}{V_{\text{ripple}}} = \frac{30.3 \text{nC}}{0.15\text{mV}} = 202 \text{nF} \quad \text{(eq. 3)} \]

It is recommended to increase the value as consumption and gate charge are temperature and voltage dependent, so let’s choose a capacitor 330 nF in this case.

\[
R_{\text{boot}} \text{ Resistor Value Calculation}
\]

To keep the application running properly, it is necessary to charge the C_{boot} again. This is done by external diode from V\text{CC} line to VB pin. In serial with the diode a resistor is placed to reduce the current peaks from V\text{CC} line. The resistor value selection is critical for proper function of the high side driver. If too small high current peaks are drawn from V\text{CC} line, if too high the capacitor will not be charged to appropriate level and the high side driver can be disabled by internal UVLO protection.

First of all keep in mind the capacitor is charged through the external boot strap diode, so it can be charged to a maximum voltage level of V\text{CC} – V\text{f}. The resistor value is calculated using this equation:

\[
R_{\text{boot}} = \frac{t_{\text{charge}}}{C_{\text{boot}} \cdot \ln \left( \frac{V_{\text{max}} - V_{\text{Cmin}}}{V_{\text{max}} - V_{\text{Cmax}}} \right)} = \frac{5\mu \text{s}}{330\text{nF} \cdot \ln \left( \frac{14.4 - 14.2}{14.4 - 14.35} \right)} = 11 \Omega \quad \text{(eq. 4)}
\]

Where:
- \(t_{\text{charge}}\) – time period the C_{boot} is being charged, usually the period the low side MOSFET is turned on
- \(C_{\text{boot}}\) – boot strap capacitor value
- \(V_{\text{max}}\) – maximum voltage the C_{boot} capacitor can be theoretically charged to. Usually the V\text{CC} – V\text{f}. The V\text{f} is forward voltage of used diode.
- \(V_{\text{Cmin}}\) –the voltage level the capacitor is charged from
- \(V_{\text{Cmax}}\) –the voltage level the capacitor is charged to. It is necessary to determine the target voltage for charging, because in theory, when a capacitor is charged from a voltage source through a resistor, the capacitor can never reach the voltage of the source. In this particular case a 50 mV difference (between the voltage behind the diode and V_{\text{Cmax}}) is used.

The resistor value obtained from eq. 4 does not count with the quiescent current I_{B2} of the high side driver. This current will create another voltage drop of:

\[
V_{\text{IB2 drop}} = R_{\text{boot}} \cdot I_{\text{B2}} = 11 \cdot 65\mu\text{A} = 0.7 \text{mV} \quad \text{(eq. 5)}
\]

The current consumed by high side driver will be higher, because the I_{B2} is valid when the device is not switching. While switching, losses by charging and discharging internal transistors as well as the level shifters will be added. This current will increase with frequency.

The additional 0.7 mV drop will be added to V_{\text{Cmax}} value. The additional 0.7 mV drop can be either accepted or the R_{\text{boot}} value can be recalculated to eliminate this additional drop.

The resistor R_{\text{boot}} calculated in eq. 4 is valid under steady state conditions. During start and/or skip operation the starting point voltage value is different (lower) and it takes more time to charge the boot strap capacitor. More over it is not counted with temperature and voltage variability during normal operation or the dynamic resistance of the boot strap diode (approximately 0.34 \Omega for MURA160). From these reasons the resistor value should be decreased especially with respect to skip operation.

Boot strap diode losses calculation.

\[
P_{\text{Dboot}} = Q_{\text{tot}} \cdot V_{\text{f}} \cdot f = 30.3 \text{nC} \cdot 0.6 \cdot 100k = 1.8 \text{mW} \quad \text{(eq. 7)}
\]

Please keep in mind the value is temperature and voltage dependent. Especially C_{boot} voltage can be higher than calculated value. See “Layout recommendation” section for more details.

\[
\text{Total Power Dissipation}
\]

The NCP5183 is suitable to drive high input capacitance MOSFET, from this reason it is equipped with high current capability drivers. Power dissipation on the die, especially at high frequencies can be limiting factor for using this driver. It is important to not exceed maximum junction temperature (listed in absolute maximum ratings table) in any cases. To calculate approximate power losses follow these steps:

1. Power loss of device (except drivers) while switching at appropriate frequency (see Figure 26) is equal to

\[
P_{\text{logic}} = P_{\text{HS}} + P_{\text{LS}} = (V_{\text{boot}} \cdot I_{\text{BSW}}) + (V_{\text{CC}} \cdot I_{\text{CSW}}) = (14.4 \cdot 1.6\mu\text{A}) + (15 \cdot 0.6\mu\text{A}) = 32.1 \text{mW} \quad \text{(eq. 8)}
\]

2. Power loss of drivers

\[
P_{\text{drivers}} = ((Q_{\text{g}} \cdot V_{\text{boot}}) + (Q_{\text{g}} \cdot V_{\text{CC}})) \cdot f = (30n \cdot 14.4) + (30n \cdot 15)) \cdot 100k = 88 \text{mW} \quad \text{(eq. 9)}
\]

3. Total power losses

\[
P_{\text{total}} = P_{\text{logic}} + P_{\text{drivers}} = 32.1 \text{m} + 88 \text{m} = 120 \text{mW} \quad \text{(eq. 10)}
\]

4. Junction temperature increase for calculated power loss

\[
t_{\text{j}} = R_{\text{ja}} \cdot P_{\text{total}} = 183 \cdot 0.12 = 22 \text{K} \quad \text{(eq. 11)}
\]

The temperature calculated in eq. 11 is the value which has to be added to ambient temperature. In case the ambient temperature is 30\text{°C}, the junction temperature will be 52\text{°C}. 

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

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SOLDERING FOOTPRINT*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2
**STYLE 1:**
- **PIN 1.** Emitter
- **PIN 2.** Collector
- **PIN 3.** Collector
- **PIN 4.** Emitter
- **PIN 5.** Base
- **PIN 6.** Emitter
- **PIN 7.** Base
- **PIN 8.** Emitter

**STYLE 2:**
- **PIN 1.** Collector, Die #1
- **PIN 2.** N-Emitter
- **PIN 3.** Collector
- **PIN 4.** Collector
- **PIN 5.** Base, #2
- **PIN 6.** Emitter, #2
- **PIN 7.** Base, #1
- **PIN 8.** Emitter, #1

**STYLE 3:**
- **PIN 1.** Drain, Die #1
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Gate
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

**STYLE 4:**
- **PIN 1.** Drain
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Gate
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

**STYLE 5:**
- **PIN 1.** Drain
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Gate
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

**STYLE 6:**
- **PIN 1.** Source
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Gate
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

**STYLE 7:**
- **PIN 1.** Source
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Gate
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

**STYLE 8:**
- **PIN 1.** Source
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Gate
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

**STYLE 9:**
- **PIN 1.** Emitter, Common
- **PIN 2.** Collector, Die #1
- **PIN 3.** Collector, Die #2
- **PIN 4.** Emitter, Common
- **PIN 5.** Emitter, Common
- **PIN 6.** Base, Die #2
- **PIN 7.** Base, Die #1
- **PIN 8.** Emitter, Common

**STYLE 10:**
- **PIN 1.** Ground
- **PIN 2.** Bias 1
- **PIN 3.** Output
- **PIN 4.** Ground
- **PIN 5.** Ground
- **PIN 6.** Bias 2
- **PIN 7.** Input
- **PIN 8.** Source

**STYLE 11:**
- **PIN 1.** Source 1
- **PIN 2.** GATE 1
- **PIN 3.** Source 2
- **PIN 4.** Gate 2
- **PIN 5.** Drain 2
- **PIN 6.** Drain 2
- **PIN 7.** Drain 1
- **PIN 8.** Drain 1

**STYLE 12:**
- **PIN 1.** Source
- **PIN 2.** Gate 1
- **PIN 3.** Source 2
- **PIN 4.** Gate 2
- **PIN 5.** Drain 2
- **PIN 6.** Drain 2
- **PIN 7.** Drain 1
- **PIN 8.** Drain 1

**STYLE 13:**
- **PIN 1.** N.C.
- **PIN 2.** Source
- **PIN 3.** Source
- **PIN 4.** Gate
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 14:**
- **PIN 1.** N-Source
- **PIN 2.** Source
- **PIN 3.** Source
- **PIN 4.** P-Source
- **PIN 5.** P-Gate
- **PIN 6.** P-Drain
- **PIN 7.** N-Drain
- **PIN 8.** N-Drain

**STYLE 15:**
- **PIN 1.** Source 1
- **PIN 2.** Gate 1
- **PIN 3.** Source 2
- **PIN 4.** Gate 2
- **PIN 5.** Drain 2
- **PIN 6.** Drain 2
- **PIN 7.** Drain 1
- **PIN 8.** Drain 1

**STYLE 16:**
- **PIN 1.** Source
- **PIN 2.** Gate 1
- **PIN 3.** Source 2
- **PIN 4.** Gate 2
- **PIN 5.** Drain 2
- **PIN 6.** Drain 2
- **PIN 7.** Drain 1
- **PIN 8.** Drain 1

**STYLE 17:**
- **PIN 1.** VCC
- **PIN 2.** V2OUT
- **PIN 3.** VOUT
- **PIN 4.** TXE
- **PIN 5.** RXE
- **PIN 6.** VEE
- **PIN 7.** GND
- **PIN 8.** ACC

**STYLE 18:**
- **PIN 1.** Anode
- **PIN 2.** Anode
- **PIN 3.** Source
- **PIN 4.** Gate
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Cathode
- **PIN 8.** Cathode

**STYLE 19:**
- **PIN 1.** Line 1 IN
- **PIN 2.** Common ANODE/GND
- **PIN 3.** Common ANODE/GND
- **PIN 4.** Line 2 IN
- **PIN 5.** Line 2 OUT
- **PIN 6.** Common ANODE/GND
- **PIN 7.** Common ANODE/GND
- **PIN 8.** Line 1 OUT

**STYLE 20:**
- **PIN 1.** Source (N)
- **PIN 2.** Gate (N)
- **PIN 3.** Source (P)
- **PIN 4.** Gate (P)
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 21:**
- **PIN 1.** Anode
- **PIN 2.** Gate 1
- **PIN 3.** Source
- **PIN 4.** Gate 2
- **PIN 5.** Source
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 22:**
- **PIN 1.** Common Cathode/VCC
- **PIN 2.** Common Cathode/VCC
- **PIN 3.** Common Cathode/VCC
- **PIN 4.** Common Cathode/VCC
- **PIN 5.** Common Cathode/VCC
- **PIN 6.** Common Cathode/VCC
- **PIN 7.** Common Cathode/VCC
- **PIN 8.** Common Cathode/VCC

**STYLE 23:**
- **PIN 1.** Line 1 IN
- **PIN 2.** Common ANODE/GND
- **PIN 3.** Common ANODE/GND
- **PIN 4.** Line 2 IN
- **PIN 5.** Line 2 OUT
- **PIN 6.** Common ANODE/GND
- **PIN 7.** Common ANODE/GND
- **PIN 8.** Line 1 OUT

**STYLE 24:**
- **PIN 1.** Base
- **PIN 2.** Emitter
- **PIN 3.** Collector/Anode
- **PIN 4.** Collector/Anode
- **PIN 5.** Cathode
- **PIN 6.** Cathode
- **PIN 7.** Collector/Anode
- **PIN 8.** Collector/Anode

**STYLE 25:**
- **PIN 1.** N.C.
- **PIN 2.** Gate
- **PIN 3.** Source
- **PIN 4.** Gate
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 26:**
- **PIN 1.** VIN
- **PIN 2.** GND
- **PIN 3.** Enable
- **PIN 4.** ILIMIT
- **PIN 5.** Source
- **PIN 6.** Source
- **PIN 7.** Source
- **PIN 8.** Source

**STYLE 27:**
- **PIN 1.** Drain
- **PIN 2.** Drain
- **PIN 3.** Source
- **PIN 4.** Source
- **PIN 5.** Source
- **PIN 6.** Source
- **PIN 7.** Source
- **PIN 8.** Source

**STYLE 28:**
- **PIN 1.** SW_TO_GND
- **PIN 2.** GND
- **PIN 3.** DV/DT
- **PIN 4.** Input
- **PIN 5.** Source
- **PIN 6.** Source
- **PIN 7.** Source
- **PIN 8.** Source

**STYLE 29:**
- **PIN 1.** BASE, DIE #1
- **PIN 2.** Emitter, #1
- **PIN 3.** BASE, #2
- **PIN 4.** Emitter, #2
- **PIN 5.** Collector, #2
- **PIN 6.** Collector, #2
- **PIN 7.** Collector, #1
- **PIN 8.** Collector, #1

**STYLE 30:**
- **PIN 1.** Drain
- **PIN 2.** Drain
- **PIN 3.** Source
- **PIN 4.** Source
- **PIN 5.** Source
- **PIN 6.** Source
- **PIN 7.** Source
- **PIN 8.** Source

**STYLE 31:**
- **PIN 1.** Collector, Die, #1
- **PIN 2.** Collector, Die, #1
- **PIN 3.** Collector, Die, #1
- **PIN 4.** Collector, Die, #1
- **PIN 5.** Collector, Die, #1
- **PIN 6.** Collector, Die, #1
- **PIN 7.** Collector, Die, #1
- **PIN 8.** Collector, Die, #1

**TABLES:**
- **TABLE 1:**
  - **Column 1:** Description
  - **Column 2:** Value

**DOCUMENT NUMBER:** 98ASB42564B

**DESCRIPTION:** SOIC–8 NB

**PAGE 2 OF 2**

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