Test Procedure for the NCP1568 UHD Board

ON Semiconductor®

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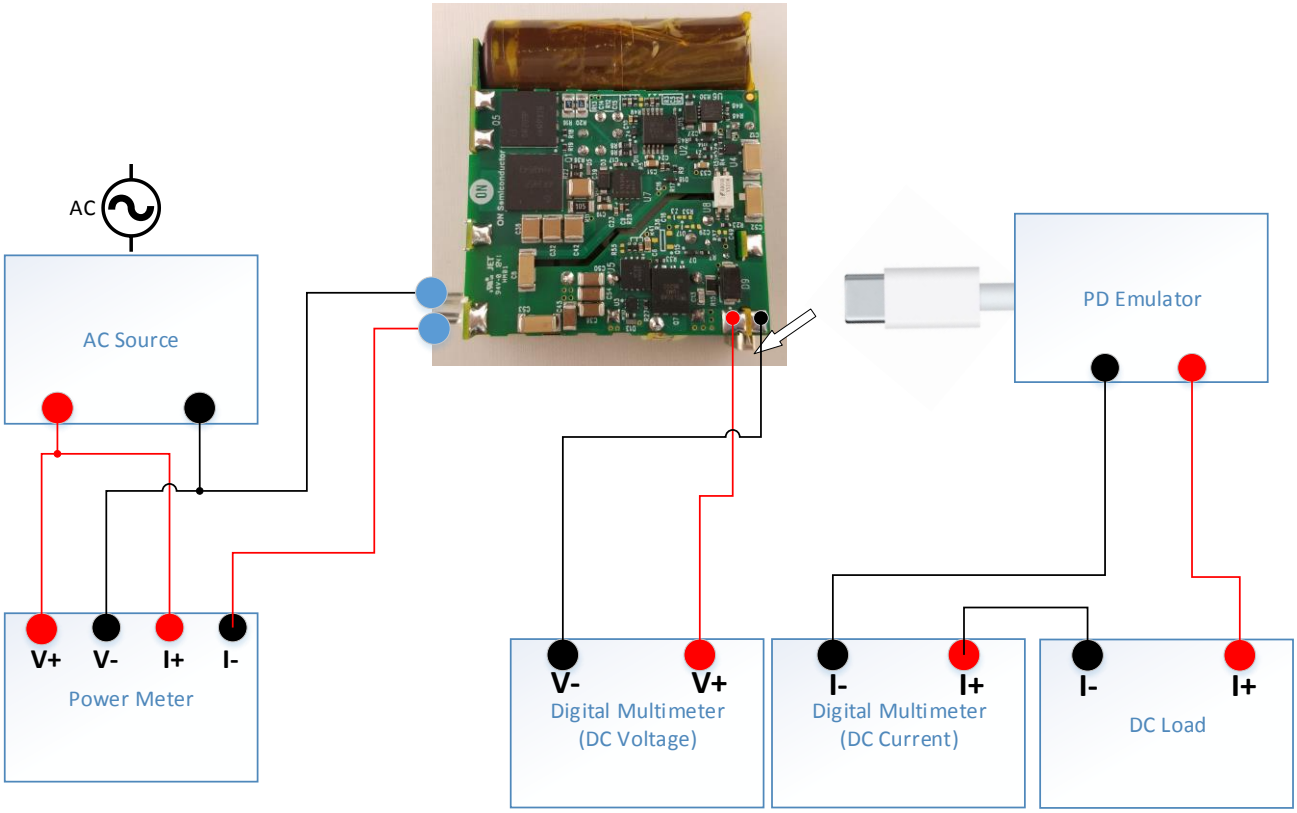

Figure 1 - Test Configuration

Table 1: Required Equipment

*Chroma 61604 AC Source	*Yokogawa WT210 Power Meter	*Agilent 34401A Digital Multimeter x2
*Kikusui PLZ303W DC Electronic Load	*Tektronix TDS5034B Oscilloscope	One NCP1568 UHD Board + PD Emulator

*Equivalent test equipment may be substituted

Test Procedure:

1. Leads will need to be soldered on the board in order to properly check signals and output. Solder insulated wires onto points 1 through 5 in Figure 2 below.
2. Connect the output of the board to the PD emulator as shown in Figure 1.
3. Connect the Agilent 34401A Digital Multimeter (measuring DC I) in series with the output of the PD emulator and the Kikusui PLZ303W DC Electronic Load. Reference figure 1.
4. Set Kikusui PLZ303W DC Electronic Load to C.C. mode.
5. Set load current on Kikusui PLZ303W DC Electronic Load to 500 mA.
6. Connect the Agilent 34401A Digital Multimeter (measuring DC V) to the nodes as shown on Figure 1 (VOUT & SECGND in Figure 2).
7. Connect the AC power source and power meter as shown in Figure 1.
8. Set the AC power source to 115 VAC, 60 Hz and turn on power source
9. Using the PD Emulator, set the output to 20 V and verify that the output measures 20 +/- 0.4 V.
10. Slowly increase the load current to 3 A. Verify on Agilent current multimeter that current is 3 A +/- 1%.
11. Allow UHD board to run for approximately 10 minute then use the Input Power Meter to measure input power. Calculate the efficiency and record measurements.
12. Take the efficiency readings at 2.25 A (75% load), 1.5 A (50% load), 0.75A (25% load) and 0.3A (10% load). Verify that the readings are close to as in Table 2.
13. Set the AC power source to 230 VAC, 50 Hz and turn on power source.
14. Repeat steps 8-11.
15. Turn off the AC power source.
16. Using the PD Emulator, set the output to 5 V and verify that the output measures 5 +/- 0.2 V
17. Repeat steps 7-13.
18. Turn off the AC power source.
19. Attach Channel 1 of oscilloscope to the node “Vsw” (see Figure 2), ground at the GND point (Figure 2).
20. Attach Channel 2 of oscilloscope to the node “LDRV” (see Figure 2), ground at the GND point (Figure 2).
21. Set oscilloscope trigger to Ch2, rising edge, DC coupling, 6 V trig reference, run mode (continuous), and variable display persistence.
22. Set the PD Emulator to the 5 V output setting.
23. Set the input voltage to 115 Vac
24. Turn on AC source.
25. Turn DC load to 2.25 A, and check to see that the board is operating in CCM (see Figure 3)
26. Turn DC load to 0.3 A, and check to see that the board is operating in DCM (see Figure 4)

27. Slowly turn load up to 2.25 A (or until mode transition) and check to see a clean transition from DCM to CCM (clean transition is detailed in Figure 5)
28. Slowly turn load down to 0.3 A (or until mode transition) and check to see a clean transition from CCM to DCM (clean transition is detailed in Figure 5)
29. Change AC voltage to 230 Vac
30. Repeat steps 23-26
31. Turn off AC source.
32. Repeat steps 22-31 for all output voltages [9 V, 15 V, 20 V]
33. Since high voltage will be present on bulk capacitor, discharge should be performed from GND and VSW (Figure 2). Use a dc voltmeter to verify voltage is less than 20 VDC before continuing.
34. Disconnect the AC source.
35. Disconnect the electronic load.
36. Disconnect multimeters.
37. Disconnect oscilloscope probes.
38. Remove the soldered connections (Figure 2) and clean the points (clean soldering and clean flux).
39. End of test.

Table 2. 20 V Efficiency Measurements

	Measured	Limit	Measurement				Calculated 4−point Avg. Efficiency Measurement	Limit
Output Power [%]	10%		25%	50%	75%	100%		
Efficiency [%] @ VIN = 115 Vrms	84.5	78.9%	87.4	91.8	92.6	**92.8**	91.1	88 %
Efficiency [%] @ VIN = 230 Vrms	80.7	78.9%	86.5	90.1	92.7	**92.9**	90.4	88 %

Table 3. 5 V Efficiency Measurements

	Measured	Limit	Measurement				Calculated 4−point Avg. Efficiency Measurement	Limit
Output Power [%]	10%		25%	50%	75%	100%		
Efficiency [%] @ VIN = 115 Vrms	80.2	72.5%	83.8	89.2	90.0	**90.3**	88.3	82%
Efficiency [%] @ VIN = 230 Vrms	74.4	72.5%	79.0	86.6	88.8	**89.7**	86.0	82%

1. GND – Top Left Solder Point
2. VSW – Top XFMR Node
3. LDRV – Left of Resistors
4. VOUT – Left side of Daughter Card
5. SECGND – Right side of Daughter Card

Figure 2 Solder Points

Transitions Information

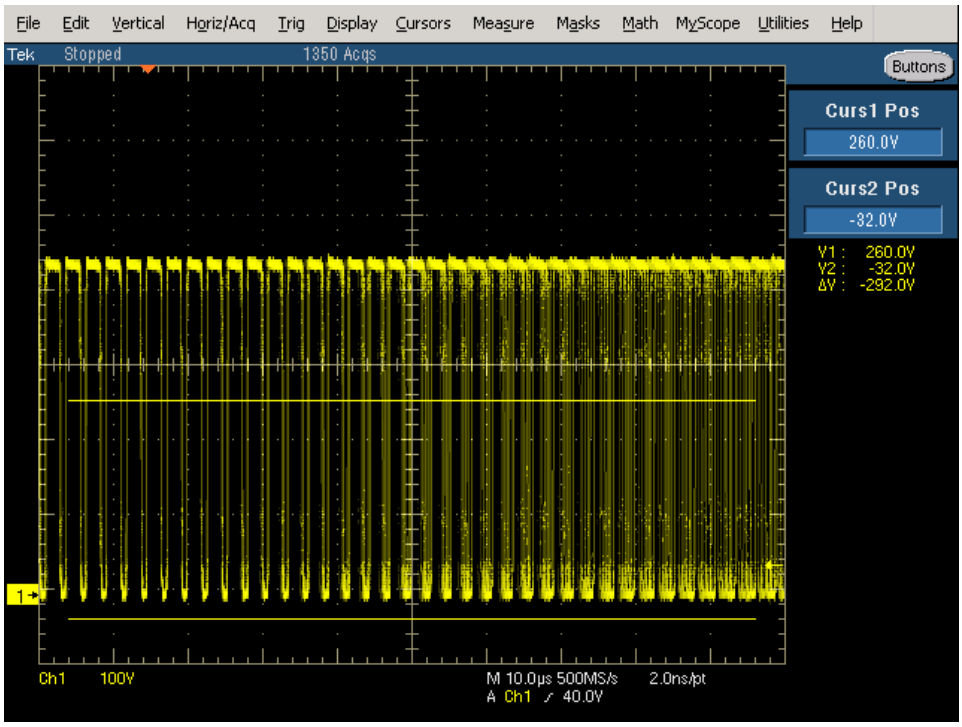

Figure 3 - Clean CCM Operation

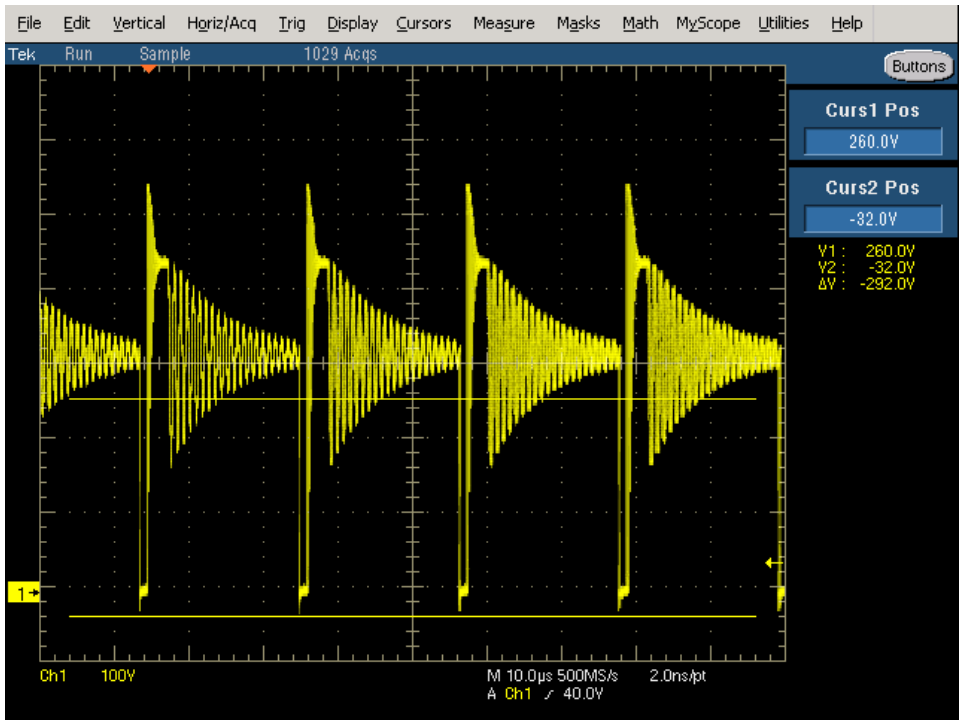

Figure 4 - Clean DCM Operation

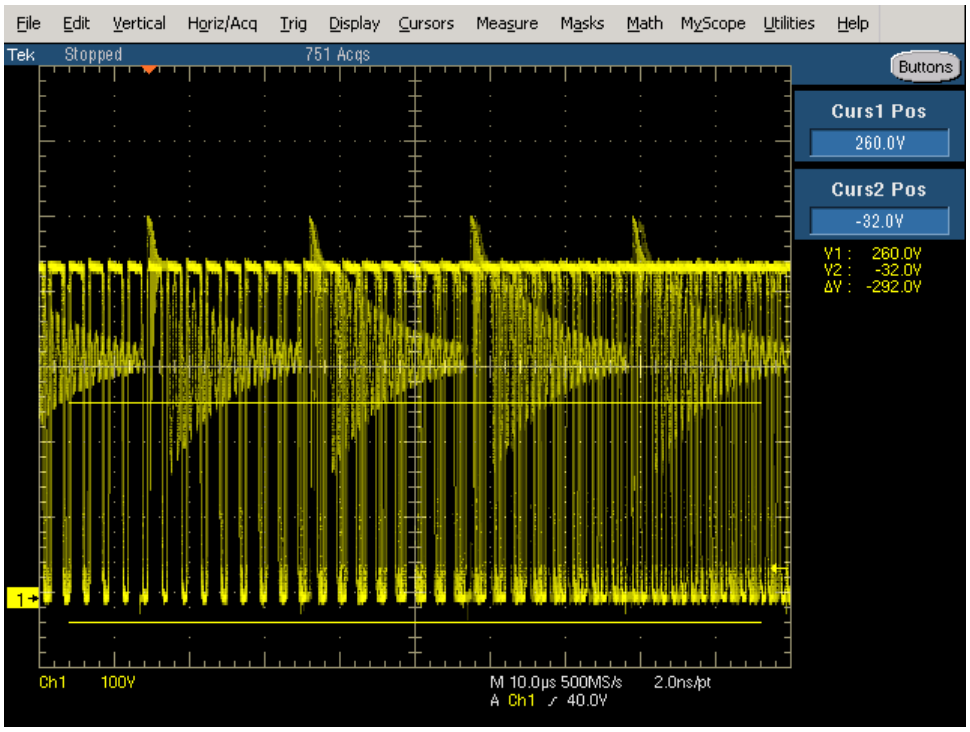

Figure 5 - Transition Overlap CCM/DCM

Transitions:

- Clean transition allows for distinct DCM and CCM operation at any single load point.
- If overlap (figure 5) is seen at any given load point without settling on DCM or CCM operation within 2 seconds, this is not a clean transition.