Quasi-Resonant Flyback Controller, High Frequency

NCP1342

The NCP1342 is a highly integrated quasi–resonant flyback controller suitable for designing high–performance off–line power converters. With an integrated active X2 capacitor discharge feature, the NCP1342 can enable no–load power consumption below 30 mW.

The NCP1342 features a proprietary valley–lockout circuitry, ensuring stable valley switching. This system works down to the 6th valley and transitions to frequency foldback mode to reduce switching losses. As the load decreases further, the NCP1342 enters quiet–skip mode to manage the power delivery while minimizing acoustic noise.

To ensure light load performance with high frequency designs, the NCP1342 incorporates Rapid Frequency Foldback with Minimum Peak Current Modulation to reduce the switching frequency quickly. To help ensure converter ruggedness, the NCP1342 implements several key protective features such as internal brownout detection, a non–dissipative Over Power Protection (OPP) for constant maximum output power regardless of input voltage, a latched overvoltage and NTC–ready overtemperature protection through a dedicated pin, and line removal detection to safely discharge the X2 capacitors when the ac line is removed.

Features
- Integrated High–Voltage Startup Circuit with Brownout Detection
- Integrated X2 Capacitor Discharge Capability
- Wide VCC Range from 9 V to 28 V
- 28 V VCC Overvoltage Protection
- Abnormal Overcurrent Fault Protection for Winding Short Circuit or Saturation Detection
- Internal Temperature Shutdown
- Valley Switching Operation with Valley–Lockout for Noise–Free Operation
- Frequency Foldback with 25 kHz Minimum Frequency Clamp for Increased Efficiency at Light Loads
- Rapid Frequency Foldback for Fast Reduction of Switching Frequency at Light Loads
- Skip Mode with Quiet–Skip Technology for Highest Performance During Light Loads
- Minimized Current Consumption for No Load Power Below 30 mW
- Frequency Jittering for Reduced EMI Signature
- Latching or Auto–Recovery Timer–Based Overload Protection
- Adjustable Overpower Protection (OPP)
- Adjustable Maximum Frequency Clamp
- Fault Pin for Severe Fault Conditions, NTC Compatible for OTP
- 4 ms Soft–Start Timer

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.
Figure 1. NCP1342 8–Pin Typical Application Circuit

Figure 2. NCP1342 9–Pin Typical Application Circuit
# NCP1342

## Table 1. PART NUMBER DECODE – NCP1342ABCDEF

<table>
<thead>
<tr>
<th>NCP1342</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>OTP/Overload</td>
<td>Jitter Frequency/Amplitude</td>
<td>Quiet–Skip</td>
<td>CS Min</td>
<td>CS Min Shift</td>
<td>Additional</td>
</tr>
<tr>
<td>A – AR/AR</td>
<td>A – 1.55 kHz/75 mV</td>
<td>A – 800 Hz</td>
<td>A – 200 mV</td>
<td>A – 400 mV</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>B – Latch/AR</td>
<td>B – 1.55 kHz/92 mV</td>
<td>B – 1.2 kHz</td>
<td>B – 150 mV</td>
<td>B – 350 mV</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>C – AR/Latch</td>
<td>C – 1.55 kHz/55 mV</td>
<td>C – 1.56 kHz</td>
<td>C – 100 mV</td>
<td>C – 300 mV</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>D – Latch/Latch</td>
<td>D – 1.55 kHz/61 mV</td>
<td>D – Disabled</td>
<td>D – 250 mV</td>
<td>D – 250 mV</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td>E – AR/None</td>
<td>E – 1.3 kHz/75 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>E</td>
<td></td>
</tr>
<tr>
<td>F – Latch/None</td>
<td>F – 1.3 kHz/92 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td>G – 1.3 kHz/55 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>G</td>
<td></td>
</tr>
<tr>
<td>H – 1.3 kHz/61 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>J – 3.9 kHz/75 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>J</td>
<td></td>
</tr>
<tr>
<td>K – 3.9 kHz/92 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>K</td>
<td></td>
</tr>
<tr>
<td>L – 3.9 kHz/55 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>M – 3.9 kHz/61 mV</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>M</td>
<td></td>
</tr>
<tr>
<td>N – Disabled</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>N</td>
<td></td>
</tr>
</tbody>
</table>

*Not present in all parts. See Table 2 for details.

## Table 2. ADDITIONAL PART OPTIONS

<table>
<thead>
<tr>
<th>F</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>–</td>
<td>Default Configuration</td>
</tr>
<tr>
<td>A</td>
<td>X2 Discharge Disabled, V&lt;sub&gt;BO(stop)&lt;/sub&gt; = 84 V, V&lt;sub&gt;BO(start)&lt;/sub&gt; = 94 V</td>
</tr>
<tr>
<td>D</td>
<td>X2 Discharge Disabled, V&lt;sub&gt;BO(stop)&lt;/sub&gt; = 84 V, V&lt;sub&gt;BO(start)&lt;/sub&gt; = 94 V, Resettable Overload Timer</td>
</tr>
<tr>
<td>E</td>
<td>X2 Discharge Disabled, Brownout Disabled</td>
</tr>
<tr>
<td>F</td>
<td>X2 Discharge Disabled, V&lt;sub&gt;CC(off)&lt;/sub&gt; Triggers Autorecovery Timer (t&lt;sub&gt;restart&lt;/sub&gt;)</td>
</tr>
<tr>
<td>G</td>
<td>X2 Discharge Disabled</td>
</tr>
<tr>
<td>H</td>
<td>V&lt;sub&gt;BO(stop)&lt;/sub&gt; = 84 V, V&lt;sub&gt;BO(start)&lt;/sub&gt; = 94 V</td>
</tr>
</tbody>
</table>

## Table 3. ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device Marking</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1342AMDCDCDR2G</td>
<td>1342AMDC</td>
<td>SOIC–8 NB (Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>NCP1342ANDAAD1R2G</td>
<td>1342ANDA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342DADBDD1R2G</td>
<td>1342DADB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342AMDCDAD1R2G</td>
<td>1342AMDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342AMACD1R2G</td>
<td>1342AMAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342ANACD1R2G</td>
<td>1342ANAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342ANDBD1R2G</td>
<td>1342ANDB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342BKCDCAD1R2G</td>
<td>1342BKDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342BMDCCAD1R2G</td>
<td>1342BMDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342BMDCD1R2G</td>
<td>1342BMDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342ANACCD1R2G</td>
<td>1342ANAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342ENACEFD1R2G (In Development)</td>
<td>1342ENACE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342AMDADDG1R2G</td>
<td>1342AMDAD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1342AMDCDHD1R2G</td>
<td>1342AMDCD</td>
<td></td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1342ENDCEAD1R2G (In Development)</td>
<td>1342ENDCE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 3. NCP1342 Block Diagram

Table 4. PIN FUNCTIONAL DESCRIPTION

<table>
<thead>
<tr>
<th>8–Pin</th>
<th>9–Pin</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Fault</td>
<td>The controller enters fault mode if the voltage on this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor.</td>
</tr>
<tr>
<td>–</td>
<td>2</td>
<td>FMAX</td>
<td>A resistor to ground sets the value for the maximum switching frequency clamp. If this pin is pulled above 4 V, the maximum frequency clamp is disabled.</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>FB</td>
<td>Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>ZCD/OPP</td>
<td>A resistor divider from the auxiliary winding to this pin provides input to the demagnetization detection comparator and sets the OPP compensation level.</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>CS</td>
<td>Input to the cycle–by–cycle current limit comparator.</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>GND</td>
<td>Ground reference.</td>
</tr>
<tr>
<td>6</td>
<td>7</td>
<td>DRV</td>
<td>This is the drive pin of the circuit. The DRV high-current capability (~0.5 /+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>VCC</td>
<td>This pin is the positive supply of the IC. The circuit starts to operate when VCC exceeds 17 V and turns off when VCC goes below 9 V (typical values). After start–up, the operating range is 9 V up to 28 V.</td>
</tr>
<tr>
<td>–</td>
<td>9</td>
<td>N/C</td>
<td>Removed for creepage distance.</td>
</tr>
<tr>
<td>8</td>
<td>10</td>
<td>HV</td>
<td>This pin is the input for the high voltage startup and brownout detection circuits. It also contains the line removal detection circuit to safely discharge the X2 capacitors when the line is removed.</td>
</tr>
</tbody>
</table>
Table 5. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Voltage Startup Circuit Input Voltage</td>
<td>$V_{HV(MAX)}$</td>
<td>−0.3 to 700</td>
<td>V</td>
</tr>
<tr>
<td>High Voltage Startup Circuit Input Current</td>
<td>$I_{HV(MAX)}$</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Input Voltage</td>
<td>$V_{CC(MAX)}$</td>
<td>−0.3 to 30</td>
<td>V</td>
</tr>
<tr>
<td>Supply Input Current</td>
<td>$I_{CC(MAX)}$</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Input Voltage Slew Rate</td>
<td>$dV_{CC}/dt$</td>
<td>1</td>
<td>V/μs</td>
</tr>
<tr>
<td>Fault Input Voltage</td>
<td>$V_{Fault(MAX)}$</td>
<td>−0.3 to $V_{CC}$ + 0.7 V</td>
<td>V</td>
</tr>
<tr>
<td>Fault Input Current</td>
<td>$I_{Fault(MAX)}$</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Zero Current Detection and OPP Input Voltage</td>
<td>$V_{ZCD(MAX)}$</td>
<td>−0.3 to $V_{CC}$ + 0.7 V</td>
<td>V</td>
</tr>
<tr>
<td>Zero Current Detection and OPP Input Current</td>
<td>$I_{ZCD(MAX)}$</td>
<td>−2/+5</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum Input Voltage (Other Pins)</td>
<td>$V_{MAX}$</td>
<td>−0.3 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Input Current (Other Pins)</td>
<td>$I_{MAX}$</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Driver Maximum Voltage (Note 1)</td>
<td>$V_{DRV}$</td>
<td>−0.3 to $V_{DRV(high)}$</td>
<td>V</td>
</tr>
<tr>
<td>Driver Maximum Current</td>
<td>$I_{DRV(SRC)}$</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$I_{DRV(SNK)}$</td>
<td>800</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_{j}$</td>
<td>−40 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_{j(MAX)}$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{STG}$</td>
<td>−60 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>Power Dissipation ($T_{A} = 25$°C, 1 oz. Cu, 42 mm$^2$ Copper Clad Printed Circuit)</td>
<td>$P_{D(MAX)}$</td>
<td>450</td>
<td>mW</td>
</tr>
<tr>
<td>DR2G Suffix, SOIC−8</td>
<td></td>
<td>330</td>
<td>mW</td>
</tr>
<tr>
<td>D1R2G Suffix, SOIC−9</td>
<td></td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>Thermal Resistance ($T_{A} = 25$°C, 1 oz. Cu, 42 mm$^2$ Copper Clad Printed Circuit)</td>
<td>$R_{i(jA)}$</td>
<td>225</td>
<td>°C/W</td>
</tr>
<tr>
<td>DR2G Suffix, SOIC−8</td>
<td></td>
<td>300</td>
<td>°C/W</td>
</tr>
<tr>
<td>D1R2G Suffix, SOIC−9</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>ESD Capability</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human Body Model per JEDEC Standard JESD22−A114F (All pins except HV)</td>
<td>$V_{DH(max)}$</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Human Body Model per JEDEC Standard JESD22–A114F (HV Pin)</td>
<td>$V_{DS(max)}$</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>Charge Device Model per JEDEC Standard JESD22−C101F</td>
<td>$V_{C(max)}$</td>
<td>1000</td>
<td>V</td>
</tr>
<tr>
<td>Latch–Up Protection per JEDEC Standard JESD78E</td>
<td>$I_{L(max)}$</td>
<td>±100</td>
<td>mA</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when $V_{CC}$ exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is $V_{CC}$. 
## Table 6. ELECTRICAL CHARACTERISTICS:

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>dV/dt = 0.1 V/ms</td>
<td>VCC(on)</td>
<td>16.0</td>
<td>17.0</td>
<td>18.0</td>
<td>V</td>
</tr>
<tr>
<td>Startup Threshold</td>
<td>VCC increasing</td>
<td>VCC(x2_reg)</td>
<td>17.0</td>
<td>18.0</td>
<td>19.0</td>
<td>V</td>
</tr>
<tr>
<td>Discharge Voltage During Line Removal</td>
<td>VCC decreasing</td>
<td>VCC(offs)</td>
<td>8.5</td>
<td>9.0</td>
<td>9.5</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Operating Voltage</td>
<td>VCC decreasing</td>
<td>VCC(HYS)</td>
<td>7.5</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Operating Hysteresis</td>
<td>VCC(on) – VCC(offs)</td>
<td>VCC(reset)</td>
<td>4.5</td>
<td>6.5</td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>Internal Latch / Logic Reset Level</td>
<td>VCC increasing, IHV = 650 µA</td>
<td>VCC(inhibit)</td>
<td>0.30</td>
<td>0.70</td>
<td>1.05</td>
<td>µA</td>
</tr>
<tr>
<td>Transition from Istart1 to Istart2</td>
<td>dV/dt = 0.1 V/ms</td>
<td>VCC increasing, IHV = 650 µA</td>
<td>–</td>
<td>–</td>
<td>500</td>
<td>µs</td>
</tr>
<tr>
<td>VCC(on) Delay</td>
<td>VCC decreasing</td>
<td>tdelay(VCC_off)</td>
<td>25</td>
<td>32</td>
<td>40</td>
<td>µs</td>
</tr>
<tr>
<td>Startup Delay</td>
<td>Delay from VCC(on) to DRV Enable</td>
<td>tdelay(start)</td>
<td>–</td>
<td>–</td>
<td>500</td>
<td>µs</td>
</tr>
<tr>
<td>Minimum Voltage for Start–Up Current Source</td>
<td>VCC(on)</td>
<td>VHV(MIN)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Inhibit Current Sourced from VCC Pin</td>
<td>Vcc = 0 V</td>
<td>Istart1</td>
<td>0.2</td>
<td>0.5</td>
<td>0.65</td>
<td>mA</td>
</tr>
<tr>
<td>Start–Up Current Sourced from VCC Pin</td>
<td>VCC = VCC(on) – 0.5 V</td>
<td>Istart2</td>
<td>2.4</td>
<td>3.75</td>
<td>5.0</td>
<td>mA</td>
</tr>
<tr>
<td>Start–Up Circuit Off–State Leakage Current</td>
<td>VHV = 162.5 V</td>
<td>IHV(offs1)</td>
<td>–</td>
<td>–</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>VHV = 325 V</td>
<td>IHV(offs2)</td>
<td>–</td>
<td>–</td>
<td>20</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>VHV = 700 V</td>
<td>IHV(offs3)</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td>Supply Current Fault or Latch</td>
<td>VCC = VCC(on) – 0.5 V</td>
<td>ICC1</td>
<td>–</td>
<td>0.115</td>
<td>0.250</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>fsw = 50 kHz, CDRV = open</td>
<td>ICC2</td>
<td>–</td>
<td>0.230</td>
<td>0.400</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>fsw = 50 kHz, CDRV = open</td>
<td>ICC3</td>
<td>–</td>
<td>1.0</td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td>VCC Overvoltage Protection Threshold</td>
<td>VCC(OVP)</td>
<td>27</td>
<td>28</td>
<td>29</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC Overvoltage Protection Delay</td>
<td>tdelay(VCC_OVP)</td>
<td>25</td>
<td>32</td>
<td>40</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

### X2 CAPACITOR DISCHARGE (ALL VERSIONS EXCEPT xxxxxA, xxxxxD, xxxxxE, xxxxxF, xxxxxG)

| Line Voltage Removal Detection Timer | tline(removal) | 65 | 100 | 135 | ms |
| Discharge Timer Duration | tline(discharge) | 21 | 32 | 43 | ms |
| Line Detection Timer Duration | tline(detect) | 21 | 32 | 43 | ms |
| VCC Discharge Current | VCC = 20 V | ICC(discharge) | 13 | 18 | 23 | mA |
| HV Discharge Level | VHV(discharge) | – | – | 30 | V |

### BROWNOUT DETECTION (ALL VERSIONS EXCEPT xxxxxE)

| System Start–Up Threshold | VHV increasing | VBO(start) | 107 | 112 | 116 | V |
| Other Versions | Versions xxxxxA, xxxxxD, xxxxxH | 89 | 94 | 99 |
| Brownout Threshold | VHV decreasing | VBO(stop) | 93 | 98 | 102 | V |
| Other Versions | Versions xxxxxA, xxxxxD, xxxxxH | 79 | 84 | 89 |
| Hysteresis | VHV increasing | VBO(HYS) | 9.0 | 14 | – | V |
| Other Versions | Versions xxxxxA, xxxxxD, xxxxxH | 6.0 | 10 | – | V |
| Brownout Detection Blanking Time | VHV decreasing | tBO(stop) | 40 | 70 | 100 | ms |

### GATE DRIVE

| Rise Time | VDRV from 10% to 90% | tDRV(rise) | – | 20 | 40 | ns |
| Fall Time | VDRV from 90% to 10% | tDRV(fall) | – | 5 | 30 | ns |

2. NTC with R110 = 8.8 kΩ
Table 6. ELECTRICAL CHARACTERISTICS: (VCC = 12 V, VHV = 120 V, VFault = open, VFB = 2.4 V, VCS = 0 V, VZCD = 0 V, VFMAX = 0 V, CVCC = 100 nF, CDRV = 100 pF, for typical values TJ = 25°C, for min/max values, TJ is –40°C to 125°C, unless otherwise noted)

<table>
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<tr>
<th>Characteristics</th>
<th>Conditions</th>
<th>Symbol</th>
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<td>VCC = VCC(off) + 0.2 V, RDRV = 10 kΩ</td>
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<td>V2t03</td>
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<td>After soft–start complete</td>
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<td>Current Limit Threshold Voltage</td>
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<td>tdelay(ILIM1)</td>
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<td>95</td>
<td>175</td>
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2. NTC with R110 = 8.8 kΩ
Table 6. ELECTRICAL CHARACTERISTICS: (VCC = 12 V, VHV = 120 V, VFault = open, VFB = 2.4 V, VCS = 0 V, VZCD = 0 V, VMAX = 0 V, C VCC = 100 nF, C DRV = 100 pF, for typical values TJ = 25°C, for min/max values, TJ is – 40°C to 125°C, unless otherwise noted)

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<td>Step VCS 0 V to 0.7 V, VFB = 2.4</td>
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<td>Step VCS 0 V to VILIM2 + 0.5 V, VFB = 4 V</td>
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<td>Overpower Protection Delay</td>
<td>VCS dv/dt = 1 V/µs, measured from VOPP(MAX) to DRV falling edge</td>
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<td>Soft–Start Period</td>
<td>Measured from 1st DRV pulse to VCS = VILIM1</td>
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2. NTC with R110 = 8.8 kΩ
Table 6. ELECTRICAL CHARACTERISTICS: (VCC = 12 V, VHV = 120 V, VFault = open, VFB = 2.4 V, VCS = 0 V, VZCD = 0 V, VMAX = 0 V, C = 100 nF, CDRV = 100 pF, for typical values T = 25°C, for min/max values, T is –40°C to 125°C, unless otherwise noted)

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<td>–</td>
<td>40</td>
<td>–</td>
<td>°C</td>
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2. NTC with R110 = 8.8 kΩ
The NCP1342 implements a quasi–resonant flyback converter utilizing current–mode architecture where the switch–off event is dictated by the peak current. This IC is an ideal candidate where low parts count and cost effectiveness are the key parameters, particularly in ac–dc adapters, open–frame power supplies, etc. The NCP1342 incorporates all the necessary components normally needed in modern power supply designs, bringing several enhancements such as non–dissipative overpower protection (OPP), brownout protection, and frequency reduction management for optimized efficiency over the entire power range. Accounting for the needs of extremely low standby power requirements, the controller features minimized current consumption and includes an automatic X2 capacitor discharge circuit that eliminates the need to install power–consuming resistors across the X2 input capacitors.

- **High–Voltage Start–Up Circuit:** Low standby power consumption cannot be obtained with the classic resistive start–up circuit. The NCP1342 incorporates a high–voltage current source to provide the necessary current during start–up and then turns off during normal operation.

- **Internal Brownout Protection:** The ac input voltage is sensed via the high–voltage pin. When this voltage is too low, the NCP1342 stops switching. No restart attempt is made until the ac input voltage is back within its normal range.

- **X2–Capacitor Discharge Circuitry:** Per the IEC60950 standard, the time constant of the X2 input capacitors and their associated discharge resistors must be less than 1 s in order to avoid electrical shock when the user unplugs the power supply and inadvertently touches the ac input cord terminals. By providing an automatic means to discharge the X2 capacitors, the NCP1342 eliminates the need to install X2 discharge resistors, thus reducing power consumption.

- **Quasi–Resonant, Current–Mode Operation:** Quasi–Resonant (QR) mode is a highly efficient mode of operation where the MOSFET turn–on is synchronized with the point where its drain–source voltage is at the minimum (valley). A drawback of this mode of operation is that the operating frequency is inversely proportional to the system load. The NCP1342 incorporates a valley lockout (VLO) and frequency foldback technique to eliminate this drawback, thus maximizing the efficiency over the entire power range.

- **Valley Lockout:** In order to limit the maximum frequency while remaining in QR mode, one would traditionally use a frequency clamp. Unfortunately, this can cause the controller to jump back and forth between two different valleys, which is often undesirable. The NCP1342 patented VLO circuitry solves this issue by determining the operating valley based on the system load, and locking out other valleys unless a significant change in load occurs.

- **Rapid Frequency Foldback:** As the load continues to decrease, it becomes beneficial to reduce the switching frequency. When the load is light enough, the NCP1342 enters rapid frequency foldback mode. During this mode, the minimum peak current is limited and dead–time is added to the switching cycle, thus reducing the frequency and switching operation to discontinuous conduction mode (DCM). Dead–time continues to be added until skip mode is reached, or the switching frequency reaches its minimum level of 25 kHz.

- **Minimum Peak Current Modulation (MPCM):** In order to reduce the switching frequency even faster (for high frequency designs), the NCP1342 uses MPCM to increase the minimum peak current during frequency foldback. It also reduces the minimum peak current gradually as the load decreases to ensure optimum skip mode entry.

- **Skip Mode:** To further improve light or no–load power consumption while avoiding audible noise, the NCP1342 enters skip mode when the operating frequency reaches its minimum value. To avoid acoustic noise, the circuit prevents the switching frequency from decaying below 25 kHz. This allows regulation via bursts of pulses at 25 kHz or greater instead of operating in the audible range.

- **Quiet–Skip:** To further reduce acoustic noise, the NCP1342 incorporates a novel circuit to prevent the skip mode burst period from entering the audible range as well.

- **Internal OPP:** In order to limit power delivery at high line, a scaled version of the negative voltage present on the auxiliary winding during the on–time is routed to the ZCD/OPP pin. This provides the designer with a simple and non–dissipative means to reduce the maximum power capability as the bulk voltage increases.

- **Frequency Jittering:** In order to reduce the EMI signature, a low frequency triangular voltage waveform is added to the input of the PWM comparator. This helps by spreading out the energy peaks during noise analysis.

- **Internal Soft–Start:** The NCP1342 includes a 4 ms soft–start to prevent the main power switch from being overly stressed during start–up. Soft–start is activated each time a new startup sequence occurs or during auto–recovery mode.
• **Dedicated Fault Input:** The NCP1342 includes a dedicated fault input. It can be used to sense an overvoltage condition and latch off the controller by pulling the pin above the overvoltage protection (OVP) threshold. The controller is also disabled if the Fault pin is pulled below the overtemperature protection (OTP) threshold. The OTP threshold is configured for use with a NTC thermistor.

• **Overload/Short−Circuit Protection:** The NCP1342 implements overload protection by limiting the maximum time duration for operation during overload conditions. The overload timer operates whenever the maximum peak current is reached. In addition to this, special circuitry is included to prevent operation in CCM during extreme overloads, such as an output short−circuit.

• **Maximum Frequency Clamp:** The 9−pin version of NCP1342 includes a maximum frequency clamp. The clamp can be adjusted via an external resistor from the FMAX Pin to ground. It can also be disabled by pulling the FMAX pin above 4 V.

**HIGH VOLTAGE START−UP**

The NCP1342 contains a multi−functional high voltage (HV) pin. While the primary purpose of this pin is to reduce standby power while maintaining a fast start−up time, it also incorporates brownout detection and line removal detection.

The HV pin must be connected directly to the ac line in order for the X2 discharge circuit to function correctly. Line and neutral should be diode “ORed” before connecting to the HV pin as shown in Figure 4. The diodes prevent the pin voltage from going below ground. A resistor in series with the pin should be used to protect the pin during EMC or surge testing. A low value resistor should be used (<5 kΩ) to reduce the voltage offset during start−up.

![Figure 4. High−Voltage Input Connection](image)

**Start−up and VCC Management**

During start−up, the current source turns on and charges the VCC capacitor with $I_{\text{start2}}$ (typically 6 mA). When $V_{\text{cc}}$ reaches $V_{\text{CC(on)}}$ (typically 16.0 V), the current source turns off. If the input voltage is not high enough to ensure a proper start−up (i.e., $V_{\text{HV}}$ has not reached $V_{\text{BO(start)}}$), the controller will not start. $V_{\text{CC}}$ then begins to fall because the controller bias current is at $I_{\text{CC2}}$ (typically 1 mA) and the auxiliary supply voltage is not present. When $V_{\text{CC}}$ falls to $V_{\text{CC(off)}}$ (typically 10.5 V), the current source turns back on and charges $V_{\text{CC}}$. This cycle repeats indefinitely until $V_{\text{HV}}$ reaches $V_{\text{BO(start)}}$. Once this occurs, the current source immediately turns on and charges $V_{\text{CC}}$ to $V_{\text{CC(on)}}$, at which point the controller starts (see Figure 6).

When $V_{\text{CC}}$ is brought below $V_{\text{CC(inhibit)}}$, the start−up current is reduced to $I_{\text{start1}}$ (typically 0.5 mA). This limits power dissipation on the device in the event that the $V_{\text{CC}}$ pin is shorted to ground. Once $V_{\text{CC}}$ rises back above $V_{\text{CC(inhibit)}}$, the start−up current returns to $I_{\text{start2}}$.

Once $V_{\text{CC}}$ reaches $V_{\text{CC(on)}}$, the controller is enabled and the controller bias current increases to $I_{\text{CC3}}$ (typically 2.0 mA). However, the total bias current is greater than this due to the gate charge of the external switching MOSFET. The increase in $I_{\text{CC}}$ due to the MOSFET is calculated using Equation 1.

$$\Delta I_{\text{CC}} = f_{\text{sw}} \cdot Q_{\text{G}} \cdot 10^{-3}$$  \hspace{1cm} (eq. 1)

where $\Delta I_{\text{CC}}$ is the increase in milliamps, $f_{\text{sw}}$ is the switching frequency in kilohertz and $Q_{\text{G}}$ is the gate charge of the external MOSFET in nanocoulombs.

$C_{\text{VCC}}$ must be sized such that a $V_{\text{CC}}$ voltage greater than $V_{\text{CC(off)}}$ is maintained while the auxiliary supply voltage increases during start−up. If $C_{\text{VCC}}$ is too small, $V_{\text{CC}}$ will fall below $V_{\text{CC(off)}}$ and the controller will turn off before the auxiliary winding supplies the IC. The total $I_{\text{CC}}$ current after the controller is enabled ($I_{\text{CC3}} + \Delta I_{\text{CC}}$) must be considered to correctly size $C_{\text{VCC}}$. 
**Figure 5. Start-up Circuitry Block Diagram**

- **Start-up Current** = $I_{\text{start1}}$
- **Start-up Current** = $I_{\text{start2}}$

**Figure 6. Start-up Timing**

- $V_{BO(\text{start})}$
- $V_{HV(\text{MIN})}$
- $V_{CC(on)}$
- $V_{CC(\text{off})}$
- $V_{CC(\text{inhibit})}$
- $t_{\text{delay (start)}}$
The NCP1342 maximum supply voltage, $V_{CC(MAX)}$, is 28 V. Typical high-voltage MOSFETs have a maximum gate voltage rating of 20 V. The DRV pin incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The DRV voltage clamp, $V_{DRV(high)}$, is typically 12 V with a maximum limit of 14 V.

**REGULATION CONTROL**

**Peak Current Control**

The NCP1342 is a peak current–mode controller, thus the FB voltage sets the peak current flowing in the transformer and the MOSFET. This is achieved by sensing the MOSFET current across a resistor and applying the resulting voltage ramp to the non–inverting input of the PWM comparator through the CS pin. The current limit threshold is set by applying the FB voltage divided by $K_{FB}$ (typically 4) to the inverting input of the PWM comparator. When the current sense voltage ramp exceeds this threshold, the output driver is turned off, however, the peak current is affected by several functions (see Figure 7):

- The peak current level is clamped during the soft-start phase. The setpoint is actually limited by a clamp level ramping from 0 to 0.8 V within 4 ms.
- In addition to the PWM comparator, a dedicated comparator monitors the current sense voltage, and if it reaches the maximum value, $V_{ILIM}$ (typically 800 mV), the gate driver is turned off and the overload timer is enabled. This occurs even if the limit imposed by the feedback voltage is higher than $V_{ILIM}$. Due to the parasitic capacitances of the MOSFET, a large voltage spike often appears on the CS Pin at turn–on. To prevent this spike from falsely triggering the current sense circuit, the current sense signal is blanked for a short period of time, $t_{LEB1}$ (typically 275 ns), by a leading edge blanking (LEB) circuit. Figure 7 shows the schematic of the current sense circuit.
- The peak current is also limited to a minimum level, $V_{CS(MIN)}$ (0.2 V, typically). This results in higher efficiency at light loads by increasing the minimum energy delivered per switching cycle, while reducing the overall number of switching cycles during light load.

![Figure 7. Current Sense Logic](image-url)
Zero Current Detection
The NCP1342 is a quasi–resonant (QR) flyback controller. While the power switch turn–off is determined by the peak current set by the feedback loop, the switch turn–on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized has the benefit of reduced switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lump capacitance, eventually settling at the input voltage. A QR flyback controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce switching losses and electromagnetic interference (EMI).

As shown by Figure 13, a valley is detected once the ZCD pin voltage falls below the demagnetization threshold, $V_{ZCD_{(trig)}}$, typically 55 mV. The controller will either switch once the valley is detected or increment the valley counter, depending on the FB voltage.

Overpower Protection
The average bulk capacitor voltage of the QR flyback varies with the RMS line voltage. Thus, the maximum power capability at high line can be much higher than desired. An integrated overpower protection (OPP) circuit provides a relatively constant output power limit across the input voltage on the bulk capacitor, $V_{bulk}$. Since it is a high–voltage rail, directly measuring $V_{bulk}$ will contribute losses in the sensing network that will greatly impact the standby power consumption. The NCP1342 OPP circuit achieves this without the need for a high–voltage sensing network, and is essentially lossless.
Since the auxiliary winding voltage during the power
switch on time is a reflection of the input voltage scaled by
the primary to auxiliary winding turns ratio, $N_{P:AUX}$ (see
Figure 9), OPP is achieved by scaling down reflected
voltage during the on–time and applying it to the ZCD pin
as a negative voltage, $V_{OPP}$. The voltage is scaled down by
a resistor divider comprised of $R_{OPPU}$ and $R_{OPPL}$. The
maximum internal current setpoint ($V_{CS(OPP)}$) is simply the
sum of $V_{OPP}$ and the peak current sense threshold, $V_{ILIM1}$.
Figure 8 shows the schematic for the OPP circuit.
The adjusted peak current limit is calculated using
Equation 2. For example, a $V_{OPP}$ of $-150$ mV results in a
peak current limit of 650 mV in NCP1342.

$$V_{CS(OPP)} = V_{OPP} + V_{ILIM1} \quad (eq. 2)$$

To ensure optimal zero–crossing detection, a diode is
needed to bypass $R_{OPPU}$ during the off–time. Equation 3 is
used to calculate $R_{OPPU}$ and $R_{OPPL}$.

$$R_{ZCD} + \frac{R_{OPPU}}{R_{OPPL}} = - \frac{N_{P:AUX} \cdot V_{bulk} - V_{OPP}}{V_{OPP}} \quad (eq. 3)$$

$R_{OPPU}$ is selected once a value is chosen for $R_{OPPL}$.$R_{OPPL}$ is selected large enough such that enough voltage is
available for the zero–crossing detection during the
off–time. It is recommended to have at least 8 V applied on
the ZCD pin for good detection. The maximum voltage is
internally clamped to $V_{CC}$. The off–time voltage on the ZCD
Pin is given by Equation 4.

$$V_{ZCD} = \frac{R_{OPPL}}{R_{ZCD} + R_{OPPL}} \cdot (V_{AUX} - V_{F}) \quad (eq. 4)$$

Where $V_{AUX}$ is the voltage across the auxiliary winding
and $V_{F}$ is the DOPP forward voltage drop.

The ratio between $R_{ZCD}$ and $R_{OPPL}$ is given by
Equation 5. It is obtained by combining Equations 3 and 4.

$$\frac{R_{ZCD}}{R_{OPPL}} = \frac{V_{AUX} - V_{F} - V_{ZCD}}{V_{ZCD}} \quad (eq. 5)$$

A design example is shown below:

System Parameters:

$$V_{AUX} = 18 \text{ V}$$
$$V_{F} = 0.6 \text{ V}$$
$$N_{P:AUX} = 0.18$$

The ratio between $R_{ZCD}$ and $R_{OPPL}$ is calculated using
Equation 5 for a minimum $V_{ZCD}$ of 8 V.

$$\frac{R_{ZCD}}{R_{OPPL}} = \frac{18 \text{ V} - 0.6 \text{ V} - 8 \text{ V}}{8 \text{ V}} = 1.2 \text{ k\Omega}$$

$R_{ZCD}$ is arbitrarily set to 1 k\Omega. $R_{OPPL}$ is also set to 1 k\Omega
because the ratio between the resistors is close to 1.
The NCP1342 maximum overpower compensation or peak current setpoint reduction is 31.25% for a $V_{OPP}$ of
$-250$ mV. We will use this value for the following example:
Substituting values in Equation 3 and solving for $R_{OPPU}$
we obtain:

$$\frac{R_{ZCD}}{R_{OPPL}} = \frac{0.18 \cdot 370 \text{ V} - (-0.25 \text{ V})}{-0.25 \text{ V}} = 271$$
$$R_{OPPU} = 271 \cdot R_{OPPL} - R_{ZCD}$$
$$R_{OPPU} = 271 \cdot 1 \text{ k\Omega} - 1 \text{ k\Omega} = 270 \text{ k\Omega}$$

For optimum performance over temperature, it is
recommended to keep $R_{OPPL}$ below 3 k\Omega.
Soft-Start
Soft-start is achieved by ramping up an internal reference, \(V_{\text{START}}\) and comparing it to the current sense signal. \(V_{\text{START}}\) ramps up from 0 V once the controller initially powers up. The peak current setpoint is then limited by the \(V_{\text{START}}\) ramp resulting in a gradual increase of the switch current during start-up. The soft-start duration, \(t_{\text{SSTART}}\), is typically 4 ms.

During startup, demagnetization phases are long and difficult to detect since the auxiliary winding voltage is very small. In this condition, the 6 ms steady-state timeout is generally shorter than the inductor demagnetization period. If it is used to restart a switching cycle, it can cause operation in CCM for several cycles until the voltage on the ZCD pin is high enough to prevent the timer from running. Therefore, a longer timeout period, \(t_{\text{OUT1}}\) (typically 100 \(\mu\)s), is used during soft-start to prevent CCM operation.

Frequency Jittering
In order to help meet stringent EMI requirements, the NCP1342 features frequency jittering to average the energy peaks over the EMI frequency range. As shown in Figure 10, the function consists of summing a triangular wave of amplitude \(V_{\text{jitter}}\) and frequency \(f_{\text{jitter}}\) with the CS signal immediately before the PWM comparator. This current acts to modulate the on-time and hence the operation frequency.

Since the jittering function modulates the peak current level, the FB signal will attempt to compensate for this effect in order to limit the output voltage ripple. Therefore, the bandwidth of the feedback loop must be well below the jitter frequency, or the jitter function will be filtered by the loop.

Due to the minimum peak current, the effect of the jittering circuit will not be seen during frequency foldback mode.

Maximum Frequency Clamp
All 9-pin versions of the NCP1342 include an adjustable maximum frequency clamp via an external resistor from the FMAX Pin to ground. It can also be disabled by pulling the FMAX pin above 4 V. The maximum frequency can be programmed using Equation 6, and is shown in Figure 11.

\[
F_{\text{SW(MAX)}} = \frac{261 \text{ kHz} \times 1 \text{ V}}{R_{\text{FMAX}} \times 10 \text{ \(\mu\)A}} \quad (\text{eq. 6})
\]
LIGHT LOAD MANAGEMENT

Valley Lockout Operation

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However, when used by itself, such an approach often causes instabilities since when this clamp is active, the controller tends to jump (or hesitate) between two valleys, thus generating audible noise.

Instead, the NCP1342 also incorporates a patented valley lockout (VLO) circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. This technique extends the QR mode operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency.

The operating valley (1st, 2nd, 3rd, 4th, 5th or 6th) is determined by the FB voltage. An internal counter increments each time a valley is detected by the ZCD/OPP Pin. Figure 12 shows a typical frequency characteristic obtainable at low line in a 65 W application.

Table 7. VALLEY FB THRESHOLDS (typical values)

<table>
<thead>
<tr>
<th>FB Falling</th>
<th>FB Rising</th>
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</thead>
<tbody>
<tr>
<td>1st to 2nd valley</td>
<td>1.400 V</td>
</tr>
<tr>
<td>2nd to 3rd valley</td>
<td>1.200 V</td>
</tr>
<tr>
<td>3rd to 4th valley</td>
<td>1.100 V</td>
</tr>
<tr>
<td>4th to 5th valley</td>
<td>1.000 V</td>
</tr>
<tr>
<td>5th to 6th valley</td>
<td>0.900 V</td>
</tr>
<tr>
<td>2nd to 1st valley</td>
<td>2.000 V</td>
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<tr>
<td>3rd to 2nd valley</td>
<td>1.800 V</td>
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<tr>
<td>4th to 3rd valley</td>
<td>1.700 V</td>
</tr>
<tr>
<td>5th to 4th valley</td>
<td>1.600 V</td>
</tr>
<tr>
<td>6th to 5th valley</td>
<td>1.500 V</td>
</tr>
</tbody>
</table>

Valley Timeout

In case of extremely damped oscillations, the ZCD comparator may not be able to detect the valleys. In this condition, drive pulses will stop while the controller waits for the next valley or ZCD event. The NCP1342 ensures continued operation by incorporating a maximum timeout period after the last demagnetization detection. The timeout signal acts as a substitute for the ZCD signal to the valley counter. Figure 13 shows the valley timeout circuit schematic. The steady state timeout period, t_{out2}, is set at 6 µs (typical) to limit the frequency step.

During startup, the voltage offset added by the OPP diode, D_{OPP}, prevents the ZCD Comparator from accurately detecting the valleys. In this condition, the steady state
timeout period will be shorter than the inductor demagnetization period causing CCM operation. CCM operation lasts for a few cycles until the voltage on the ZCD pin is high enough to detect the valleys. A longer timeout period, $t_{\text{out1}}$, (typically 100 $\mu$s) is set during soft-start to limit CCM operation.

In VLO operation, the number of timeout periods are counted instead of valleys when the drain–source voltage oscillations are too damped to be detected. For example, if the FB voltage sets VLO mode to turn on at the fifth valley, and the ZCD ringing is damped such that the ZCD circuit is only able to detect:
- Valleys 1 to 4: the circuit generates a DRV pulse 6 $\mu$s (steady-state timeout delay) after the 4th valley detection.
- Valleys 1 to 3: the timeout delay must run twice, and the circuit generates a DRV pulse 12 $\mu$s after the 3rd valley detection.

### Figure 13. Valley Timeout Circuitry

**Rapid Frequency Foldback with Minimum Peak Current Modulation (MPCM)**

As the output load decreases (FB voltage decreases), the valleys are incremented from 1 to 6. When the sixth valley is reached and the FB voltage further decreases to $V_{\text{MPCM(entry)}}$ (800 mV typical), the controller enters MPCM and begins frequency foldback (FF). At this point, the minimum peak current is increased by $V_{\text{MPCM(delta)}}$ (400 mV typical). The increase in peak current serves to force the switching frequency to a much lower value, thus improving the efficiency at light loads. During this mode, the controller regulates the power delivery by modulating the switching frequency.

Once in frequency foldback mode, the controller reduces the switching frequency by adding dead–time after the 6th valley is detected. This dead–time increases as the FB voltage decreases.

The dead–time circuit is designed to add 0 $\mu$s dead–time when $V_{\text{FB}} = 0.4$ V and linearly increases the total dead–time to $t_{\text{DT(MAX)}}$ (36 $\mu$s typical) as $V_{\text{FB}}$ falls down to 0.4 V. The minimum frequency clamp prevents the switching frequency from dropping below 25 kHz to eliminate the risk of audible noise. Note that the dead–time is not added (it is blanked) until MPCM is engaged to ensure valley switching prior to entering MPCM mode.

In addition to dead–time, the peak current setpoint is linearly reduced as $V_{\text{FB}}$ falls down to 0.4 V. This ensures that the peak current is not too high during the lightest loads, and has the effect of reducing the skip entry power level. Figure 14 shows the MPCM with respect to the feedback voltage, while Figure 15 shows the VLO to FF operation.

To reduce the output power hysteresis between entering and exiting MPCM, the exit threshold ($V_{\text{MPCM(exit)}}$) is set slightly below the entry threshold (750 mV typical). A 1 ms timer, $t_{\text{MPCM}}$, is engaged every time MPCM is entered or exited to prevent oscillations during the operating point transition. If at any time FB falls to skip mode, or rises to 5th valley, MPCM will be immediately exited regardless of $t_{\text{MPCM}}$.
Figure 14. Minimum Peak Current Modulation

Figure 15. Valley Lockout Thresholds
Minimum Frequency Clamp and Skip Mode

As mentioned previously, the circuit prevents the switching frequency from dropping below \( f_{MIN} \) (25 kHz typical). When the switching cycle would be longer than 40 \( \mu \)s, the circuit forces a new switching cycle. However, the \( f_{MIN} \) clamp cannot generate a DRV pulse until the demagnetization is completed. In other words, it will not cause operation in CCM.

Since the NCP1342 forces a minimum peak current and a minimum frequency, the power delivery cannot be continuously controlled down to zero. Instead, the circuit starts skipping pulses when the FB voltage drops below the skip level, \( V_{skip} \), and recovers operation when \( V_{FB} \) exceeds \( V_{skip} + V_{skip(HYS)} \). This skip–mode method provides an efficient method of control during light loads.

Quiet–Skip

To further avoid acoustic noise, the circuit prevents the burst frequency during skip mode from entering the audible range by limiting it to a maximum of 800 Hz. This is achieved via a timer \( t_{quiet} \) that is activated during Quiet–Skip. The start of the next burst cycle is prevented until this timer has expired.

As the output power decreases, the switching frequency decreases. Once it hits 25 kHz, the skip–in threshold is reached and burst mode is entered – switching stops as soon as the current drive pulses ends – it does not stop immediately.

Once switching stops, FB will rise. As soon as FB crosses the skip–exit threshold, drive pulses will resume, but the controller remains in burst mode. At this point, a 1.25 ms timer, \( t_{quiet} \), is started together with a count–to–3 counter. The next time the FB voltage drops below the skip–in threshold, drive pulses stop at the end of the current pulse as long as 3 drive pulses have been counted (if not, they do not stop until the end of the 3rd pulse). They are not allowed to start again until the timer expires, even if the skip–exit threshold is reached first. It is important to note that the timer will not force the next cycle to begin – i.e. if the natural skip frequency is such that skip–exit is reached after the timer expires, the drive pulses will wait for the skip–exit threshold.

This means that during no–load, there will be a minimum of 3 drive pulses, and the burst–cycle period will likely be much longer than 1.25 ms. This operation helps to improve efficiency at no–load conditions.

In order to exit burst mode, the FB voltage must rise higher than 1 V. If this occurs before \( t_{quiet} \) expires, the drive pulses will resume immediately – i.e. the controller won’t wait for the timer to expire. Figure 16 provides an example of how Quiet–Skip works.
Figure 16. Quiet–Skip Timing Diagram
fault management

The NCP1342 contains three separate fault modes. Depending on the type of fault, the device will either latch off, restart when the fault is removed, or resume operation after the auto-recovery timer expires.

**Latching Faults**

Some faults will cause the NCP1342 to latch off. These include the abnormal OCP (AOCP), V_{CC} OVP, and the external latch input. When the NCP1342 detects a latching fault, the driver is immediately disabled. The operation during a latching fault is identical to that of a non-latching fault except the controller will not attempt to restart at the next V_{CC(on)}, even if the fault is removed. In order to clear the latch and resume normal operation, V_{CC} must first be allowed to drop below V_{CC(reset)} or a line removal event must be detected. This operation is shown in Figure 17.

---

**Figure 17. Operation During Latching Fault**
Non–Latching Faults
When the NCP1342 detects a non–latching fault (brownout or thermal shutdown), the drivers are disabled, and VCC falls towards VCC\text{(off)} due to the IC internal current consumption. Once VCC reaches VCC\text{(off)}, the HV current source turns on and C\text{VCC} begins to charge towards VCC\text{(on)}. When VCC, reaches VCC\text{(on)}, the cycle repeats until the fault is removed. Once the fault is removed, the NCP1342 is re–enabled when VCC reaches VCC\text{(on)} according to the initial power–on sequence, provided VHV is above VBO\text{(start)}. This operation is shown in Figure 18. When VHV is reaches VBO\text{(start)}, VCC immediately charges to VCC\text{(on)} if VCC is already above VCC\text{(on)} when the fault is removed, the controller will start immediately as long as VHV is above VBO\text{(start)}.

Figure 18. Operation During Non–Latching Fault
Auto-recovery Timer Faults

Some faults cause the NCP1342 auto-recovery timer to run. If an auto-recovery fault is detected, the gate drive is disabled and the auto-recovery timer, $t_{autorec}$ (typically 1.2 s), starts. While the auto-recovery timer is running, the HV current source turns on and off to maintain $V_{cc}$ between $V_{cc(off)}$ and $V_{cc(on)}$. Once the auto-recovery timer expires, the controller will attempt to start normally at the next $V_{cc(on)}$ provided $V_{HV}$ is above $V_{BO(start)}$. This operation is shown in Figure 19.

![Auto-recovery Timer Faults Diagram](image-url)
PROTECTION FEATURES

Brownout Protection

A timer is enabled once \( V_{HV} \) drops below its disable threshold, \( V_{BO(stop)} \) (typically 99 V). The controller is disabled if \( V_{HV} \) doesn’t exceed \( V_{BO(stop)} \) before the brownout timer, \( t_{BO} \) (typically 54 ms), expires. The timer is set long enough to ignore a two cycle dropout. The timer starts counting once \( V_{HV} \) drops below \( V_{BO(stop)} \).

Figure 20 shows the brownout detector waveforms during a brownout.

When a brownout is detected, the controller stops switching and enters non-latching fault mode (see Figure 18). The HV current source alternatively turns on and off to maintain \( V_{CC} \) between \( V_{CC(on)} \) and \( V_{CC(\text{off})} \) until the input voltage is back above \( V_{BO(\text{start})} \).

Line Removal Detection and X2 Capacitor Discharge

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistor network is the most common method to meet this requirement. Unfortunately, the resistor network consumes power across all operating modes and it is a major contributor of input power losses during light-load and no-load conditions.

The NCP1342 eliminates the need for external discharge resistors by integrating active input filter capacitor discharge circuitry. A novel approach is used to reconfigure the high voltage startup circuit to discharge the input filter capacitors upon removal of the ac line voltage. The line removal detection circuitry is always active to ensure safety compliance.

The line removal is detected by digitally sampling the voltage present at the HV pin, and monitoring the slope. A timer, \( t_{\text{line(removal)}} \) (typically 100 ms), is used to detect when the slope of the input signal is negative or below the resolution level. The timer is reset any time a positive slope...
is detected. Once the timer expires, a line removal condition is acknowledged initiating an X2 capacitor discharge cycle, and the controller is disabled.

If $V_{CC}$ is above $V_{CC(on)}$, it is first discharged to $V_{CC(on)}$. A second timer, $t_{line(discharge)}$ (typically 32 ms), is used for the time limiting of the discharge phase to protect the device against overheating. Once the discharge phase is complete, $t_{line(discharge)}$ is reused while the device checks to see if the line voltage is reapplied. During the discharge phase, if $V_{CC}$ drops to $V_{CC(on)}$, it is quickly recharged to $V_{CC(X2_reg)}$. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(discharge)}$ (30 V maximum). This feature allows the device to discharge large X2 capacitors in the input line filter to a safe level.

It is important to note that the HV pin cannot be connected to any dc voltage due to this feature, i.e. directly to the bulk capacitor.

![Figure 21. Line Removal Timing](image-url)
An over temperature protection block monitors the junction temperature during the discharge process to avoid thermal runaway, in particular during open/short pins safety tests. Please note that the X2 discharge capability is also active at all times, including off-mode and before the controller actually starts to pulse (e.g. if the user unplugs the converter during the start-up sequence).

**Dedicated Fault Input**

The NCP1342 includes a dedicated fault input accessible via the Fault pin (8-pin and 9-pin versions only). The controller can be latched by pulling up the pin above the upper fault threshold, \(V_{\text{Fault(OVP)}}\) (typically 3.0 V). The controller is disabled if the Fault pin voltage is pulled below the lower fault threshold, \(V_{\text{Fault(OTP_in)}}\) (typically 0.4 V). The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 23 shows the architecture of the Fault input.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, \(t_{\text{delay(OVP)}}\) and \(t_{\text{delay(OTP)}}\), are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.
OVP
An active clamp prevents the Fault pin voltage from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull-up current has to be higher than the pull-down capability of the clamp (set by $R_{\text{Fault(clamp)}}$ at $V_{\text{Fault(clamp)}}$), i.e., approximately 1 mA.

The upper fault threshold is intended to be used for an overvoltage fault using a zener diode and a resistor in series from the auxiliary winding voltage. The controller is latched once $V_{\text{Fault}}$ exceeds $V_{\text{Fault(OVP)}}$.

Once the controller is latched, it follows the behavior of a latching fault according to Figure 17 and is only reset if $V_{\text{CC}}$ is reduced to $V_{\text{CC(reset)}}$, or $X2$ discharge is activated. In the typical application these conditions occur only if the ac voltage is removed from the system.

OTP
The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source, $I_{\text{Fault(OTP)}}$ (typically 45.0 μA), generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{\text{Fault(OTP)}}$.

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{\text{Fault(OTP)}}$. This current source is enabled once $V_{\text{CC}}$ reaches $V_{\text{CC(on)}}$. A filter capacitor is typically connected between the Fault and GND pins. This will result in a delay before $V_{\text{Fault}}$ reaches its steady state value once $I_{\text{Fault(OTP)}}$ is enabled. Therefore, the lower fault comparator (i.e. overtemperature detection) is ignored during soft-start.

Version A latches off the controller after an overtemperature fault is detected according to Figure 17. In Version B, the controller is re-enabled once the fault is removed such that $V_{\text{Fault}}$ increases above $V_{\text{Fault(OTP_out)}}$, the auto-recovery timer expires, and $V_{\text{CC}}$ reaches $V_{\text{CC(on)}}$ as shown in Figure 19.

![Figure 23. Fault Pin Internal Schematic](image-url)
Overload Protection
The overload timer integrates the duration of the overload fault. That is, the timer count increases while the fault is present and reduces its count once it is removed. The overload timer duration, \( t_{OVLD} \), is typically 160 ms. When the overload timer expires, the controller detects an overload condition does one of the following:

- The controller latches off (version A) or
- Enters a safe, low duty–ratio auto–recovery mode (version B).

Figure 24 shows the overload circuit schematic, while Figure 25 and Figure 26 show operating waveforms for latched and auto–recovery overload conditions.

![Overload Circuitry Diagram]

**Figure 24. Overload Circuitry**
Figure 25. Latched Overload Operation
Figure 26. Auto-Recovery Overload Operation

- **Output Load**
  - Max Load
  - Overcurrent applied

- **Fault Flag**
  - Fault timer starts
  - Fault disappears

- **V_{CC}**
  - Fault timer starts
  - Restarts At V_{CC(on)} (new burst cycle if Fault still present)

- **V_{CC(on)}**
  - Controller stops

- **V_{CC(off)}**

- **DRV**
  - Controller stops
  - Fault timer
  - 160 ms

- **Fault timer**
  - t\_{OVLD}
  - t\_{restart}
  - t\_{delay(start)}
Abnormal Overcurrent Protection (AOCP)

Under some severe fault conditions, like a winding short-circuit, the switch current can increase very rapidly during the on-time. The current sense signal significantly exceeds \( V_{ILIM1} \), but because the current sense signal is blanked by the LEB circuit during the switch turn-on, the power switch current can become huge and cause severe system damage.

The NCP1342 protects against this fault by adding an additional comparator for Abnormal Overcurrent Fault detection. The current sense signal is blanked with a shorter LEB duration, \( t_{LEB2} \), typically 125 ns, before applying it to the Abnormal Overcurrent Fault Comparator. The voltage threshold of the comparator, \( V_{ILIM2} \), typically 1.2 V, is set 50% higher than \( V_{ILIM1} \), to avoid interference with normal operation. Four consecutive Abnormal Overcurrent faults cause the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Fault Overcurrent Comparator.

Current Sense Pin Failure Protection

A 1 \( \mu \)A (typically) pull-up current source, \( I_{CS} \), pulls up the CS pin to disable the controller if the pin is left open.

Additionally, the maximum on-time, \( t_{on\text{(MAX)}} \) (32 \( \mu \)s typically), prevents the MOSFET from staying on permanently if the CS Pin is shorted to GND.

Output Short Circuit Protection

During an output short-circuit, there is not enough voltage across the secondary winding to demagnetize the core. Due to the valley timeout feature of the controller, the flux level will quickly walk up until the core saturates. This can cause excessive stress on the primary MOSFET and secondary diode. This is not a problem for the NCP1342, however, because the valley timeout timer is disabled while the ZCD Pin voltage is above the arming threshold. Since the leakage energy is high enough to arm the ZCD trigger, the timeout timer is disabled and the next drive pulse is delayed until demagnetization occurs.

\( V_{CC} \) Overvoltage Protection

An additional comparator on the \( V_{CC} \) pin monitors the \( V_{CC} \) voltage. If \( V_{CC} \) exceeds \( V_{CC\text{(OVP)}} \), the gate drive is disabled and the NCP1342 follows the operation of a latching fault (see Figure 17).

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the controller. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, \( T_{SHDN} \) (typically 140°C). When a thermal shutdown fault is detected, the controller enters a non-latching fault mode as depicted in Figure 18. The controller restarts at the next \( V_{CC\text{(on)}} \) once the junction temperature drops below the thermal shutdown hysteresis, \( T_{SHDN\text{(HYS)}} \), typically 40°C.

The thermal shutdown is also cleared if \( V_{CC} \) drops below \( V_{CC\text{(reset)}} \), or a line removal fault is detected. A new power up sequence commences at the next \( V_{CC\text{(on)}} \) once all the faults are removed.
TYPICAL CHARACTERISTICS

Figure 27. $V_{CC(on)}$ vs. Temperature

Figure 28. $V_{CC(\text{off})}$ vs. Temperature

Figure 29. $I_{\text{start1}}$ vs. Temperature

Figure 30. $I_{\text{start2}}$ vs. Temperature

Figure 31. $I_{HV(\text{off1})}$ vs. Temperature

Figure 32. $I_{HV(\text{off2})}$ vs. Temperature
TYPICAL CHARACTERISTICS

Figure 33. $I_{CC1}$ vs. Temperature

Figure 34. $I_{CC2}$ vs. Temperature

Figure 35. $I_{CC3}$ vs. Temperature

Figure 36. $V_{CC(OVP)}$ vs. Temperature

Figure 37. $I_{CC\text{(discharge)}}$ vs. Temperature

Figure 38. $V_{BO\text{(start)}}$ vs. Temperature
TYPICAL CHARACTERISTICS

Figure 39. $V_{BO(\text{stop})}$ vs. Temperature

Figure 40. $t_{DRV(\text{rise})}$ vs. Temperature

Figure 41. $t_{DRV(\text{fall})}$ vs. Temperature

Figure 42. $f_{\text{MAX1}}$ vs. Temperature

Figure 43. $f_{\text{MAX2}}$ vs. Temperature

Figure 44. $f_{\text{MAX3}}$ vs. Temperature
TYPICAL CHARACTERISTICS

Figure 45. $t_{\text{on(MAX)}}$ vs. Temperature

Figure 46. $V_{\text{ZCD(trig)}}$ vs. Temperature

Figure 47. $V_{\text{ZCD(HYS)}}$ vs. Temperature

Figure 48. $V_{\text{ZCD(MAX)}}$ vs. Temperature

Figure 49. $V_{\text{ZCD(MIN)}}$ vs. Temperature

Figure 50. $V_{\text{freeze}}$ vs. Temperature
TYPICAL CHARACTERISTICS

Figure 51. $f_{\text{jitter}}$ vs. Temperature

Figure 52. $V_{\text{jitter}}$ vs. Temperature

Figure 53. $V_{\text{Fault(OVP)}}$ vs. Temperature

Figure 54. $V_{\text{Fault(OTP\_in)}}$ vs. Temperature

Figure 55. $V_{\text{Fault(OTP\_out)}}$ vs. Temperature

Figure 56. $I_{\text{OTP}}$ vs. Temperature
TYPICAL CHARACTERISTICS

Figure 57. $V_{\text{Fault(clamp)}}$ vs. Temperature

Figure 58. $R_{\text{Fault(clamp)}}$ vs. Temperature

Figure 59. $f_{\text{MIN}}$ vs. Temperature

Figure 60. $t_{\text{quiet}}$ vs. Temperature

Figure 61. $t_{\text{ZCD(blank)}}$ vs. Temperature

Figure 62. $V_{\text{ILIM1}}$ vs. Temperature
**Typical Characteristics**

**Figure 63.** $V_{ILM2}$ vs. Temperature

**Figure 64.** $t_{DT(MAX)}$ vs. Temperature

**Figure 65.** $V_{skip}$ vs. Temperature
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2
**SOIC–8 NB**  
**CASE 751–07**  
**ISSUE AK**

**DOCUMENT NUMBER:** 98ASB42564B  
**DESCRIPTION:** SOIC–8 NB  
**DATE:** 16 FEB 2011  
**Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.**

---

### Style 1

**PIN 1. Emitter**  
2. Collector  
3. Collector, #1  
4. Collector  
5. Collector, #1  
6. Base  
7. Base  
8. Emitter  

### Style 2

**PIN 1. Collector, Die, #1**  
2. Collector, #1  
3. Collector, #2  
4. Collector, #1  
5. Emitter, #1  
6. Base, #2  
7. Base, #2  
8. Emitter, #1  

### Style 3

**PIN 1. Drain, Die #1**  
2. Drain, Die #1  
3. Drain, #2  
4. Drain, #2  
5. Gate, #2  
6. Source, #2  
7. Gate, #1  
8. Source, #1  

### Style 4

**PIN 1. Anode**  
2. Base, Die #1  
3. Anode  
4. Source  
5. Collector, #2  
6. Anode  
7. Collector, #2  
8. Common Cathode  

### Style 5

**PIN 1. Drain**  
2. Drain  
3. Drain  
4. Drain  
5. Gate  
6. Gate  
7. Source  
8. Source  

### Style 6

**PIN 1. Source**  
2. External Bypass  
3. Third Stage Source  
4. Ground  
5. Collector, Die #2  
6. Emitter, #2  
7. Source  
8. First Stage Vd  

### Style 7

**PIN 1. Input**  
2. Base, Die #1  
3. Base, #1  
4. Collector, #2  
5. Collector, Die #2  
6. Emitter, #2  
7. Collector, #1  
8. Collector, #1  

### Style 8

**PIN 1. Collector, Die #1**  
2. Collector, Die #1  
3. Collector, Die #2  
4. Collector, #2  
5. Collector, #2  
6. Collector, #2  
7. Collector, #2  
8. Collector, #2  

### Style 9

**PIN 1. Emitter, Common**  
2. Collector, Die #1  
3. Collector, Die #2  
4. Collector, Common  
5. Emitter, Common  
6. Base, Die #2  
7. Base, Die #1  
8. Emitter, Common  

### Style 10

**PIN 1. Ground**  
2. Bias 1  
3. Output  
4. Ground  
5. Ground  
6. Bias 2  
7. Input  
8. Drain  

### Style 11

**PIN 1. Source 1**  
2. Gate 1  
3. Source 2  
4. Gate 2  
5. Drain 2  
6. Drain 2  
7. Drain 1  
8. Drain 1  

### Style 12

**PIN 1. Source**  
2. Base  
3. Source  
4. Gate  
5. Drain  
6. Drain  
7. Drain  
8. Drain  

### Style 13

**PIN 1. N.C.**  
2. Source  
3. Source  
4. Gate  
5. Drain  
6. Drain  
7. Drain  
8. Drain  

### Style 14

**PIN 1. N-Source**  
2. Source  
3. P-Source  
4. P-Gate  
5. P-Drain  
6. P-Drain  
7. N-Drain  
8. N-Drain  

### Style 15

**PIN 1. Anode 1**  
2. Anode 1  
3. Anode 1  
4. Anode 1  
5. Cathode, Common  
6. Cathode, Common  
7. Cathode, Common  
8. Cathode, Common  

### Style 16

**PIN 1. Emitter, Die #1**  
2. Base, Die #1  
3. Emitter, Die #2  
4. Base, #2  
5. Collector, Die #2  
6. Collector, Die #2  
7. Collector, Die #1  
8. Collector, Die #1  

### Style 17

**PIN 1. Vcc**  
2. VINOUT  
3. VIOUT  
4. Txe  
5. RXE  
6. Vee  
7. Gnd  
8. Acc  

### Style 18

**PIN 1. Anode**  
2. Anode  
3. Anode  
4. Anode  
5. Cathode  
6. Cathode  
7. Cathode  
8. Cathode  

### Style 19

**PIN 1. Source 1**  
2. Gate 1  
3. Source 2  
4. Gate 2  
5. Drain 2  
6. Drain 2  
7. Drain 1  
8. Drain 1  

### Style 20

**PIN 1. Source**  
2. Gate (N)  
3. Source (P)  
4. Gate (P)  
5. Drain  
6. Drain  
7. Drain  
8. Drain  

### Style 21

**PIN 1. Cathode 1**  
2. Cathode 2  
3. Cathode 3  
4. Cathode 4  
5. Cathode 5  
6. Common Anode  
7. Common Anode  
8. Common Anode  

### Style 22

**PIN 1. IO Line 1**  
2. Common Cathode/VCC  
3. Common Cathode/VCC  
4. IO Line 3  
5. Common Anode/GND  
6. IO Line 4  
7. Common Anode/GND  
8. Common Anode/GND  

### Style 23

**PIN 1. Line 1 In**  
2. Common Anode/Gnd  
3. Common Anode/Gnd  
4. Line 2 In  
5. Line 2 Out  
6. Common Anode/Gnd  
7. Common Anode/Gnd  
8. Line 1 Out  

### Style 24

**PIN 1. Base**  
2. Emitter  
3. Collector/Anode  
4. Collector/Anode  
5. Cathode  
6. Cathode  
7. Collector/Anode  
8. Collector/Anode  

### Style 25

**PIN 1. Vin**  
2. Nc  
3. Rext  
4. Gnd  
5. Iout  
6. Iout  
7. Iout  
8. Iout  

### Style 26

**PIN 1. Gnd**  
2. Gnd  
3. Gnd  
4. Source  
5. Source  
6. Source  
7. Source  
8. Drain  

### Style 27

**PIN 1. Ilimit**  
2. Input  
3. Source  
4. Source  
5. Source  
6. Source  
7. Source  
8. Drain  

### Style 28

**PIN 1. Sw_to_Gnd**  
2. Dasic_off  
3. Dasic_sw_det  
4. Gnd  
5. V_mon  
6. Vbulk  
7. Vbulk  
8. Vbulk
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−9 NB
CASE 751BP
ISSUE A

DATE 21 NOV 2011

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

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3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

SCALE 1:1

TOP VIEW

SIDE VIEW

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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