NCP1027

High-Voltage Switcher for Medium Power Offline SMPS Featuring Low Standby Power

The NCP1027 offers a new solution targeting output power levels from a few watts up to 15 W in a universal mains flyback application. Our proprietary high-voltage technology lets us include a power MOSFET together with a startup current source, all directly connected to the bulk capacitor. To prevent lethal runaway in low input voltage conditions, an adjustable brown-out circuitry blocks the activity until sufficient input level is reached.

Current-mode operation together with an adjustable ramp compensation offers superior performance in universal mains applications. Furthermore, an Over Power Protection pin brings the ability to precisely compensate all internal delays in high input voltage conditions and optimize the maximum output current capability.

Protection wise, a timer detects an overload or a short-circuit and stops all operations, ensuring a safe auto-recovery, low duty cycle burst operation. An integrated, auto-recovery, Overvoltage Protection permanently monitors the VCC level and temporarily shuts down the driving pulses in case of an unexpected feedback loop runaway.

Finally, a great R_{DS(on)} figure makes the circuit an excellent choice for standby/auxiliary offline power supplies or applications requiring higher output power levels.

Features
- Built-in 700 V MOSFET with Typical R_{DS(on)} of 5.8 Ω, T_J = 25°C
- Current-Mode Fixed Frequency Operation: 65 kHz and 100 kHz
- Fixed Peak Current of 800 mA
- Skip-Cycle Operation at Low Peak Currents
- Internal Current Source for Clean and Lossless Startup Sequence
- Auto-Recovery Output Short Circuit Protection with Timer-Based Detection
- Auto-Recovery Overvoltage Protection with Auxiliary Winding Operation
- Programmable Brown-Out Input for Low Input Voltage Detection
- Programmable Over Power Protection
- Input to Permanently Latchoff the Part
- Internal Frequency Jittering for Improved EMI Signature
- Extended Duty Cycle Operation to 80% Typical
- No-Load Input Standby Power of 85 mW @ 265 Vac
- 500 mW Loaded, Input Power of 715 mW @ 230 Vac
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications
- Medium Power AC–DC Adapters for Chargers
- Auxiliary/Standby Power Supplies for ATX and TVS Power Supplies

<table>
<thead>
<tr>
<th>Reference</th>
<th>230 VAC</th>
<th>90–265 VAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1027</td>
<td>25 W*</td>
<td>15 W*</td>
</tr>
</tbody>
</table>

*Typical values, open-frame, 65 kHz version, R_{UA} < 75°C/W, T_A = 50°C.
PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Powers the Internal Circuitry</td>
<td>This pin is connected to an external capacitor of typically 22 µF. The VCC includes an active shunt which serves as an auto-recovery overvoltage protection.</td>
</tr>
<tr>
<td>2</td>
<td>Ramp Comp.</td>
<td>Ramp Compensation in CCM</td>
<td>To extend the duty cycle operation in Continuous Conduction Mode (CCM), pin 3 offers the ability to inject ramp compensation in the controller. If unused, short this pin to VCC.</td>
</tr>
<tr>
<td>3</td>
<td>Brown–Out</td>
<td>Brown–Out and Latchoff Input</td>
<td>By monitoring the bulk level via a resistive network, the circuit protects itself from low mains conditions. If an external event brings this pin above 4.0 V, the part fully latches off.</td>
</tr>
<tr>
<td>4</td>
<td>FB</td>
<td>Feedback Signal Input</td>
<td>By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.</td>
</tr>
<tr>
<td>5</td>
<td>Drain</td>
<td>Drain Connection</td>
<td>The internal drain power switch circuit connection.</td>
</tr>
<tr>
<td></td>
<td>–</td>
<td>–</td>
<td>This unconnected pin ensures adequate creepage distance.</td>
</tr>
<tr>
<td>7</td>
<td>OPP</td>
<td>Over Power Protection</td>
<td>Driving this pin reduces the power supply capability in high line conditions. If no Over Power Protection is needed, short this pin to ground.</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>The IC Ground</td>
<td>–</td>
</tr>
</tbody>
</table>
Figure 2. Internal Block Diagram
MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage on all Pins, Except Pin 5 (Drain)</td>
<td>VCC</td>
<td>−0.3 to 10</td>
<td>V</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>BVdss</td>
<td>−0.3 to 700</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current Peak During Transformer Saturation</td>
<td>IDS(pk)</td>
<td>1.8</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Current into Pin 1 when Activating the 8.7 V Active Clamp</td>
<td>I_VCC</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal Resistance, Junction−to−Air – PDIP7</td>
<td>R_JUA</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction−to−Air – PDIP7 with 1.0 cm² of 35 µ Copper Area</td>
<td>R_JUA</td>
<td>75</td>
<td>°C/W</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>TJMAX</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td>−60 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Human Body Model (HBM) (All Pins Except HV)</td>
<td></td>
<td>2.0</td>
<td>kV</td>
</tr>
<tr>
<td>ESD Capability, Machine Model (MM)</td>
<td></td>
<td>200</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC JESD22−A114−F.
   Machine Model Method 200 V per JEDEC JESD22−A115−A.

2. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (For typical values TJ = 25°C, for min/max values TJ = 0°C to +125°C, Max TJ = 150°C, VCC = 8.0 V, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Pin</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUPPLY SECTION AND VCC MANAGEMENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>VCC Increasing Level at which the Switcher Starts to Operate</td>
<td>1</td>
<td>VCCON</td>
<td>7.9</td>
<td>8.5</td>
<td>8.9</td>
<td>V</td>
</tr>
<tr>
<td>VCC Decreasing Level at which the Switcher Stops Operation</td>
<td>1</td>
<td>VCC(min)</td>
<td>6.7</td>
<td>7.2</td>
<td>7.9</td>
<td>V</td>
</tr>
<tr>
<td>Hysteresis between VCCON and VCC(min)</td>
<td>–</td>
<td>VCChystee</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Offset Voltage above VCCON at which the Internal Clamp Activates</td>
<td>1</td>
<td>VCCclamp</td>
<td>140</td>
<td>200</td>
<td>300</td>
<td>mV</td>
</tr>
<tr>
<td>VCC Voltage at which the Internal Latch is Reset</td>
<td>1</td>
<td>VCCreset</td>
<td>–</td>
<td>4.0</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Internal IC Consumption, MOSFET Switching at 65 kHz or 100 kHz</td>
<td>1</td>
<td>ICC1</td>
<td>–</td>
<td>1.4</td>
<td>1.9</td>
<td>mA</td>
</tr>
</tbody>
</table>

POWER SWITCH CIRCUIT

<table>
<thead>
<tr>
<th>Characteristic</th>
<th></th>
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<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Power Switch Circuit On−State Resistance NCP1027 (Id = 100 mA)</td>
<td>5</td>
<td>RDS(on)</td>
<td>–</td>
<td>5.8</td>
<td>7.0</td>
<td>Ω</td>
</tr>
<tr>
<td>TJ = 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ = 125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Switch Circuit and Startup Breakdown Voltage (ID(off) = 120 µA, TJ = 25°C)</td>
<td>5</td>
<td>BVdss</td>
<td>700</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>TJ = 25°C (Vds = 700 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ = 125°C (Vds = 700 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Switch and Startup Breakdown Voltage Off−State Leakage Current</td>
<td>5</td>
<td>Idss(OFF)</td>
<td>–</td>
<td>50</td>
<td>–</td>
<td>µA</td>
</tr>
<tr>
<td>TJ = 25°C (Vds = 700 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ = 125°C (Vds = 700 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Characteristics (RL = 50 Ω, Vds Set for Idrain = 0.7 x Ilim)</td>
<td>5</td>
<td>t_on</td>
<td>–</td>
<td>35</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Turn−on Time (90%−10%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn−off Time (10%−90%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</table>

INTERNAL STARTUP CURRENT SOURCE

<table>
<thead>
<tr>
<th>Characteristic</th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>High−Voltage Current Source, VCC = VCCON − 200 mV</td>
<td>1</td>
<td>IC1</td>
<td>3.5</td>
<td>6.0</td>
<td>8.0</td>
<td>mA</td>
</tr>
<tr>
<td>High−Voltage Current Source, VCC = 0</td>
<td>1</td>
<td>IC2</td>
<td>350</td>
<td>650</td>
<td>900</td>
<td>µA</td>
</tr>
<tr>
<td>VCC Transition Level for IC1 to IC2 Toggling Point</td>
<td>1</td>
<td>VCTTh</td>
<td>–</td>
<td>1.3</td>
<td>–</td>
<td>V</td>
</tr>
</tbody>
</table>
## ELECTRICAL CHARACTERISTICS (continued)
(For typical values $T_J = 25^\circ C$, for min/max values $T_J = 0^\circ C$ to $+125^\circ C$,
Max $T_J = 150^\circ C$, $V_{CC} = 8.0$ V, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Pin</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CURRENT COMPARATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Internal Current Setpoint, Pin 4 Open, $T_J = 25^\circ C$, $F_{SW} = 65$ kHz (Note 3)</td>
<td>–</td>
<td>$I_{peak_27_CS_65_k}$</td>
<td>720</td>
<td>800</td>
<td>880</td>
<td>mA</td>
</tr>
<tr>
<td>Final Switch Current with a Primary Slope of 200 mA/$\mu$s, $F_{SW} = 65$ kHz (Note 4)</td>
<td>–</td>
<td>$I_{peak_27_SW_65_k}$</td>
<td>–</td>
<td>820</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum Internal Current Setpoint, Pin 4 Open, $T_J = 25^\circ C$, $F_{SW} = 100$ kHz (Note 3)</td>
<td>–</td>
<td>$I_{peak_27_CS_100_k}$</td>
<td>720</td>
<td>800</td>
<td>880</td>
<td>mA</td>
</tr>
<tr>
<td>Final Switch Current with a Primary Slope of 200 mA/$\mu$s, $F_{SW} = 100$ kHz (Note 4)</td>
<td>–</td>
<td>$I_{peak_27_SW_100_k}$</td>
<td>–</td>
<td>820</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Setpoint Decrease for a Pin 7 Injected Current of 40 $\mu$A, $T_J = 25^\circ C$</td>
<td>7</td>
<td>$I_{OPP}$</td>
<td>–</td>
<td>23</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Voltage Level in Pin 7 at which OPP Starts to Operate</td>
<td>7</td>
<td>$I_{OPPtripV}$</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Soft–Start Duration</td>
<td>–</td>
<td>$T_{SS}$</td>
<td>–</td>
<td>1.0</td>
<td>–</td>
<td>ms</td>
</tr>
<tr>
<td>Propagation Delay from Current Detection to Drain OFF State</td>
<td>–</td>
<td>$T_{prop}$</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Leading Edge Blanking Duration</td>
<td>–</td>
<td>$T_{LEB}$</td>
<td>–</td>
<td>200</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>INTERNAL OSCILLATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillation Frequency (Note 5) $65$ kHz Version, $T_J = 25^\circ C$</td>
<td>–</td>
<td>$f_{OSC}$</td>
<td>58.5</td>
<td>65</td>
<td>71.5</td>
<td>kHz</td>
</tr>
<tr>
<td>Oscillation Frequency (Note 5) $100$ kHz Version, $T_J = 25^\circ C$</td>
<td>–</td>
<td>$f_{OSC}$</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency Jittering in Percentage of $f_{OSC}$</td>
<td>–</td>
<td>$f_{jitter}$</td>
<td>–</td>
<td>±6.0</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Jittering Swing Frequency</td>
<td>–</td>
<td>$f_{swing}$</td>
<td>–</td>
<td>300</td>
<td>–</td>
<td>Hz</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>–</td>
<td>$D_{max}$</td>
<td>74</td>
<td>80</td>
<td>87</td>
<td>%</td>
</tr>
<tr>
<td>FEEDBACK SECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Pullup Resistor</td>
<td>4</td>
<td>$R_{up}$</td>
<td>–</td>
<td>16</td>
<td>–</td>
<td>kΩ</td>
</tr>
<tr>
<td>Ramp Compensation Level on Pin 1 – $R_{ramp} = 100$ kΩ</td>
<td>2</td>
<td>$R_{level}$</td>
<td>–</td>
<td>2.75</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>SKIP CYCLE GENERATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Skip Mode Level, in Percentage of Maximum Peak Current</td>
<td>–</td>
<td>$I_{skip}$</td>
<td>–</td>
<td>25</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>PROTECTIONS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Brown–Out Level</td>
<td>3</td>
<td>$V_{BO}$</td>
<td>510</td>
<td>570</td>
<td>620</td>
<td>mV</td>
</tr>
<tr>
<td>Brown–Out Hysteresis Current, $T_J = 25^\circ C$ (Note 3)</td>
<td>3</td>
<td>$I_{BOhyste}$</td>
<td>10</td>
<td>11.5</td>
<td>13</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>Brown–Out Hysteresis Current, $T_J = 0^\circ C$ to 125$^\circ C$</td>
<td>3</td>
<td>$I_{BOhyste}$</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>Fault Validation Further to Error Flag Assertion</td>
<td>–</td>
<td>$T_{on}$</td>
<td>40</td>
<td>55</td>
<td>–</td>
<td>ms</td>
</tr>
<tr>
<td>OFF Phase in Fault Mode</td>
<td>–</td>
<td>$T_{OFF}$</td>
<td>–</td>
<td>440</td>
<td>–</td>
<td>ms</td>
</tr>
<tr>
<td>Latching Voltage on Brown–Out Pin</td>
<td>3</td>
<td>$V_{latch}$</td>
<td>3.15</td>
<td>3.5</td>
<td>3.85</td>
<td>V</td>
</tr>
<tr>
<td>Latch Input Integrating Filter Time Constant</td>
<td>3</td>
<td>$T_{delBOL}$</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>OVP Integrating Filter Time Constant</td>
<td>–</td>
<td>$T_{delOVP}$</td>
<td>–</td>
<td>50</td>
<td>–</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$V_{CC}$ Current at which the Switcher Stops Pulsing</td>
<td>1</td>
<td>$IOVP$</td>
<td>6.0</td>
<td>8.5</td>
<td>11</td>
<td>mA</td>
</tr>
<tr>
<td>TEMPERATURE MANAGEMENT</td>
<td></td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Temperature Shutdown</td>
<td>–</td>
<td>$T_{SD}$</td>
<td>160</td>
<td>–</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>Hysteresis in Shutdown</td>
<td>–</td>
<td>–</td>
<td>40</td>
<td>–</td>
<td>–</td>
<td>°C</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. See characterization curves for full temperature span evolution.
4. The final switch current is: $I_{peak\_2X\_CS} + T_{prop} \times V_{in} / L_{p}$, with $V_{in}$ the input voltage and $L_{p}$ the primary inductor in a flyback.
5. Oscillator frequency is measured with disabled jittering.
NCP1027

TYPICAL CHARACTERISTICS

Figure 15.

Figure 16.

Figure 17.

Figure 18.

Figure 19.

Figure 20.
TYPICAL CHARACTERISTICS

Figure 21.

Figure 22.

Figure 23. $I_{\text{peak}} \text{Reduction} = F(I_{\text{opp}}, \text{@ temperature})$
**Introduction**

The NCP1027 offers a complete current-mode control solution and enhances the NCP101X series. The component integrates everything needed to build a rugged and low-cost Switch-Mode Power Supply (SMPS) featuring low standby power.

- **Current-Mode Operation:** The controller uses a current-mode control architecture, which, together with an adjustable ramp compensation circuitry, ensures efficient and stable continuous or discontinuous conduction designs.
- **700 V–5.8 Ω Power Switch Circuit:** Due to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high-voltage power switch circuit featuring a 5.8 Ω $R_{DS(on)}$ – $T_J = 25°C$. This value lets the designer build a 15 W power supply operated on universal mains as long as sufficient copper area exists to lower the junction-to-ambient thermal resistance. An internal current source delivers the startup current, necessary to crank the power supply.
- **Short-Circuit Protection:** By permanently monitoring the feedback line activity, the circuit is able to detect the presence of a short-circuit, immediately reducing the output power for a total system protection. A 55 ms timer is started as soon as the feedback pin asks for the maximum peak current. At the end of this timer, if the fault is still present, then the device enters a safe, auto-recovery burst mode, affected by a fixed 440 ms recurrence. Once the short has disappeared, the controller resumes and goes back to normal operation. The timer duration is fully independent from the $V_{CC}$ capacitor value.
- **Over Power Protection:** A possibility exists to reduce the maximum output power capability in high line conditions. A simple two resistor network wired to the bulk capacitor will program the maximum current reduction for a given input voltage (down to 20% of the maximum peak current).
- **Fail-Safe Optocoupler/Overvoltage Protection:** As the auxiliary winding is connected to the $V_{CC}$ pin, an internal active clamp connected between $V_{CC}$ and ground limits the supply dynamics to 8.7 V. In case the current injected in this clamp exceeds a level of 6.0 mA (minimum), the controller immediately stops switching and waits a full timer period before attempting to restart. If the default is gone, the controller resumes operation. If the default is still there, e.g. a broken optocoupler, the controller protects the load through a safe burst mode.
- **Brown-Out Input:** A fraction of the input voltage appears on pin 3, due to a resistive divider. If the mains drops below a level adjusted by this resistive divider, the circuit does not switch. As soon as the mains goes back within its normal range, the device resumes operation and operates normally. By adjusting the bridge resistors, it becomes possible to set the brown-out levels (on and off) independently.
- **Latchoff:** Pin 3 also welcomes a comparator who offers a way to fully latch the controller. If an external event (e.g. an overtemperature) brings the brown-out pin above 3.5 V, the circuit stays permanently off until the user cycles its $V_{CC}$ down, for instance by unplugging the converter from the mains outlet.
- **Frequency Jittering:** The internal clock receives a low frequency modulation which helps smoothing the power supply EMI signature.
- **Soft-Start:** A 1.0 ms soft-start ensures a smooth startup sequence, reducing output overshoots.
- **Skip Cycle:** If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP1027 drastically reduces the power wasted during light load conditions. Experiments carried over the 5.0 V/2.0 A demonstration board reveal a standby power at no-load and 265 Vac of 85 mW and an efficiency for 500 mW output power of 64% at 230 Vac.
Startup Sequence

The NCP1027 includes a high-voltage startup circuitry, directly deriving current from the bulk line to charge the VCC capacitor. Figure 24 details the simplified internal arrangement.

When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the VCC capacitor. When the voltage on this VCC capacitor reaches the VCCON level (typically 8.5 V), the current source turns off, reducing the amount of power being dissipated. At this time, the VCC capacitor only supplies the controller, and the auxiliary supply should take over before VCC collapses below VCC(min). This VCC capacitor, CVCC, must therefore be calculated to hold enough energy so that VCC stays above VCC(min) (7.3 V typical) until the auxiliary voltage fully takes over.

An auxiliary winding is needed to maintain the VCC in order to self-supply the switcher. The VCC capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see in Figure 24, an internal active Zener diode, protects the switcher against lethal VCC runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the internal current increase incurred by the VCC rapid growth triggers the over voltage protection (OVP) circuit and immediately stops the output pulses for 440 ms. Then a new startup attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

The VCC capacitor can be calculated knowing a) the amount of energy that needs to be stored; b) the time it takes for the auxiliary voltage to appear; and c) the current consumed by the controller at that time. For a better understanding, Figure 25 shows how the voltage evolves on the VCC capacitor upon startup.
Figure 25. A typical startup sequence showing the V\textsubscript{CC} capacitor voltage evolution versus time.

Suppose our power supply takes 10 ms (t\textsubscript{startup}) to bring the output voltage to its target value. We know that the switcher consumption is around 2.0 mA (I\textsubscript{C1}). Therefore, we can calculate the amount of capacitance we need, to hold V\textsubscript{CC} above 7.5 V at least for 10 ms while delivering 2.0 mA:

\[ C \geq \frac{I\textsubscript{C1}t\textsubscript{startup}}{\Delta V\textsubscript{CC}} \]

or, by replacing with the above values,

\[ C \geq \frac{2\text{mA} \times 10\text{ms}}{20\text{mV}} \geq 20 \mu\text{F} \]

then select a 33 \( \mu \text{F} \) for the V\textsubscript{CC} capacitor.

Fault Condition – Short−Circuit on V\textsubscript{CC}

In some fault situations, a short−circuit can purposely occur between V\textsubscript{CC} and GND. In high line conditions (V\textsubscript{HV} = 370 V\textsubscript{DC}) the current delivered by the startup device will seriously increase the junction temperature. For instance, since IC1 equals 3.0 mA (the min corresponds to the highest T\textsubscript{j}), the device would dissipate 370 \( \times \) 3 m = 1.1 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, IC1 and IC2. At powerup, as long as V\textsubscript{CC} is below a 1.3 V level, the source delivers IC1 (around 650 \( \mu \text{A} \) typical), then, when V\textsubscript{CC} reaches 1.3 V, the source smoothly transitions to IC2 and delivers its nominal value. As a result, in case of short−circuit between V\textsubscript{CC} and GND, the power dissipation will drop to 370 \( \times \) 650 \( \mu \text{W} \) = 240 mW. Figure 26 portrays this particular behavior.

The first startup period is calculated by the formula C \( \times \) V = I \( \times \) t, which implies a 33 \( \mu \text{F} \) \( \times \) 1.3/650 \( \mu \text{F} \) = 66 ms startup time for the first sequence (t1). The second sequence (t2) is obtained by toggling the source to 4.0 mA with a delta V of V\textsubscript{CCON} − V\textsubscript{Vth} = 8.5 − 1.5 = 7.0 V, which finally leads to a second startup time of 7 \( \times \) 33 \( \mu \text{F} \)/6.0 m = 39 ms. The total startup time becomes 66 m + 39 m = 105 ms as a typical value. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.
Fault Condition – Output Short-Circuit

As soon as VCC reaches VCC_ON, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the VCC pin as the output voltage rises. During the start-sequence, the controller smoothly ramps up the peak current to Imax setting, e.g. Ipeak_HI, which is reached after a typical period of 1.0 ms. As soon as the peak current setpoint reaches its maximum (during the startup period but also anytime an overload occurs), an internal error flag is asserted, Ipflag, indicating that the system has reached its maximum current limit set point (Ip = Ip max). The assertion of this flag triggers a 55 ms counter. If at counter completion Ipflag remains asserted, all driving pulses are stopped and the part stays off during eight periods of 55 ms (440 ms). A new attempt to restart occurs and will last 55 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty-cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 27 depicts this particular mode.

![Figure 27. In case of short-circuit or overload, the NCP1027 protects itself and the power supply via a low frequency burst mode. The VCC is maintained by the current source and self-supplies the controller.](image-url)
In Figure 27, one can see that the $V_{CC}$ is still alive, testifying for a badly coupled power secondary and primary auxiliary windings. Some situations exist where an output short-circuit make the auxiliary winding collapse before the timer completion. In this particular case, the Undervoltage Lock Out (UVLO) circuitry has the priority and safely cuts off all driving pulses. Figure 28 describes this variation.

Figure 28. The auxiliary winding collapses in presence of a short-circuit. Pulses are immediately stopped as $V_{CC}$ crosses the minimum operating voltage, $V_{CC_{\text{min}}}$.
Fault Condition – Output Too Low

This particular mode of operation occurs when the feedback is ensured by a two-loop control imposing either constant output voltage (CV) or constant output current (CC), for instance in a battery charger. In CC mode, the output voltage falls down below the original target but the feedback loop is kept closed by the CC controller. For that reason, the controller becomes unable to detect a real output short-circuit since Ipflag will never be asserted. Due to a good winding coupling, the primary side auxiliary collapsing will ensure a proper fault detection via the UVLO internal circuit. Figure 29 depicts this operating way.

![Diagram](image)

**Figure 29.** In this particular case, the output goes low but the timer is not started since the FB pin is still held by the optocoupler. Due to the UVLO circuit, the controller safely stops operation at $V_{CC} = V_{CC(min)}$. 

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Fault Condition – Low Input Voltage

The NCP1027 includes a brown−out circuitry able to protect the power supply in case of low input voltage conditions. Figure 30 shows how internally the NCP1027 monitors the voltage image of the bulk capacitor. Below a given level, the controller blocks the driving pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 30a, offers a way to observe the high−voltage (HV) rail. A resistive divider made of $R_{upper}$ and $R_{lower}$, brings a portion of the HV rail on pin 3. Below the turn−on level, the 10 $\mu$A current source $IBO$ is off. Therefore, the turn−on level solely depends on the division ratio brought by the resistive divider.

![Figure 30a. The internal brown−out configuration with an offset current source.](image1)

![Figure 30b. Simulation results for 100/70 ON/OFF levels.](image2)

![Figure 30.](image3)

To the contrary, when the internal BO signal is high, the $IBO$ source is activated and creates an hysteresis. As a result, it becomes possible to select the turn−on and turn−off levels via a few lines of algebra.

**$IBO$ is Off**

$$V(+) = V_{bulk1} \times \frac{R_{lower}}{R_{lower} + R_{upper}}$$  \hspace{1cm} (eq. 1)

**$IBO$ is On**

$$V(+) = V_{bulk2} \times \frac{R_{lower}}{R_{lower} + R_{upper}} + IBO \times \left(\frac{R_{lower} \times R_{upper}}{R_{lower} + R_{upper}}\right)$$  \hspace{1cm} (eq. 2)

We can now extract $R_{lower}$ from Equation 1 and plug it into Equation 2, then solve for $R_{upper}$:

$$R_{upper} = R_{lower} \times \frac{V_{bulk1} − V_{BO}}{V_{BO}}$$

$$R_{lower} = V_{BO} \times \frac{V_{bulk1} − V_{bulk2}}{IBO \times (V_{bulk1} − V_{BO})}$$

If we decide to turn−on our converter for $V_{bulk1}$ equals 100 V and turn it off for $V_{bulk2}$ equals 70 V, then we obtain:

$R_{upper} = 3.0 \text{ M}$Ω

$R_{lower} = 18 \text{ k}$Ω
The bridge power dissipation is $330\frac{2}{3}\times3.018\text{ Meg} = 36\text{ mW}$ in nominal high–line operation. Figure 30b simulation result confirms our calculations.

Figure 31 describes signal variations during a brown–out condition. Please note that output pulses only reappear when $V_{CC}$ reaches $V_{CC(ON)}$, ensuring a clean startup sequence. As in fault mode conditions, the startup source is activated on and off and self–supplies the controller in a Dynamic Self–Supply (DSS) mode.

![Figure 31. Signal Evolution During a Brown–Out Condition](image)

Depending on input surge tests, it might be necessary to wire a filtering capacitor between BO and GND (close to the circuit) to avoid adversely triggering the internal latch (unless this is a wanted feature) when the pulse train appears.

**Latchoff Protection**

There are some situations where the converter shall be fully turned–off and stay latched. This can happen in the presence of a secondary overvoltage (the feedback loop is drifting) or when an overtemperature is detected. Secondary monitoring is usually implemented when the coupling between auxiliary and power windings does not lead to a precise primary detection, hence the auto–recovery OVP on pin 1 would not satisfy the precision requirements. Due to the addition of a comparator on the BO pin, a simple external circuit can lift up this pin above $V_{LATCH}$ and permanently disable pulses. The $V_{CC}$ needs to be cycled down below 3.5 V typically to reset the controller.
In Figure 32, Q1 is blocked and does not bother the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses an OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is brought to ground and the BO pin goes up, permanently latching off the controller. Figure 33 depicts the converter behavior in case of total latch-off.

Figure 33. If the BO pin is lifted up to VLATCH, the controller permanently latches off.
**Auto-Recovery Overvoltage Protection**

The particular NCP1027 arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 34 shows, an active Zener diode monitors and protects the VCC pin. Below its equivalent breakdown voltage, that is to say 8.7 V typical, no current flows in it. If the auxiliary VCC pushes too much current inside the Zener, then the controller considers an OVP situation and stops the pulses. Figure 34 shows that the insertion of a resistor \( R_{\text{limit}} \) between the auxiliary DC level and the VCC pin is mandatory a) not to damage the internal 8.7 V Zener diode during an overshoot for instance (absolute maximum current is 15 mA) b) to implement the fail-safe optocoupler protection (OVP) as offered by the active clamp. Please note that there cannot be bad interaction between the clamping voltage of the internal Zener and VCCON since this clamping voltage is actually built on top of VCCON with a fixed amount of offset (200 mV typical). \( R_{\text{limit}} \) should be carefully selected to avoid triggering the OVP as we discussed, but also to avoid disturbing the VCC in low/light load conditions. The following details how to evaluate the \( R_{\text{limit}} \) value.

Self-supplying controllers in extremely low standby applications often puzzles the designer. Actually, if an SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V \( (V_{\text{nom}}) \), this voltage can drop below 10 V \( (V_{\text{stdby}}) \) when entering standby. This is because the recurrence of the switching pulses expands so much, that the low frequency refueling rate of the VCC capacitor is not enough to keep a proper auxiliary voltage. Figure 35 portrays a typical scope shot of an SMPS entering deep standby (output unloaded). Thus, care must be taken when calculating \( R_{\text{limit}} \) 1) to not trigger the VCC overcurrent latch (by injecting 6.0 mA into the active clamp – always use the minimum value for worse case design) in normal operation but 2) not to drop too much voltage over \( R_{\text{limit}} \) when entering standby. Otherwise, the converter will enter burst mode as it will sense an UVLO condition. Based on these recommendations, we are able to bound \( R_{\text{limit}} \) between two equations:

\[
\frac{V_{\text{nom}} - V_{\text{clamp}}}{I_{\text{trip}}} \leq R_{\text{limit}} \leq \frac{V_{\text{stdby}} - V_{\text{CCON}}}{\text{ICC1}}
\]

(\text{eq. 3})

Where:

- \( V_{\text{nom}} \) is the auxiliary voltage at nominal load.
- \( V_{\text{stdby}} \) is the auxiliary voltage when standby is entered.
- \( I_{\text{trip}} \) is the current corresponding to the nominal operation. It thus must be selected to avoid false tripping in overshoot conditions. Always use the minimum of the specification for a robust design.
- \( \text{ICC1} \) is the controller consumption. This number slightly decreases compared to ICC1 from the spec since the part in standby does almost not switch. It is around 1.0 mA for the 65 kHz version.
- \( V_{\text{CCON}} \) is the level above which the auxiliary voltage must be maintained to keep the controller away from the UVLO trip point. It is good to obtain around 8.0 V in order to offer an adequate design margin, e.g. to not reactivate the startup source (which is not a problem in itself if low standby power does not matter).

Since \( R_{\text{limit}} \) shall not bother the controller in standby, e.g. keep Vauxiliary to around 8.0 V (as selected above), we purposely select a Vnom well above this value. As explained before, experience shows that a 40% decrease can be seen on auxiliary windings from nominal operation down to standby mode. Let’s select a nominal auxiliary winding of 20 V to offer sufficient margin regarding 8.0 V when in standby (\( R_{\text{limit}} \) also drops voltage in standby…).

---

**Figure 34. A more detailed view of the NCP1027 offers better insight on how to properly wire an auxiliary winding.**
Plugging the values in Equation 3 gives the limits within which $R_{\text{limit}}$ shall be selected:

$$\frac{20-8.7}{6 \text{ m}} \leq R_{\text{limit}} \leq \frac{12-8}{1 \text{ m}}$$

that is to say: $1.8 \text{ k\Omega} < R_{\text{limit}} < 4 \text{ k\Omega}$.

If we design a 65 kHz power supply delivering 12 V, then the ratio between auxiliary and power must be: $12/20 = 0.6$. The OVP latch will activate when the clamp current exceeds 6.0 mA. This will occur when $V_{\text{auxiliary}}$ grows up to:

1. $8.7 + 1.8 \text{ k}\Omega \times (6 \text{ m} + 1.8 \text{ m}) = 23 \text{ V}$ for the first boundary ($R_{\text{limit}} = 1.8 \text{ k}\Omega$).
2. $8.7 + 4 \text{ k}\Omega \times (6 \text{ m} + 1.8 \text{ m}) = 40 \text{ V}$ for the second boundary ($R_{\text{limit}} = 4.0 \text{ k}\Omega$).

Due to a 0.6 ratio between the auxiliary $V_{\text{CC}}$ and the power winding, the auxiliary OVP will be seen as a lower overshoot on the real output:

1. $23 \times 0.6 = 13.8 \text{ V}$
2. $40 \times 0.6 = 24 \text{ V}$

As one can see, tweaking the $R_{\text{limit}}$ value will allow the selection of a given overvoltage output level. Theoretically predicting the auxiliary drop from nominal to standby is an almost impossible exercise since many parameters are involved, including the converter time constants. Fine tuning of $R_{\text{limit}}$ thus requires a few iterations and experiments on a breadboard to check the auxiliary voltage variations but also the output voltage excursion in fault. Once properly adjusted, the fail-safe protection will preclude any lethal voltage runaways in case a problem would occur in the feedback loop.

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**Figure 35.** The burst frequency becomes so low that it is difficult to keep an adequate level on the auxiliary $V_{\text{CC}}$.

**Figure 36.** If the $V_{\text{CC}}$ current exceeds a certain threshold, an auto-recovery protection is activated and protects the design.
Improving the Precision in Auto-Recovery OVP

Given the OVP variations the internal trip current dispersion incur, it is sometimes more interesting to explore a different solution, improving the situation to the cost of a minimal amount of surrounding elements. Figure 37 shows that adding a simple Zener diode on top of the limiting resistor, offers a better precision since what matters now is the internal 8.7 V VCC breakdown, plus the Zener voltage. A resistor in series with the Zener diodes keeps the maximum current in the VCC pin below the maximum rating of 15 mA just before tripping the OVP.

![Figure 37. A simple Zener diode added in parallel with R_limit, allows for a better precision OVP.](image)

Over Power Compensation

Over Power Compensation or Protection (OPP) represents a way to limit the effects of the propagation delay when the converter is supplied from its highest input voltage. The propagation delay naturally extends the power capability of any current-limited converter. Figure 38 explains why. The main parameter is the on slope, that is to say, the pace at which the inductor current grows-up when the power switch closes. For a flyback controller, the slope is given by:

\[ S_{on} = \frac{V_{in}}{L_p} \]  

(eq. 4)

where \( L_p \) is the transformer magnetizing/primary inductance and \( V_{in} \), the input voltage.

As the internal logic takes some time to react, the switch gate shutdown does not immediately occur when the maximum power limit is detected (just before activating the overload protection circuit). Clearly speaking, it can take up to 100 ns for the NCP1027 current sense comparator to propagate through the various logical gates before reaching the power switch and finally shutting it off. This is the well-known propagation delay noted \( t_{prop} \). Unfortunately, during this time, the current keeps growing as Figure 38 depicts. The peak current will therefore be troubled by this propagation delay. The formula to obtain the final value is simply:

\[ I_{peak, final} = \frac{V_{in}}{L_p} t_{prop} + I_{peak, max} \]  

(eq. 5)

At low line, \( S_{on} \) is relatively low and does not bother the final peak value. The situation differs at high line and induces a higher peak current. Therefore, the power supply output power capability increases with the input voltage. Let us take a look at a simple example. Suppose the peak current is 700 mA:

\[ L_p = 1.0 \, \text{mH} \]
\[ V_{in, lowline} = 100 \, \text{Vdc} \]
\[ V_{in, highline} = 350 \, \text{Vdc} \]
\[ I_{peak, max} = 700 \, \text{mA} \]
\[ t_{prop} = 100 \, \text{ns} \]

\[ P_{out, lowline} = \frac{1}{2} I_{peak, final}^2 F_{SW} L_p \eta \]

(eq. 6)

Where: \( F_{SW} \) is the switching frequency and \( \eta \) the efficiency. Usually \( \eta \) is bigger in high line conditions than in low line conditions. This formula is valid for a Discontinuous Conduction Mode flyback.

From Equation 5, we can calculate the final peak current in both conditions:

\[ I_{peak, final, low} = (100/1m) \times 100n + 700m = 710 \, \text{mA at low line.} \]
\[ I_{peak, final, high} = (350/1m) \times 100n + 700m = 735 \, \text{mA at high line.} \]

From Equation 6, we can have an idea of the maximum output power capability again, in both conditions with respective low and high line efficiency numbers of 78% and 82% for instance:

\[ P_{out, lowline} = 0.5 \times 0.712^2 \times 1m \times 65k \times 0.78 = 12.8 \, \text{W} \]
\[ P_{out, highline} = 0.5 \times 0.735^2 \times 1m \times 65k \times 0.82 = 14.4 \, \text{W} \]
This difference might not be seen as a problem, but some design specifications impose stringent conditions on the maximum output current capability, regardless the line input. Hence the need for an OPP input…

Since we want to limit the power to 12.8 W at high line, let us calculate the needed peak current:

From equation 6: \( I_{\text{peak}} = \sqrt{\frac{2P_{\text{out}}}{F_{\text{SWL}}} - p} \) = 693 mA to deliver 12.8 W at high line.

Compared to our 735 mA, we need to decrease the setpoint by 6% roughly when \( V_{\text{in}} \) equals 350 Vdc.

The NCP1027 hosts a special circuitry looking at the couple voltage/current present on pin 7. Figure 39 shows how to arrange components around the controller to obtain Over Power Protection.

First, you need to know the required injected current and the voltage across pin 7 to start activating OPP. Experiments consist in wiring Figure 39 circuit and running the power supply in conditions where it must shut down (e.g. highest input voltage and maximum output current per specification). For this, \( R_{\text{OPPL}} \) can be put to 10 k\( \Omega \) and \( R_{\text{OPPU}} \) made of a series string of 4 \( \times \) 1.0 M\( \Omega \) resistors plus a 10–turn 1.0 M\( \Omega \) potentiometer set at its maximum value. An amp–meter is inserted in series with pin 7 and a volt–meter monitors its voltage with respect to ground. Once the power supply is powered, slowly rotate the potentiometer and observe both voltage and current going up at pin 7. At a certain time, as voltage and current increase, the controller will shut down the power supply. The current at this time is the one we are looking for. Suppose these experiments lead to 80 \( \mu \)A with a pin 7 activation voltage of 2.45 V. Final resistor equations are:

\[
V_{\text{bulkH}} = 375 \text{ Vdc} \quad \text{; the maximum voltage at which OPP must shut down the controller}
\]

\[
V_{\text{bulkL}} = 200 \text{ Vdc} \quad \text{; the minimum voltage below which OPP is not activated}
\]

\[
I_{\text{OPP}} = 80 \mu\text{A} \quad \text{; the current in pin 7}
\]

\[
V_f = 2.45 \text{ V} \quad \text{; the voltage of pin 7 at the above condition}
\]

\[
R_{\text{OPPL}} = \frac{V_{\text{bulkH}} - V_{\text{bulkL}}}{I_{\text{OPP}}(V_{\text{bulkL}} - V_f)} \quad V_f = 27 \text{ k}\Omega \quad \text{(eq. 7)}
\]

\[
R_{\text{OPPL}_H} = \frac{R_{\text{OPPL}}}{V_{\text{bulkL}} - V_f} \quad V_f = 2.2 \text{ M}\Omega \quad \text{(eq. 8)}
\]

If the OPP feature is not needed for some designs, it is possible to ground it via a copper wire to the adjacent ground pin. This can help to develop a larger copper area in an application where the thermal resistance is an important parameter.

**Ramp Compensation**

When operating in Continuous Conduction Mode (CCM), current–mode power supplies can exhibit so–called sub–harmonic oscillations. To cure this problem, the designer must inject ramp compensation. The ramp can either be added to the current sense information or directly subtracted from the feedback signal. Figure 40 details the internal arrangement of the ramp compensation circuitry.

**Figure 39. A resistive network reduces the power capability in high–line conditions.**

**Figure 40. The Internal Feedback Chain and the Ramp Compensation Network**
The principle consists in selecting the RR resistor, connected from pin 2 to ground, to impose a current \( I_{RR} \) in the transistor collector.

The equation to get the right compensation level is the following:

\[
RR = \frac{V_p}{S_a \times TSW} \tag{9}
\]

where \( V_p \), the total voltage swing, equals 2.75 V.

**Application example:**

Suppose we have the following flyback specifications:

- \( V_{out} = 5.0 \text{ V} \) output voltage
- \( V_f = 1.0 \text{ V} \) secondary diode forward drop @ \( I_{out} \) nominal

We can calculate the \( S_a \), by reflecting the output voltage over the primary inductance. The slope is projected over a complete switching period. Here, we use a 65 kHz part.

\[
S_{off} = \frac{V_{out} + V_f}{N_{Lp}} \times TSW = \frac{6 \times 15 \mu A}{0.052 \times 3.8 \text{mH}} = 455 \text{mA/15 \mu s} \quad (eq. 10)
\]

Due to the internal sense arrangement, this current slope will become a voltage slope having a value of:

\[
S'_{off} = 455 \text{mA} \times 0.375 = 170 \text{mV/15 \mu s} \quad (eq. 11)
\]

If we chose 50% of this downslope, then the final compensation ramp will present a slope of:

\[
S_a = \frac{170 \text{mV}}{2} = 85 \text{mV/15 \mu s} \quad (eq. 12)
\]

We then have:

\[
RR = \frac{V_p}{S_a \times TSW} = \frac{2.75 \text{V}}{2.75 \times 2.75 \text{k} \Omega} = 89 \text{k}\Omega \quad (eq. 13)
\]

In the above calculations, the internal ESD resistor has purposely been omitted to avoid bringing in another variable. In case no ramp compensation is required, pin 2 must be tied to \( V_{CC} \), the adjacent pin.

**Soft−Start**

The NCP1027 features a 1.0 ms soft−start, which reduces the power−on stress, but also contributes to lower the output overshoot. Figure 42 shows a typical operating waveform. The NCP1027 features a novel patented structure which offers a better soft−start ramp, almost ignoring the startup pedestal inherent to traditional current−mode supplies.
**Jittering**

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP1027 offers a ±6% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 43 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

![Figure 43. Modulation Effects on the Clock Signal by the Jittering Sawtooth](image)

**Skip–Cycle**

Skip cycle offers an efficient way to reduce the standby power by skipping unwanted cycles at light loads. However, the recurrent frequency in skip often enters the audible range and a high peak current obviously generates acoustic noise in the transformer. The noise takes its origins in the resonance of the transformer mechanical structure which is excited by the skipping pulses. A possible solution, successfully implemented in the NCP1200 series, also authorizes skip cycle but only when the power demand as dropped below a given level. This is what Figure 44 shows, as implemented on the NCP1027.

![Figure 44. Low Peak Current Skip Cycle Guarantees Noise–Free Operation](image)
5.0 V/3.0 A Universal Mains Power Supply

Due to its low $R_{\text{DS(on)}}$, the NCP1027 can be used in universal mains SMPS up to 15 W of continuous power, provided that the chip power dissipation is well under control. That is to say that average power calculations and measurements have been carried and correlated. The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

1. The lateral MOSFET body−diode shall never be forward biased, either during startup (because of a large leakage inductance) or in normal operation as shown by Figure 45. This condition sets the maximum voltage that can be reflected during $t_{\text{off}}$.

$$V_{\text{in}} \text{min} = 120 \text{ Vdc}$$
$$V_{\text{in}} \text{max} = 375 \text{ Vdc}$$
$$V_{\text{out}} = 5.0 \text{ V}$$
$$V_{\text{out}} = 15 \text{ W}$$
Operating mode is CCM

2. Lateral MOSFETs have a poorly doped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since $V_{\text{drain max}} = V_{\text{in}} + N (V_{\text{out}} + V_f)$

$$d_{\text{max}} = \frac{NV_{\text{out}}}{V_{\text{in}} + V_{\text{out}, \text{min}}} = \frac{1}{1 + \frac{V_{\text{in,min}}}{V_{\text{out}}}} = 0.49 \quad (\text{eq. 16})$$

3. To obtain the primary inductance, we have the choice between two equations:

$$L = \frac{(V_{\text{in}}d)^2}{I_{\text{SW/KP}}p_{\text{in}}} \quad (\text{eq. 17}), \text{ where } K = \frac{\Delta L}{I_1}$$

- Small $K$: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
• **Large K**: approaching BCM where the rms losses are the worse, but smaller inductance, leading to a better leakage inductance.

From Equation 16, a $K$ factor of 0.8 (40% ripple), gives an inductance of:

$$L = \frac{(120 \times 0.49)^2}{60k \times 0.8 \times 18.75} = 3.8 \text{ mH}$$

$$\Delta L = \frac{V_{ind}}{L_{FSW}} = \frac{120 \times 0.49}{3.8m \times 60k} = 258 \text{ mA peak}$$

The peak current can be evaluated to be:

$$I_{peak} = I_{avg} + \frac{\Delta L}{2} = I_{peak} = \frac{156m}{0.49} + \frac{\Delta L}{2} = 447 \text{ mA}$$

In Figure 46, $I_1$ can also be calculated:

$$I_1 = I_{peak} - \frac{\Delta L}{2} = 0.447 - 0.129 = 318 \text{ mA}$$

5. Based on the above numbers, we can now evaluate the conduction losses:

$$I_{d, \text{rms}} = I_1 \sqrt{1 + \frac{1}{3} \left( \frac{0.258}{2 \times 0.318} \right)^2} = 228 \text{ mA rms}$$

If we take the maximum $R_{DS(on)}$ for a 120°C junction temperature, i.e. 11 Ω then conduction losses worse case are:

$$P_{\text{cond}} = I_{d, \text{rms}}^2 R_{DS(on)} = 571 \text{ mW}$$

6. Off–time and on–time switching losses can be estimated based on the following calculations:

$$P_{\text{off}} = \frac{I_{peak} V_{\text{ds}}}{6T_{SW}} = \frac{0.447 \times 650 \times 40n}{6 \times 15u} = 130 \text{ mW} \quad \text{(eq. 18)}$$

$$P_{\text{on}} = \frac{I_{peak} (V_{out} + V_f)_{\text{on}}}{6T_{SW}} = \frac{0.447 \times 114 \times 40n}{6 \times 15u} = 22 \text{ mW} \quad \text{(eq. 19)}$$

The theoretical total power is then 0.571 + 0.13 + 0.022 = 723 mW.

7. The ramp compensation will be calculated as suggested by Equation 13 giving a resistor of 78 kΩ or 82 kΩ for the normalized value.

### Power Switch Circuit Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the power switch circuit $BV_{dss}$ which is 700 V. Figures 47a, b, c present possible implementations:

**Figure 47a:** The simple capacitor limits the voltage according to Equation 14. This option is only valid for low power applications, e.g. below 5.0 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute $C$ with Equation 15. Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses...

**Figure 47b:** The most standard circuitry called the RCD network. You calculate $R_{\text{clamp}}$ and $C_{\text{clamp}}$ using the following formulae:

$$R_{\text{clamp}} = \frac{2V_{\text{clamp}} (V_{\text{clamp}} - (V_{out} + V_f)) N}{I_{\text{peak}}^2 F_{\text{SW}}} \quad \text{(eq. 20)}$$

$$C_{\text{clamp}} = \frac{V_{\text{clamp}}}{V_{\text{ripple}} F_{\text{SW}} N_{\text{clamp}}} \quad \text{(eq. 21)}$$
clamp is usually selected 50−80 V above the reflected value \( N \times (V_{out} + V_f) \). The diode needs to be a fast one and an MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when \( I_{peak} \) and \( V_{in} \) are maximum and \( V_{out} \) is close to reach the steady−state value.

Figure 47c: This option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a Zener diode or a TVS. There are little technology differences behind a standard Zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of Zener. A 5.0 W Zener diode, like the 1N5388B, will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal Zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5.0 W of continuous power, but is able to accept surges up to 600 W @ 1.0 ms. Select the Zener or TVS clamping level between 40 to 80 V above the reflected output voltage when the supply is heavily loaded.

Power Dissipation and Heatsinking

The NCP1027 hosting a power switch circuit and a controller, it is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the PDI7 package. When surrounded by a surface greater than 1.0 cm² of 35 μm copper, it becomes possible to drop the thermal resistance junction−to−ambient, \( R_{JA} \) down to 75°C/W and thus dissipate more power. The maximum power the device can thus evacuate is: \( P_{max} = \frac{T_{j\max} - T_{amb\max}}{R_{JA}} \) (eq. 22) which gives around 930 mW for an ambient of 50°C and a maximum junction of 120°C. The losses inherent to the switch circuit \( R_{DS(on)} \) can be theoretically evaluated, but the final prototype evaluation must include board measurements to confirm that the junction temperature stays within safe limits. Figure 48 gives a possible layout to help dropping the thermal resistance. When measured on a 70 μm (2 oz.) copper thickness PCB, we obtained a thermal resistance of 75°C/W.

When routing the printed circuit, it is important to keep high impedance line very short, like the brown−out signal and the OPP input if used.

Application Diagram

Figure 49 displays the final application schematic. The output uses a TLV431 whose low bias current represents an advantage for low standby power switch mode supplies. The secondary side features an additional LC filter needed to remove unwanted spikes, although less problematic than in DCM operation. On the primary side, a resistive network senses the input bulk voltage and prevents the controller from turning on for input voltages below 100 Vdc. The auxiliary winding delivers 20 V nominal and thus offers comfortable margin when the converter enters standby. As we do not use any OPP, pin 7 goes to ground and offers extended possibility to layout more copper area.
Figure 49. 5.0 V−3.0 A Universal Mains Power Supply
Transformer Specifications:

Vout = 5.0 V/3.0 A
Vaux = 20 V/10 mA
Lp = 3.8 mH
Ip, rms = 280 mA
Ip, max = 800 mA
Isec, rms = 5.0 A
Fsw = 65 kHz
Np:Nsec = 1 : 0.052
Np:Naux = 1 : 0.208
PACKAGE DIMENSIONS

PDIP−7 (PDIP−8 LESS PIN 6)

CASE 626A

ISSUE B

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
   AGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
   OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT
   TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
   PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
   TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE
   LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
   LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
   CORNERS).

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INCHES

MILLIMETERS

NOTE 5

END VIEW

WITH LEADS CONSTRAINED

NOTE 6

SEATING PLANE

NOTE 3

SIDE VIEW

NOTE 8

TOP VIEW

END VIEW

WITH LEADS CONSTRAINED

NOTE 2

A

B

C

D

E

H

L

M

a

b

b2

A

A1

D1

A2

eB

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