

# NBA3N5573

## PCIe Clock Generator, Automotive Grade, Dual Output, 3.3 V



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### Description

The NBA3N5573 is an automotive grade precision, low phase noise clock generator that supports PCI Express and Ethernet requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal and generates a differential HCSL output at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies. Outputs can interface with LVDS with proper termination (See Figure 4).

This device is housed in 3 mm x 3 mm, 0.5 p QFN16 package with wettable flanks to accommodate visual inspection.

### Features

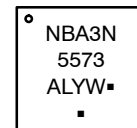
- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- AEC-Q100 Qualified and PPAP Capable
- No External Loop Filter Required
- HCSL Differential Output or LVDS with Proper Termination
- Four Selectable Multipliers of the Input Frequency
- Output Enable with Tri-State Outputs
- PCIe Gen1, Gen2, Gen3, Gen4, QPI, UPI Jitter Compliant
- Phase Noise: @ 100 MHz
 

Offset	Noise Power
100 Hz	-113 dBc
1 kHz	-127 dBc
10 kHz	-135 dBc
100 kHz	-138 dBc
1 MHz	-139 dBc
10 MHz	-160 dBc
20 MHz	-162 dBc
- Typical Period Jitter RMS of 1.5 ps
- Operating Supply Voltage Range 3.3 V ±10%
- Operating Temperature Range -40°C to +105°C
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



1  
QFNW16  
MN SUFFIX  
CASE 484AN

### MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

### Applications

- Automotive
- Networking
- Industrial Equipment
- PCIe Clock Generation Gen 1, Gen 2, Gen 3 and Gen 4
- Gigabit Ethernet
- FB DIMM

### End Products

- Infotainment and In-Cabin Electronics
- Autonomous Vehicles
- Switch and Router
- Set Top Box
- Servers, Desktop Computers
- Automated Test Equipment

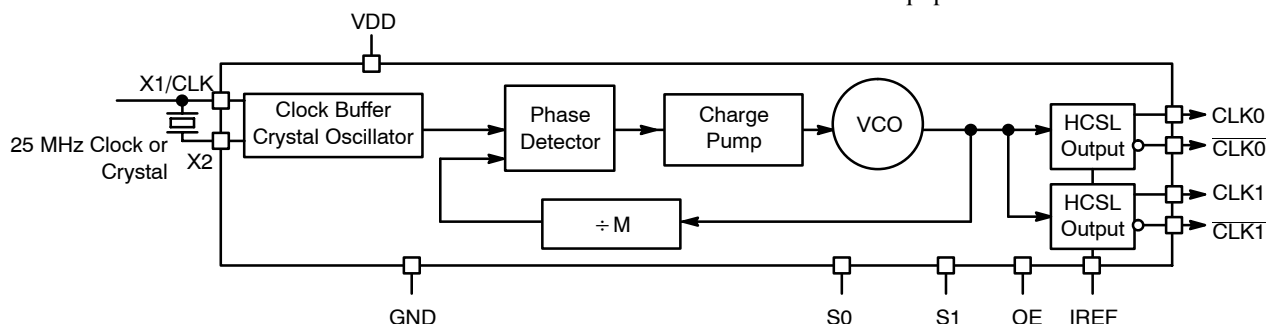


Figure 1. NBA3N5573 Simplified Logic Diagram

# NBA3N5573

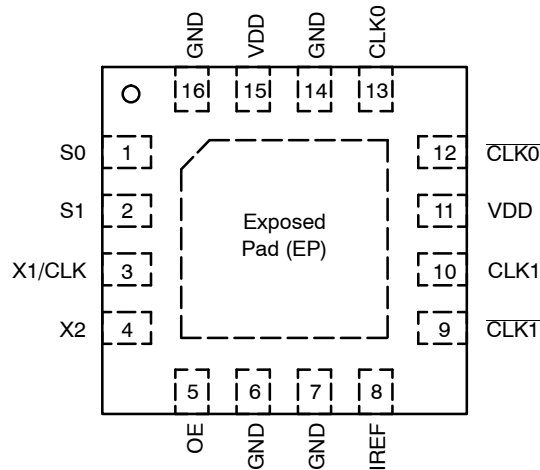


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	S0	Input	LVTTTL/LVCMOS frequency select input 0. Internal pullup resistor to $V_{DD}$ . See output select Table 2 for details.
2	S1	Input	LVTTTL/LVCMOS frequency select input 1. Internal pullup resistor to $V_{DD}$ . See output select Table 2 for details.
11, 15	$V_{DD}$	Power Supply	Positive supply voltage pins are connected to +3.3 V supply voltage.
3	X1/CLK	Input	Crystal or Clock input. Connect to 25 MHz crystal source or single-ended clock.
4	X2	Input	Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input.
5	OE	Input	Output enable tri-states output when connected to GND. Internal pullup resistor to $V_{DD}$ .
6, 7, 14, 16	GND	Power Supply	Ground 0 V. These pins provide GND return path for the devices.
8	$I_{REF}$	Output	Output current reference pin. Precision resistor (typ. 475 $\Omega$ ) is connected to set the output current.
10	CLK1	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 4)
9	$\overline{CLK1}$	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 4)
13	CLK0	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 4)
12	$\overline{CLK0}$	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 4)
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of the package. The Exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be connected to the device GND

Table 2. OUTPUT FREQUENCY SELECT TABLE WITH 25 MHz CRYSTAL

S1*	S0*	CLK Multiplier	$f_{CLKout}$ (MHz)
L	L	1x	25
L	H	4x	100
H	L	5x	125
H	H	8x	200

\*Pins S1 and S0 default high when left open.

## Recommended Crystal Parameters

Crystal	Fundamental AT-Cut
Frequency	25 MHz
Load Capacitance	16–20 pF
Shunt Capacitance, $C_0$	7 pF Max
Equivalent Series Resistance	50 $\Omega$ Max
Initial Accuracy at 25 °C	$\pm 20$ ppm
Temperature Stability	$\pm 30$ ppm
Aging	$\pm 20$ ppm
Drive Level	100 $\mu$ W Max

**Table 3. ATTRIBUTES**

Characteristic	Value
ESD Protection Human Body Model	> 2 kV
RPU – OE, S0 and S1 Pull-up Resistor	100 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	7623
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS** (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>DD</sub>	Positive Power Supply	GND = 0 V		4.6	V
V <sub>I</sub>	Input Voltage (V <sub>IN</sub> )	GND = 0 V	GND ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	-0.5 V to V <sub>DD</sub> +0.5 V	V
T <sub>A</sub>	Operating Temperature Range			-40 to +105	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
T <sub>J(max)</sub>	Maximum Junction Temperature			+125	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-16 QFN-16	42 35	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 3)	QFN-16	4	°C/W
T <sub>sol</sub>	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
- JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

**Table 5. DC CHARACTERISTICS** (V<sub>DD</sub> = 3.3 V ±10%, GND = 0 V, T<sub>A</sub> = -40°C to +105°C, Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	2.97	3.3	3.63	V
I <sub>DD</sub>	Power Supply Current		120	135	mA
I <sub>DDOE</sub>	Power Supply Current when OE is Set Low			65	mA
V <sub>IH</sub>	Input HIGH Voltage (X/CLK, S0, S1, and OE)	2000		V <sub>DD</sub> + 300	mV
V <sub>IL</sub>	Input LOW Voltage (X/CLK, S0, S1, and OE)	GND – 300		800	mV
V <sub>OH</sub>	Output HIGH Voltage for HCSL Output (See Figure 5)	660	700	850	mV
V <sub>OL</sub>	Output LOW Voltage for HCSL Output (See Figure 5)	-150	0	150	mV
V <sub>cross</sub>	Crossing Voltage Magnitude (Absolute) for HCSL Output	250		550	mV
ΔV <sub>cross</sub>	Change in Magnitude of V <sub>cross</sub> for HCSL Output			150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- Measurement taken with outputs terminated with R<sub>S</sub> = 33.2 Ω, R<sub>L</sub> = 49.9 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 3.

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**Table 6. AC CHARACTERISTICS** ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ; Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
$f_{CLKIN}$	Clock/Crystal Input Frequency		25		MHz
$f_{CLKOUT}$	Output Clock Frequency	25		200	MHz
$\theta_{NOISE}$	Phase-Noise Performance $f_{CLKx} = 200\text{ MHz}/100\text{ MHz}$				dBc/Hz
	@ 100 Hz offset from carrier		-106/-113		
	@ 1 kHz offset from carrier		-121/-127		
	@ 10 kHz offset from carrier		-129/-135		
	@ 100 kHz offset from carrier		-131/-138		
	@ 1 MHz offset from carrier		-133/-139		
	@ 10 MHz offset from carrier		-157/-160		
$t_{JITTER}$	Period Jitter Peak-to-Peak (Note 6) $f_{CLKx} = 200\text{ MHz}$		10	20	ps
	Period Jitter RMS (Note 6) $f_{CLKx} = 200\text{ MHz}$		1.5	3	
	Cycle-Cycle RMS Jitter (Note 7) $f_{CLKx} = 200\text{ MHz}$		2	5	
	Cycle-to-Cycle Peak to Peak Jitter (Note 7) $f_{CLKx} = 200\text{ MHz}$		20	35	ps
$t_{JIT(\Phi)}$	Additive Phase RMS Jitter, Integration Range 12 kHz to 20 MHz		0.4		ps
OE	Output Enable/Disable Time		10		$\mu\text{s}$
$t_{DUTY\_CYCLE}$	Output Clock Duty Cycle (Measured at cross point)	45	50	55	%
$t_R$	Output Risetime (Measured from 175 mV to 525 mV, Figure 5)	175	340	700	ps
$t_F$	Output Falltime (Measured from 525 mV to 175 mV, Figure 5)	175	340	700	ps
$\Delta t_R$	Output Risetime Variation (Single-Ended)			125	ps
$\Delta t_F$	Output Falltime Variation (Single-Ended)			125	ps
Stabilization Time	Stabilization Time From Powerup $V_{DD} = 3.3\text{ V}$		3.0		ms
$t_{SKEW}$	Within Device Output to Output Skew			40	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

5. Measurement taken from differential output on single-ended channel terminated with  $R_S = 33.2\ \Omega$ ,  $R_L = 49.9\ \Omega$ , with test load capacitance of 2 pF and current biasing resistor set at 475  $\Omega$ . See Figure 3.
6. Sampled with 10000 cycles.
7. Sampled with 1000 cycles.

Table 7. ELECTRICAL CHARACTERISTICS – PHASE JITTER PARAMETERS

Symbol	Parameter	Conditions (Notes 8 and 9)	Min	Typ	Max	Industry Limit	Unit
$t_{jphPCleG1}$	RMS Phase Jitter	PCle Gen 1 (Notes 10 and 11)		10	16	86	ps (p-p)
$t_{jphPCleG2}$		PCle Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 10)		0.2	0.25	3	ps (rms)
		PCle Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 10)		0.9	1.2	3.1	ps (rms)
$t_{jphPCleG3}$		PCle Gen 3 (PLL BW of 2–4 MHz, CDR = 10 MHz) (Note 10)		0.2	0.3	1	ps (rms)
$t_{jphPCleG4}$		PCle Gen 4 (PLL BW of 2–4 MHz, CDR = 10 MHz) (Note 10)		0.21	0.3	0.5	ps (rms)
$t_{jphUPI}$		UPI (9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI)		0.62	0.8	1.0	ps (rms)
$t_{jphQPI\_SMI}$		QPI & SMI (100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Note 12)		0.1	0.3	0.5	ps (rms)
		QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Note 12)		0.1	0.15	0.3	ps (rms)
		QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Note 12)		0.07	0.1	0.2	ps (rms)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Applies to all outputs.

9. Guaranteed by design and characterization, not tested in production

10. See <http://www.pcisig.com> for complete specs

11. Sample size of at least 100K cycles. This figures extrapolates to 108 ps pk-pk @ 1M cycles for a BER of 1-12.

12. Calculated from Intel-supplied Clock Jitter Tool v 1.6.3.

HCSL INTERFACE

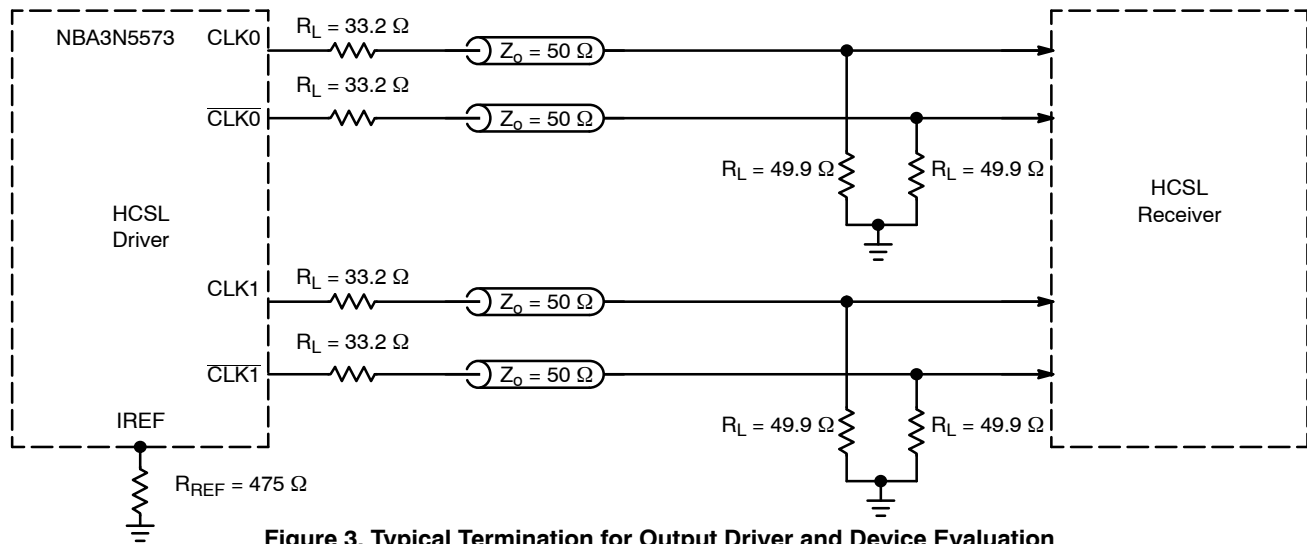
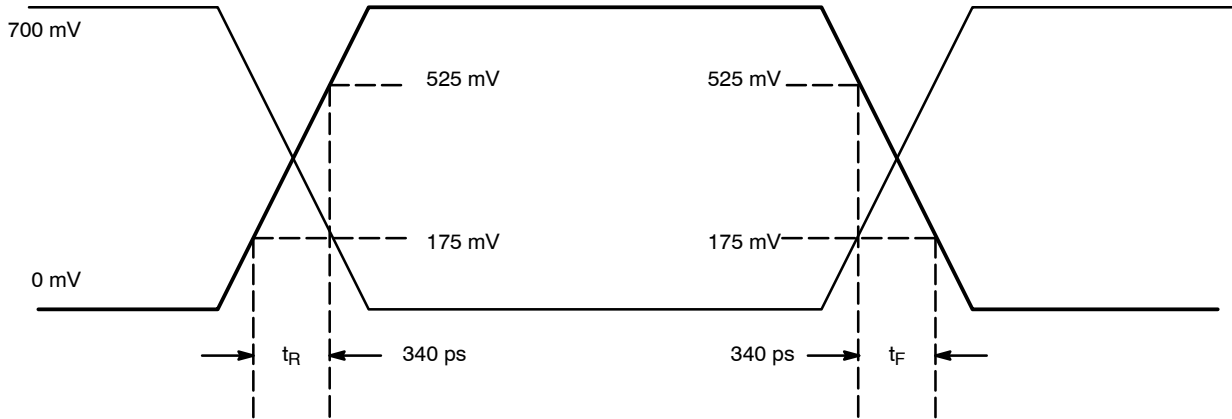
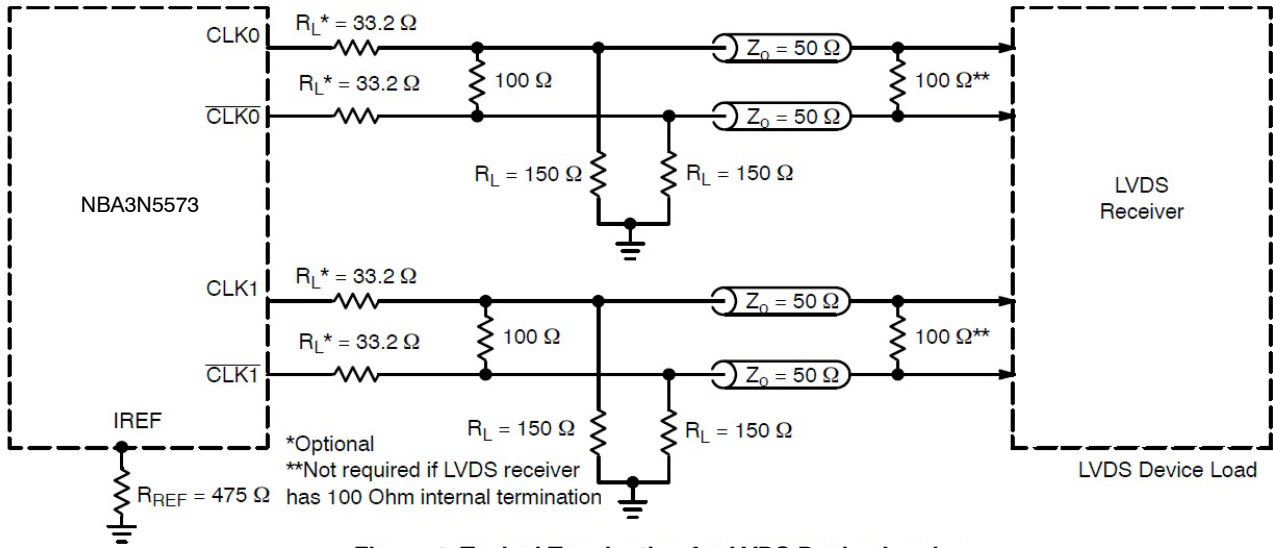


Figure 3. Typical Termination for Output Driver and Device Evaluation

LVDS COMPATIBLE INTERFACE



ORDERING INFORMATION

Device	Package	Shipping†
NBA3N5573MNTXG	QFN-16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

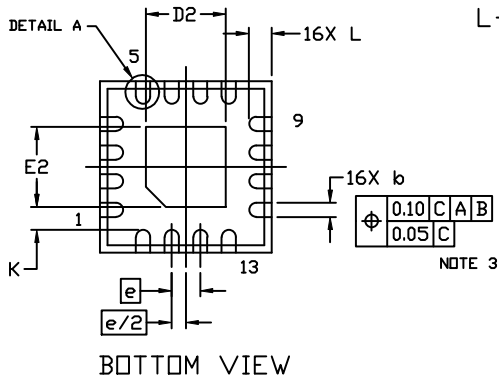
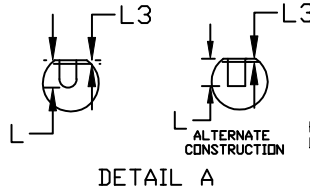
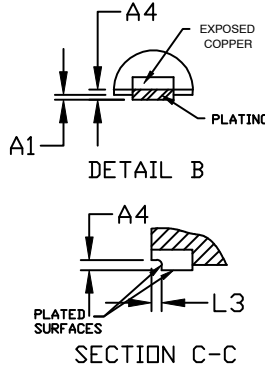
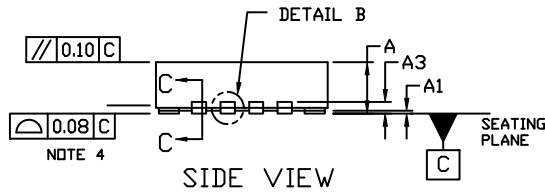
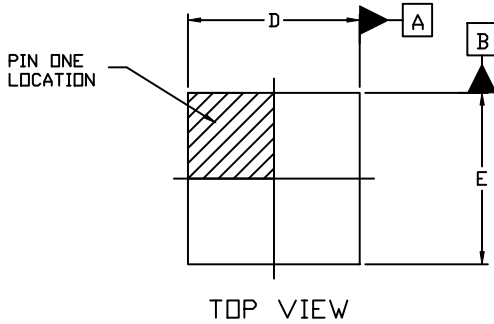
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## PACKAGE DIMENSIONS

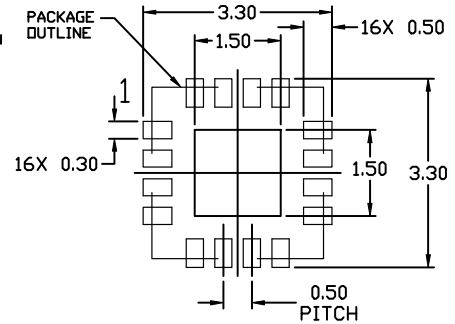
**QFNW16 3x3, 0.5P**  
**CASE 484AN**  
**ISSUE O**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
A4	0.13 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.30	1.40	1.50
e	0.50 BSC		
K	0.40 REF		
L	0.30	0.40	0.50
L3	0.05 REF		



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