

# NB7V72M

## 1.8V / 2.5V Differential 2 x 2 Crosspoint Switch with CML Outputs Clock/Data Buffer/Translator

### Multi-Level Inputs w/ Internal Termination

#### Description

The NB7V72M is a high bandwidth, low voltage, fully differential 2 x 2 crosspoint switch with CML outputs. The NB7V72M design is optimized for low skew and minimal jitter as it produces two identical copies of Clock or Data operating up to 5 GHz or 6.5 Gb/s, respectively. As such, the NB7V72M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications. The differential  $\overline{IN}/\overline{IN}$  inputs incorporate internal 50  $\Omega$  termination resistors and will accept LVPECL, CML, or LVDS logic levels (see Figure 10). The 16 mA differential CML outputs provide matching internal 50  $\Omega$  terminations and produce 400 mV output swings when externally terminated with a 50  $\Omega$  resistor to  $V_{CC}$  (see Figure 11). The NB7V72M is the 1.8 V/2.5 V CML version of the NB7L72M and is offered in a low profile 3x3 mm 16-pin QFN package. Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

The NB7V72M is a member of the GigaComm™ family of high performance clock products.

#### Features

- Maximum Input Data Rate > 6.5 Gb/s
- Data Dependent Jitter < 15 ps pk-pk
- Maximum Input Clock Frequency > 5 GHz
- Random Clock Jitter < 0.8 ps RMS, Max
- 150 ps Typical Propagation Delay
- 30ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV peak-to-peak, typical
- Operating Range:  $V_{CC} = 1.71$  V to 2.625 V with  $GND = 0$  V
- Internal 50  $\Omega$  Input Termination Resistors
- QFN-16 Package, 3mm x 3mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



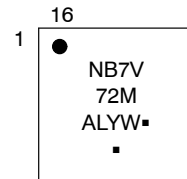
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<http://onsemi.com>

#### MARKING DIAGRAM\*



1  
QFN-16  
MN SUFFIX  
CASE 485G



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

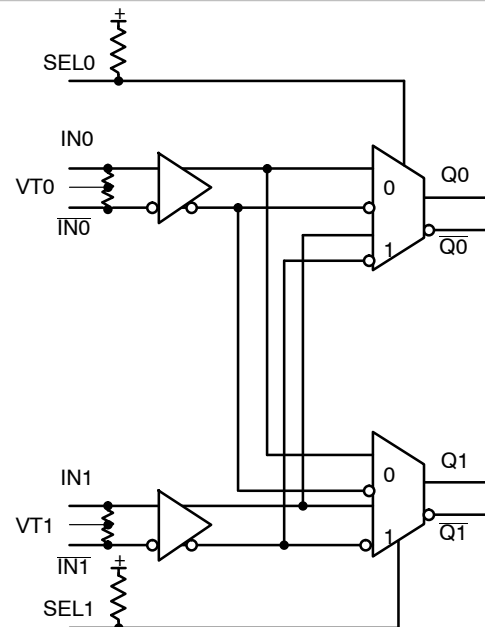


Figure 1. Logic Diagram

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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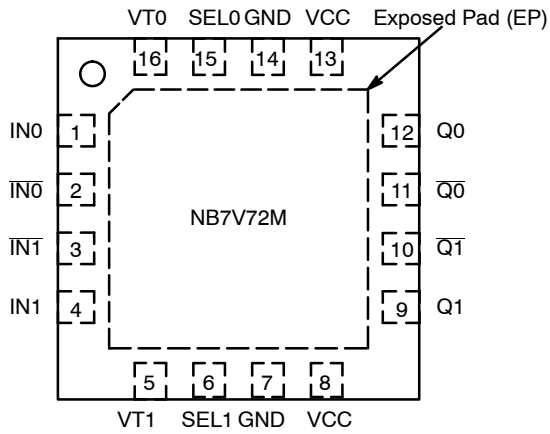


Figure 2. Pin Configuration (Top View)

Table 1. INPUT/OUTPUT SELECT TRUTH TABLE

SEL0*	SEL1*	Q0	Q1
L	L	IN0	IN0
L	H	IN0	IN1
H	L	IN1	IN0
H	H	IN1	IN1

\*Defaults HIGH when left open

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	IN0	LVPECL, CML, LVDS Input	Noninverted Differential Input. (Note 1)
2	IN0-bar	LVPECL, CML, LVDS Input	Inverted Differential Input. (Note 1)
3	IN1-bar	LVPECL, CML, LVDS Input	Inverted Differential Input. (Note 1)
4	IN1	LVPECL, CML, LVDS Input	Noninverted Differential Input. (Note 1)
5	VT1	-	Internal 50 $\Omega$ Termination Pin for IN1 and IN1-bar
6	SEL1	LVC MOS Input	Input Select logic pin for IN0 or IN1 Inputs to Q1 output. See Table 1, Input/Output Select Truth Table; pin defaults HIGH when left open.
7	GND	-	Negative Supply Voltage
8	VCC	-	Positive Supply Voltage
9	Q1	CML Output	Noninverted Differential Output. (Note 1)
10	Q1-bar	CML Output	Inverted Differential Output. (Note 1)
11	Q0-bar	CML Output	Inverted Differential Output. (Note 1)
12	Q0	CML Output	Noninverted Differential Output. (Note 1)
13	VCC	-	Positive Supply Voltage
14	GND	-	Negative Supply Voltage
15	SEL0	LVC MOS Input	Input Select logic pin for IN0 or IN1 Inputs to Q0 output. See Table 1, Input/Output Select Truth Table; pin defaults HIGH when left open.
16	VT0	-	Internal 50 $\Omega$ Termination Pin for IN0 and IN0-bar
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and is recommended to be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on INx/INx-bar input, then the device will be susceptible to self-oscillation.
2. All VCC and GND pins must be externally connected to a power supply for proper operation.

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**Table 3. ATTRIBUTES**

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 4 kV > 200 V
R <sub>PU</sub> – Input Pullup Resistor		75kΩ
Moisture Sensitivity	16-QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		210
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		3.0	V
V <sub>IN</sub>	Positive Input Voltage	GND = 0 V		-0.5 to V <sub>CC</sub> +0.5	V
V <sub>INPP</sub>	Differential Input Voltage  I <sub>N</sub> - I <sub>N</sub>			1.89	V
I <sub>IN</sub>	Input Current Through R <sub>T</sub> (50 Ω Resistor)			± 40	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfp 500 lfp	QFN-16 QFN-16	42 35	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case) (Note 3)		QFN-16	4	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 5. DC CHARACTERISTICS, Multi-Level Inputs**  $V_{CC} = 1.71\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  (Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
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## POWER SUPPLY CURRENT

$I_{CC}$	Power Supply Current (Inputs and Outputs Open)	$V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$	120 80	145 110	170 140	mA
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## CML OUTPUTS

$V_{OH}$	Output HIGH Voltage (Note 5)	$V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$	$V_{CC} - 40$ 2460 1760	$V_{CC} - 20$ 2480 1780	$V_{CC}$ 2500 1800	mV
$V_{OL}$	Output LOW Voltage (Note 5)	$V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$	$V_{CC} - 650$ 1850 1150	$V_{CC} - 400$ 2100 1400	$V_{CC} - 300$ 2200 1500	mV

## DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Note 6) (Figures 5 and 7)

$V_{th}$	Input Threshold Reference Voltage Range (Note 7)	1050		$V_{CC} - 100$	mV
$V_{IH}$	Single-Ended Input HIGH Voltage	$V_{th} + 100$		$V_{CC}$	mV
$V_{IL}$	Single-Ended Input LOW Voltage	GND		$V_{th} - 100$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	200		$V_{CC} - GND$	mV

## DIFFERENTIAL DATA/CLOCK INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8) (Note 8)

$V_{IHD}$	Differential Input HIGH Voltage ( $IN_n, \overline{IN}_n$ )	1100		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage ( $IN_n, \overline{IN}_n$ )	GND		$V_{CC} - 100$	mV
$V_{ID}$	Differential Input Voltage ( $IN_n, \overline{IN}_n$ ) ( $V_{IHD} - V_{ILD}$ )	100		1200	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration, Note 9) (Figure 9)	1050		$V_{CC} - 50$	mV
$I_{IH}$	Input HIGH Current $IN_n, \overline{IN}_n$ ( $V_{TIN}/V_{TIN}$ Open)	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $IN_n, \overline{IN}_n$ ( $V_{TIN}/V_{TIN}$ Open)	-150		150	$\mu\text{A}$

## CONTROL INPUTS (SEL0, SEL1)

$V_{IH}$	Input HIGH Voltage for Control Pins	$V_{CC} \times 0.65$		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage for Control Pins	GND		$V_{CC} \times 0.35$	mV
$I_{IH}$	Input HIGH Current	-150	20	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150	5	150	$\mu\text{A}$

## TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor	40	50	60	$\Omega$
$R_{TOUT}$	Internal Output Termination Resistor	40	50	60	$\Omega$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .
- CML outputs loaded with  $50\ \Omega$  to  $V_{CC}$  for proper operation.
- $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.
- $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.
- $V_{CMR}$  min varies 1:1 with GND,  $V_{CMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal.

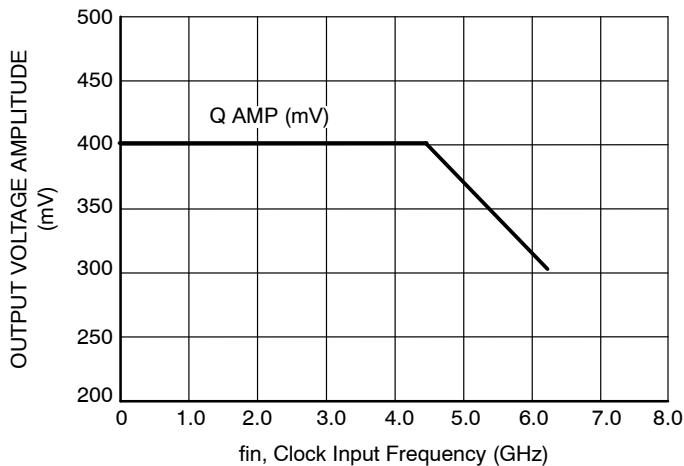
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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 1.71\text{ V to }2.625\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (Note 10)

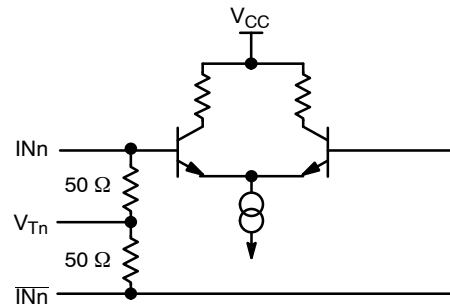
Symbol	Characteristic	Min	Typ	Max	Unit	
$f_{MAX}$	Maximum Input Clock Frequency $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$	5 4.5			GHz	
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)	6.5			Gbps	
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) $f_{in} \leq 5\text{ GHz}$ (See Figures 3 and 10, Note 11)	200	400		mV	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Differential Outputs, @ 1GHz, Measured at Differential Cross-point	$I_{Nn}/I_{\overline{Nn}}$ to $Q_n/\overline{Q_n}$	110	150	200	ps
$t_{PLH\ TC}$	Propagation Delay Temperature Coefficient		50		$\Delta\text{fs}/^\circ\text{C}$	
$t_{SKEW}$	Output-to-Output Skew (within device) (Note 12) Device-to-Device Skew ( $t_{pdmax} - t_{pdmin}$ )			30 50	ps	
$t_{DC}$	Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} \leq 5\text{GHz}$	45	50	55	%	
$t_{jitter}$	RJ – Output Random Jitter (Note 13) $f_{in} \leq 5\text{ GHz}$ DJ – Deterministic Jitter (Note 14) $\leq 9\text{ Gbps}$		0.5	0.8 10	ps RMS ps pk-pk	
$V_{INPP}$	Input Voltage Swing (Differential Configuration) (Note 15)	100		1200	mV	
$t_r, t_f$	Output Rise/Fall Times @ 1 GHz (20% – 80%), $Q_n, \overline{Q_n}$	20	30	50	ps	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured using a 400 mV source, 50% duty cycle clock source. All output loading with external  $50\ \Omega$  to  $V_{CC}$ . Input edge rates  $\geq 40\text{ ps}$  (20% – 80%).
11. Output voltage swing is a single-ended measurement operating in differential mode.
12. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the cross-point of the outputs.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
15. Input voltage swing is a single-ended measurement operating in differential mode.



**Figure 3. CLOCK Output Voltage Amplitude ( $V_{OUTPP}$ ) vs. Input Frequency ( $f_{in}$ ) at Ambient Temperature (Typ)**



**Figure 4. Input Structure**

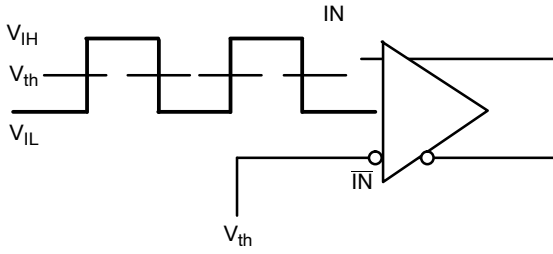


Figure 5. Differential Input Driven Single-Ended

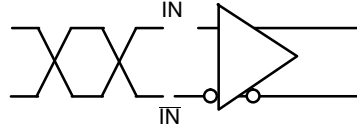


Figure 6. Differential Inputs Driven Differentially

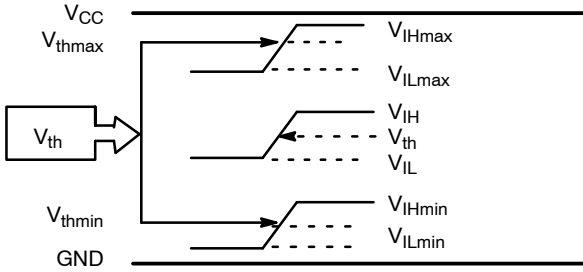


Figure 7.  $V_{th}$  Diagram

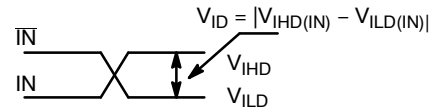


Figure 8. Differential Inputs Driven Differentially

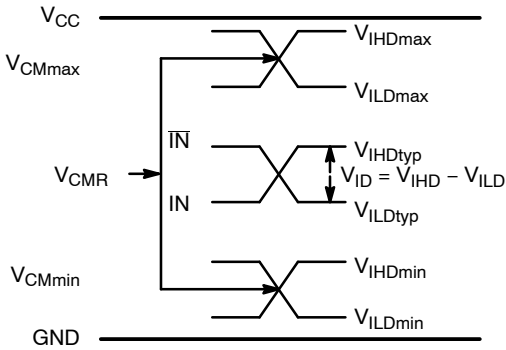


Figure 9.  $V_{CMR}$  Diagram

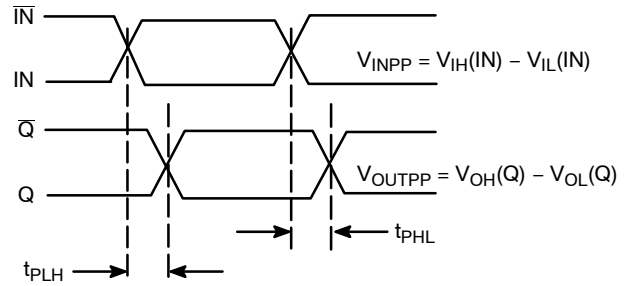


Figure 10. AC Reference Measurement

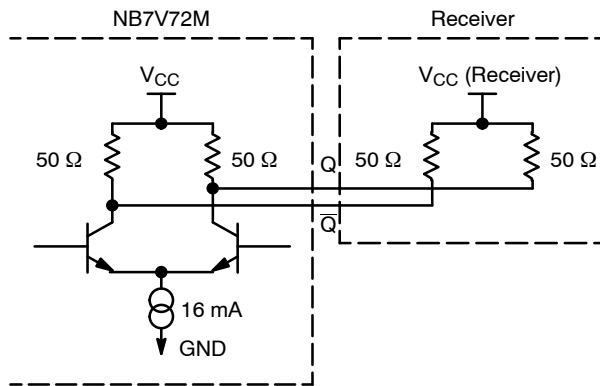


Figure 11. Typical CML Output Structure and Termination

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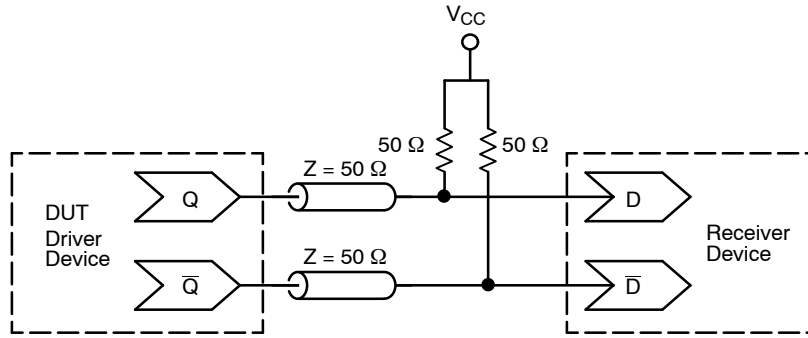


Figure 12. Typical Termination for CML Output Driver and Device Evaluation

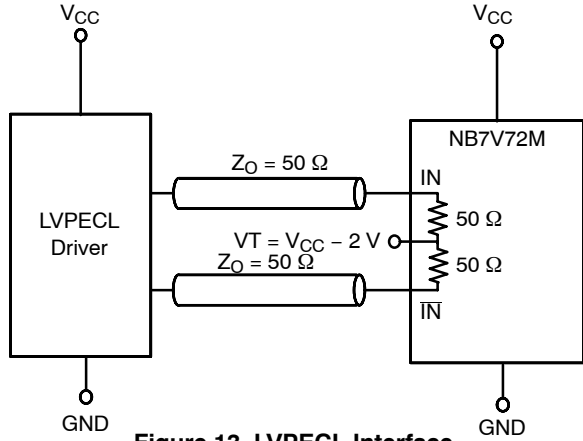


Figure 13. LVPECL Interface

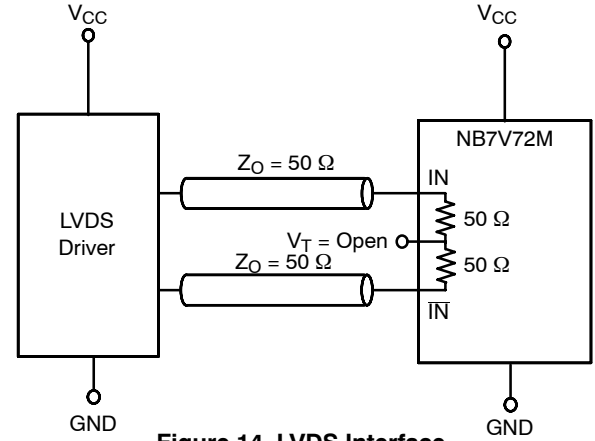


Figure 14. LVDS Interface

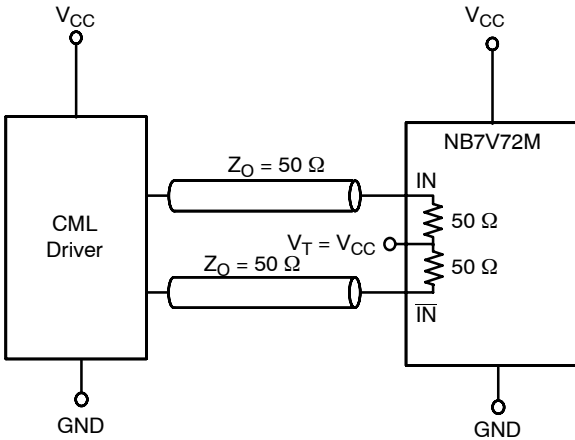


Figure 15. Standard 50  $\Omega$  Load CML Interface

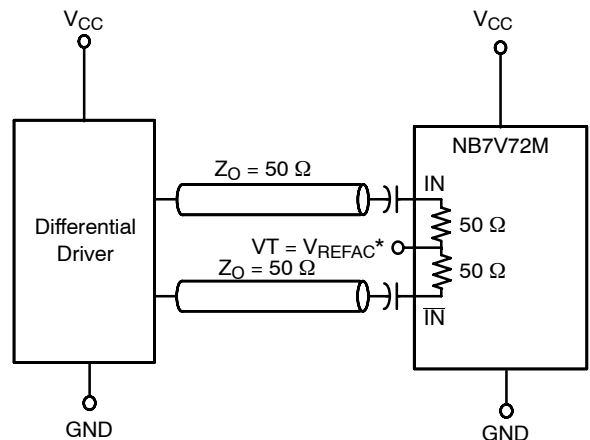


Figure 16. Capacitor-Coupled Differential Interface

( $V_T$  Connected to External  $V_{REFAC}$ )

\* $V_{REFAC}$  bypassed to ground with a 0.01  $\mu F$  capacitor

## ORDERING INFORMATION

Device	Package	Shipping†
NB7V72MMNG	QFN-16 (Pb-free)	123 Units / Rail
NB7V72MMNHTBG	QFN-16 (Pb-free)	100 / Tape & Reel
NB7V72MMNTXG	QFN-16 (Pb-free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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