

3.3 V Dual Differential LVPECL/LVDS to LVTTTL Translator

NB100ELT23L

Description

The NB100ELT23L is a dual differential LVPECL/LVDS to LVTTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23L makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23L is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the ELT23L does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the NB100ELT23L can accept any standard differential LVPECL/LVDS input referenced from a V_{CC} of +3.3 V.

Features

- 2.1 ns Typical Propagation Delay
- Maximum Operating Frequency > 160 MHz
- 24 mA LVTTTL Outputs
- Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.6 V with $GND = 0\text{ V}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



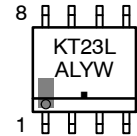
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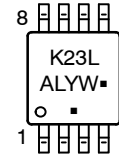
MARKING DIAGRAMS*



SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
NB100ELT23LDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NB100ELT23LDTG	TSSOP-8 (Pb-Free)	100 Units / Tube
NB100ELT23LDTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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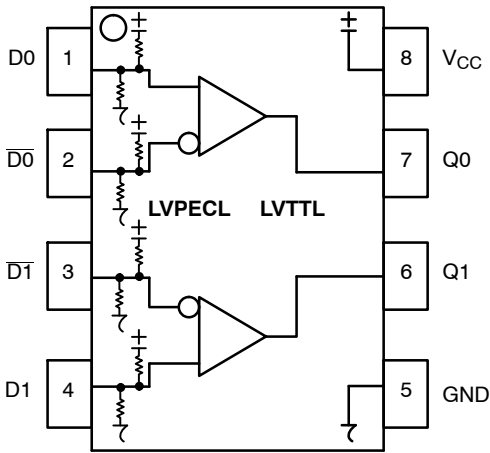


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	LVTTTL Outputs
D0*, D1* D0**, D1**	Differential LVPECL Inputs
V _{CC}	Positive Supply
GND	Ground

*Pins will default to $V_{CC}/2$ when left open. If connected to a common termination voltage under no signal conditions, then the device will be susceptible to self-oscillation.

**Pins will default to $2/3 V_{CC}$ when left open. If connected to a common termination voltage under no signal conditions, then the device will be susceptible to self-oscillation. See AND8020, Section 6 for options.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor D D-bar	50 kΩ 75 kΩ
Internal Input Pullup Resistor	50 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 TSSOP-8	Level 1 Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 1.25 in
Transistor Count	91 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Power Supply	GND = 0 V		3.8	V
V _I	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	3.8	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SO-8 SO-8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
T _{sol}	Wave Solder	Pb-Free	<2 to 3 sec @ 260°C	265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. PECL DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0 V (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CCH}	Power Supply Current (Outputs set to HIGH)	10	23	30	10	23	30	10	24	30	mA
I _{CCL}	Power Supply Current (Outputs set to LOW)	15	26	35	15	26	35	15	27	35	mA
V _{IH}	Input HIGH Voltage	2075		2420	2075		2420	2075		2420	mV
V _{IL}	Input LOW Voltage	1355		1675	1355		1675	1355		1675	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3)	1.2		3.3	1.2		3.3	1.2		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. All values vary 1:1 with V_{CC}.

3. V_{IHCMR} minimum varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. TTL DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V, T_A = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -3.0 mA	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 24 mA			0.5	V
I _{OS}	Output Short Circuit Current		-180		-50	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

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Table 6. AC CHARACTERISTICS $V_{CC} = 3.3\text{ V} \pm 5\%$, $GND = 0.0\text{ V}$ (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency	160			160			160			MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 5) $C_L = 20\text{ pF}$	1.55	1.9	2.95	1.55	1.9	2.95	1.55	1.9	3.25	ns
t_{SK++} , t_{SK--} , t_{SKPP}	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 6)			60 25 500			60 25 500			60 25 500	ps
t_{JITTER}	Random Clock Jitter (RMS)		6.0	20		6.0	20		6.0	20	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times $C_L = 20\text{ pF}$ (0.8 V to 2.0 V)	700 300	900	1700 1250	700 300	900	1700 1250	700 300	900	1700 1250	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $500\ \Omega$ to GND, $C_L = 20\text{ pF}$.
5. Reference ($V_{CC} = 3.3\text{ V} \pm 5\%$; $GND = 0\text{ V}$).
6. Skews are measured between outputs under identical conditions.

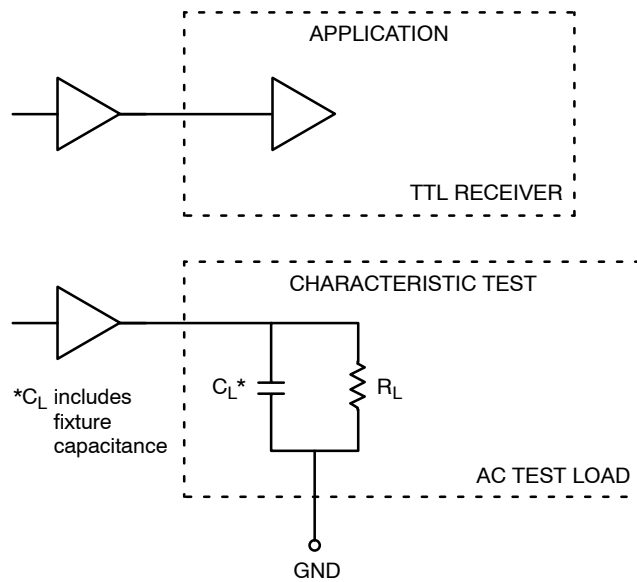


Figure 2. TTL Output Loading Used for Device Evaluation

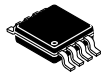
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

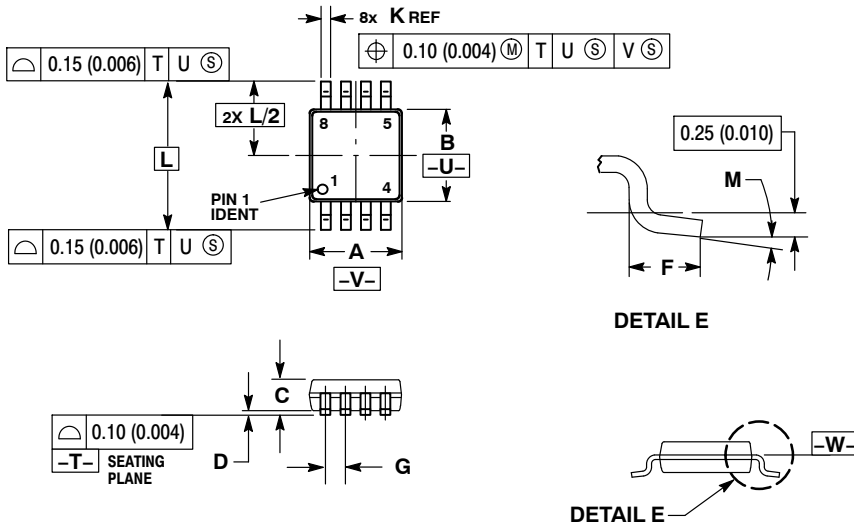
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TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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