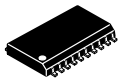
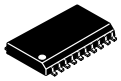
Inverting Octal 3-STATE Buffer, Octal 3-STATE Buffer

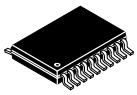
MM74HC540, MM74HC541



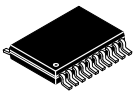
SOIC−20 WB
CASE 751D−05



SOIC−20, 300 mils
CASE 751BJ



TSSOP−20 WB
CASE 948E



TSSOP−20, 4.4x6.5
CASE 948AQ

General Description

The MM74HC540 and MM74HC541 3−STATE buffers utilize advanced silicon−gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS−TTL equivalent inputs.

The MM74HC540 is an inverting buffer and the MM74HC541 is a non−inverting buffer. The 3−STATE control gate operates as a two−input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are HIGH, all eight outputs are in the high−impedance state.

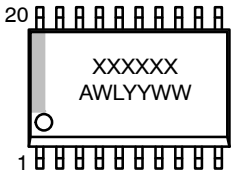
In order to enhance PC board layout, the MM74HC540 and MM74HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

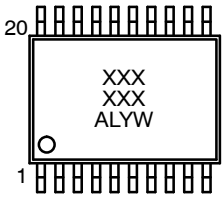
- Typical Propagation Delay: 12 ns
- 3−STATE Outputs for Connection to System Buses
- Wide Power Supply Range: 2−6 V
- Low Quiescent Current: 160 μA Maximum (74HC Series)
- Output Current: 6 mA
- These are Pb−Free Devices

MARKING DIAGRAMS

SOIC−20



TSSOP−20

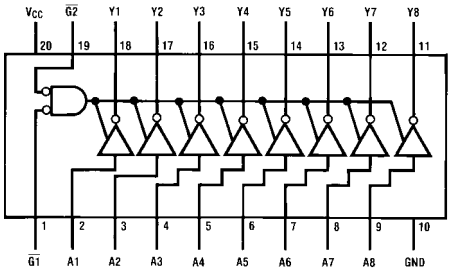


XXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot Number
Y	= Year
WW, YW	= Work Week

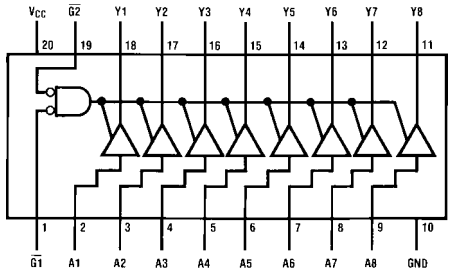
ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.



MM74HC540 (Top View)



MM74HC541 (Top View)

Figure 1. Connection Diagrams
(Pin Assignments for SOIC and TSSOP)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Rating		Value	Unit
V_{CC}	Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{CD}	Clamp Diode Current		±20	mA
I_{OUT}	DC Output Current, per pin		±35	mA
I_{CC}	DC V_{CC} or GND Current, per pin		±70	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
P_D	Power Dissipation	SOIC TSSOP	1302 833	mW
T_L	Lead Temperature (Soldering 10 seconds)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Rise or Fall Times	V_{CC} = 2.0 V	–	1000	ns
		V_{CC} = 4.5 V	–	500	ns
		V_{CC} = 6.0 V	–	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Unit
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0 V 4.5 V 6.0 V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum LOW Level Input Voltage		2.0 V 4.5 V 6.0 V		0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V V V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 V 4.5 V 6.0 V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	 4.5 V 6.0 V	 4.2 5.7	 3.98 5.48	 3.84 5.34	 3.7 5.2	V V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 V 4.5 V 6.0 V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	 4.5 V 6.0 V	 0.2 0.2	 0.26 0.26	 0.33 0.33	 0.4 0.4	V V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0 V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3−STATE Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}, $\overline{G} = V_{IH}$ $V_{OUT} = V_{CC}$ or GND	6.0 V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ μA	6.0 V		8.0	80	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	C_L = 45 pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	C_L = 45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	15	25	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.0 V to 6.0. V, C_L = 50 pF, $t_r = t_f$ = 6 ns, unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C		Unit
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	C_L = 50 pF C_L = 150 pF	2.0 V 2.0 V	55 83	100 150	126 190	149 224	ns ns
		C_L = 50 pF C_L = 150 pF	4.5 V 4.5 V	12 22	20 30	25 38	30 45	ns ns
		C_L = 50 pF C_L = 150 pF	6.0 V 6.0 V	11 18	17 26	21 32	25 38	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	C_L = 50 pF C_L = 150 pF	2.0 V 2.0 V	58 83	115 165	145 208	171 246	ns ns
		C_L = 50 pF C_L = 150 pF	4.5 V 4.5 V	14 17	23 33	29 42	34 49	ns ns
		C_L = 50 pF C_L = 150 pF	6.0 V 6.0 V	11 14	20 28	25 35	29 42	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF C_L = 150 pF	 2.0 V 4.5 V	 75 100	 150 200	 189 252	 224 298	 ns ns
		C_L = 50 pF C_L = 150 pF	4.5 V 4.5 V	15 30	30 40	38 50	45 60	ns ns
		C_L = 50 pF C_L = 150 pF	6.0 V 6.0 V	13 17	26 34	32 43	38 51	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0 V 4.5 V 6.0 V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0 V 4.5 V 6.0 V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 3)	$\overline{G}$ = V_{IH} $\overline{G}$ = V_{IL}		10 50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MM74HC540WM	HC540A	SOIC−20 WB (Pb−Free and Halide Free)	38 Units / Tube
MM74HC540WMX	HC540A		1000 / Tape & Reel
MM74HC540MTCX	HC 540A	TSSOP−20 WB (Pb−Free)	2500 / Tape & Reel
MM74HC541WM	HC541A	SOIC−20 WB (Pb−Free and Halide Free)	38 Units / Tube
MM74HC541WMX	HC541A	SOIC−20, 300 mils (Pb−Free and Halide Free)	1000 / Tape & Reel
MM74HC541MTC	HC 541A	TSSOP−20 WB (Pb−Free)	75 Units / Tube
MM74HC541MTCX	HC 541A	TSSOP20, 4.4 × 6.5 (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 4)

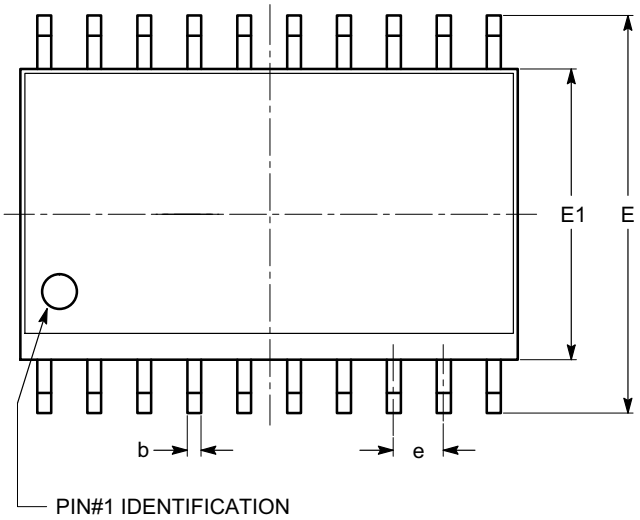
MM74HC540MTC	HC 540A	TSSOP−20 WB (Pb−Free)	75 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

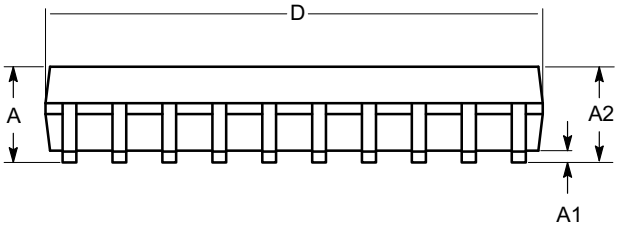
SOIC−20, 300 mils
CASE 751BJ
ISSUE O

DATE 19 DEC 2008

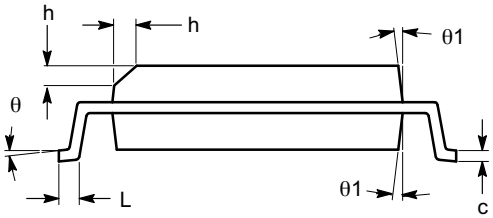


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40	0.81	1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW



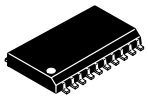
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

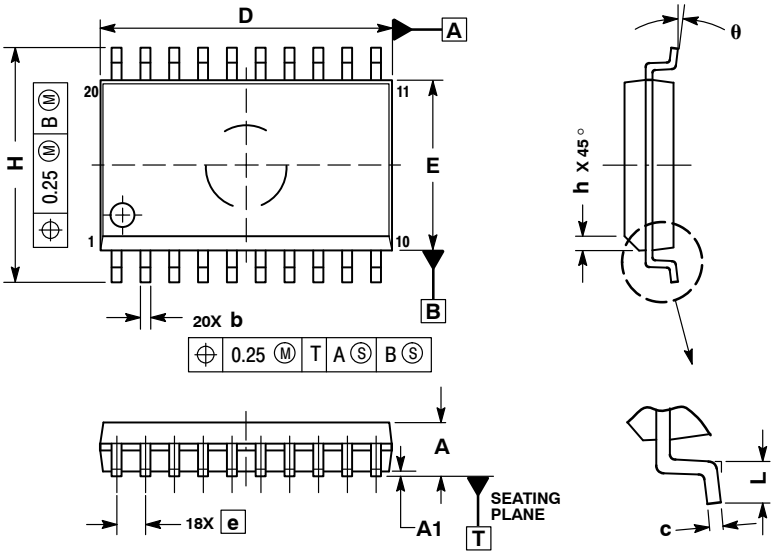
DOCUMENT NUMBER:	98AON34287E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−20, 300 MILS	PAGE 1 OF 1

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



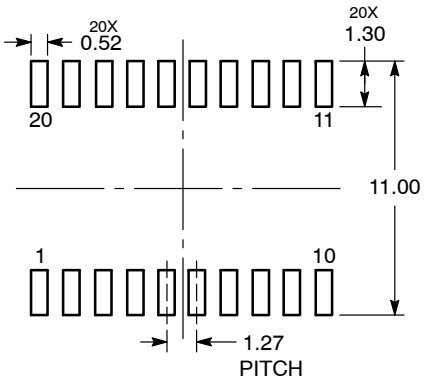
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

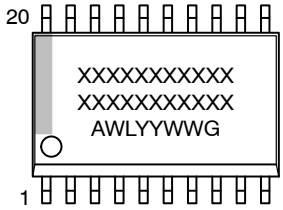
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



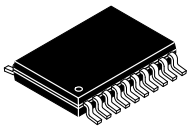
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

TSSOP–20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



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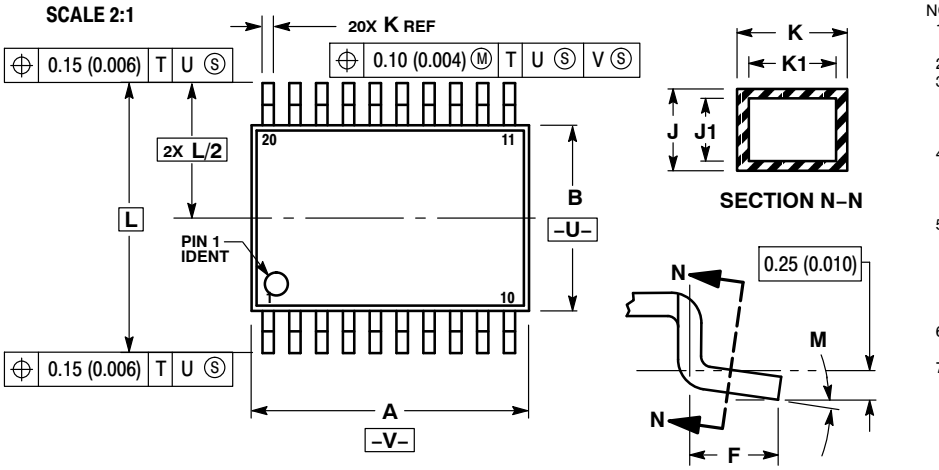
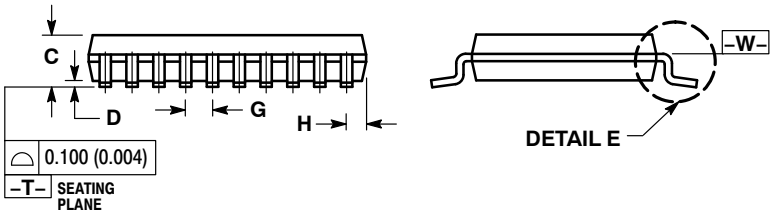


SECTION N–N

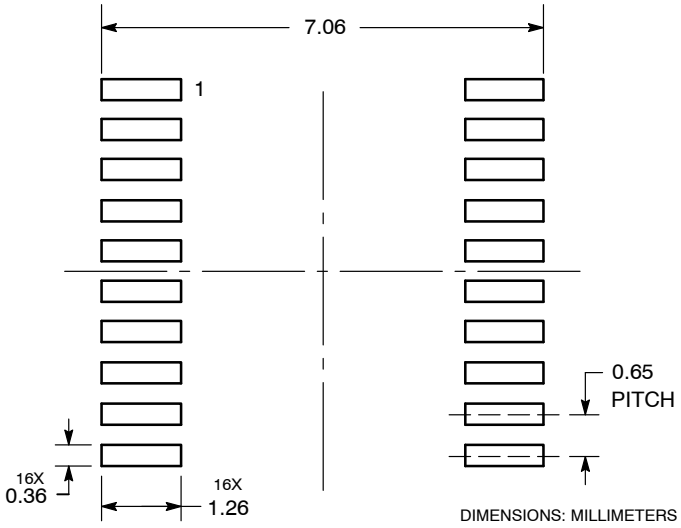
DETAIL E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

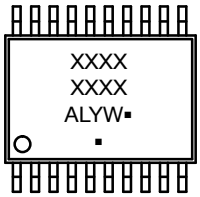
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

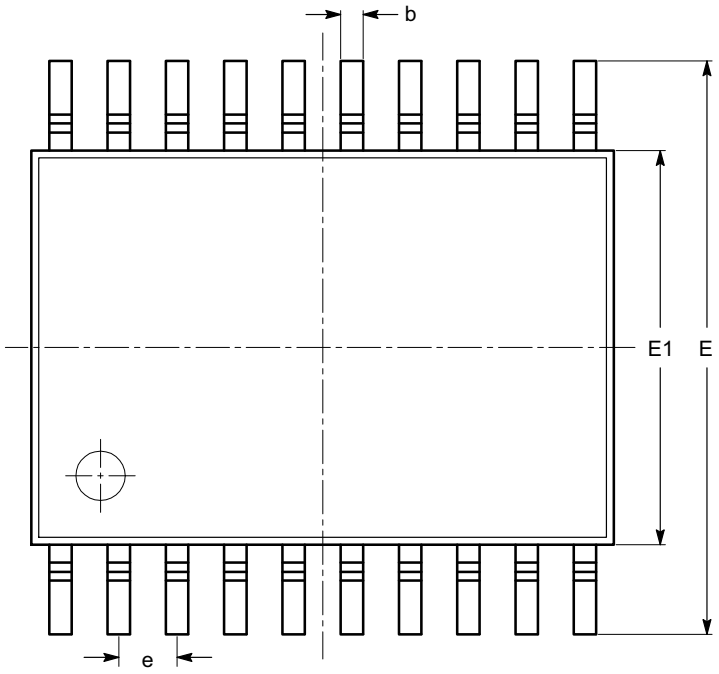
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70169A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**TSSOP–20 WB**		**PAGE 1 OF 1**

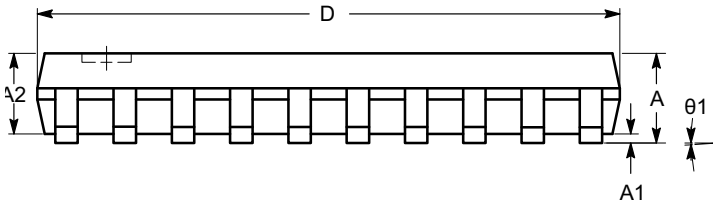
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

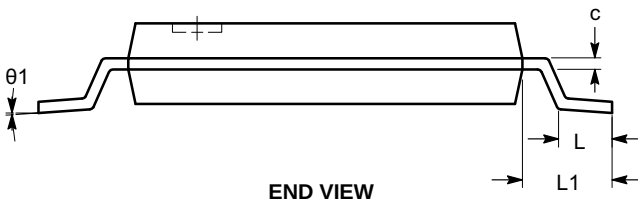


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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