

# MJW21193 (PNP) MJW21194 (NPN)

## Silicon Power Transistors

The MJW21193 and MJW21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

### Features

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	Vdc
Collector-Base Voltage	$V_{CBO}$	400	Vdc
Emitter-Base Voltage	$V_{EBO}$	5.0	Vdc
Collector-Emitter Voltage - 1.5 V	$V_{CEX}$	400	Vdc
Collector Current - Continuous	$I_C$	16	Adc
Collector Current - Peak (Note 1)	$I_{CM}$	30	Adc
Base Current - Continuous	$I_B$	5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	- 65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ .

### THERMAL CHARACTERISTICS

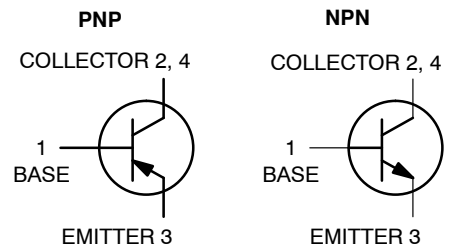
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$



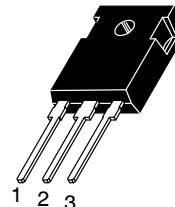
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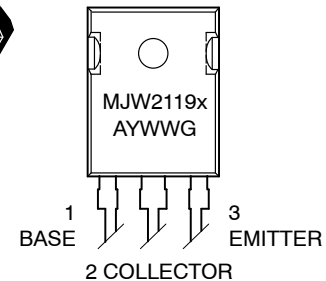
## 16 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS, 200 WATTS



### MARKING DIAGRAM



TO-247  
CASE 340L  
STYLE 3



x = 3 or 4  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
MJW21193G	TO-247 (Pb-Free)	30 Units/Rail
MJW21194G	TO-247 (Pb-Free)	30 Units/Rail

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	-	-	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 200 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	-	-	100	μAdc
Emitter Cutoff Current (V <sub>CE</sub> = 5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	-	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = 250 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc)	I <sub>CEX</sub>	-	-	100	μAdc

### SECOND BREAKDOWN

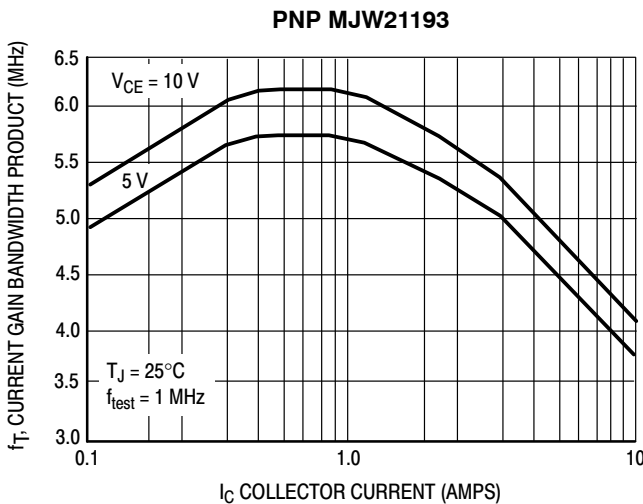
Second Breakdown Collector Current with Base Forward Biased (V <sub>CE</sub> = 50 Vdc, t = 1 s (non-repetitive)) (V <sub>CE</sub> = 80 Vdc, t = 1 s (non-repetitive))	I <sub>S/b</sub>	4.0 2.25	- -	- -	Adc
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### ON CHARACTERISTICS

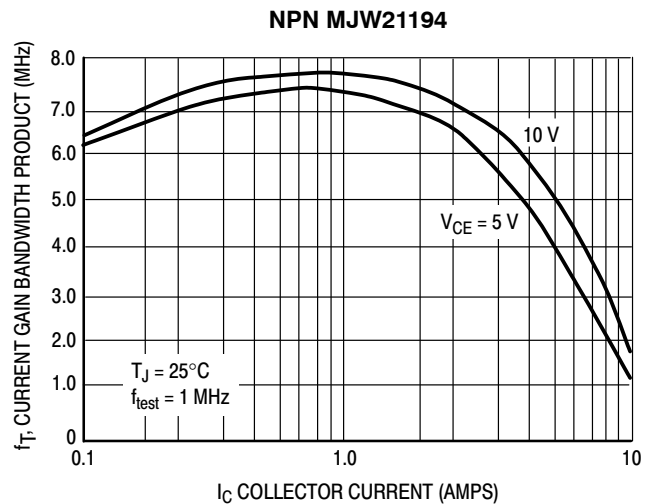
DC Current Gain (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 16 Adc, I <sub>B</sub> = 5 Adc)	h <sub>FE</sub>	20 8	- -	80 -	
Base-Emitter On Voltage (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc)	V <sub>BE(on)</sub>	-	-	2.2	Vdc
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.8 Adc) (I <sub>C</sub> = 16 Adc, I <sub>B</sub> = 3.2 Adc)	V <sub>CE(sat)</sub>	- -	- -	1.4 4	Vdc

### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output V <sub>RMS</sub> = 28.3 V, f = 1 kHz, P <sub>LOAD</sub> = 100 W <sub>RMS</sub> (Matched pair h <sub>FE</sub> = 50 @ 5 A/5 V)	h <sub>FE</sub> unmatched h <sub>FE</sub> matched	T <sub>HD</sub>	- -	0.8 0.08	- -	%
Current Gain Bandwidth Product (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 1 MHz)		f <sub>T</sub>	4	-	-	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1 MHz)		C <sub>ob</sub>	-	-	500	pF



**Figure 1. Typical Current Gain Bandwidth Product**

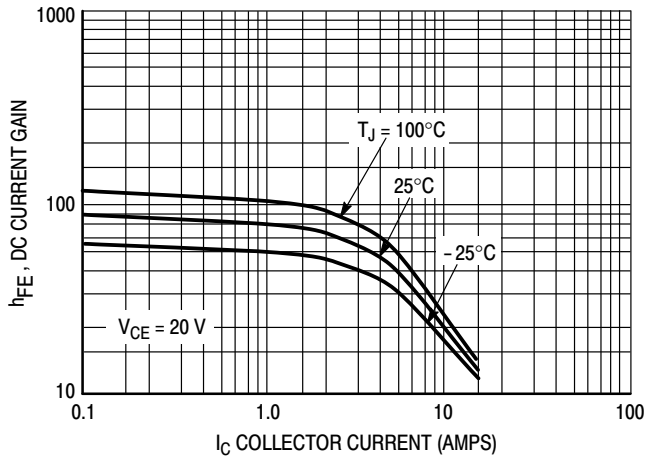


**Figure 2. Typical Current Gain Bandwidth Product**

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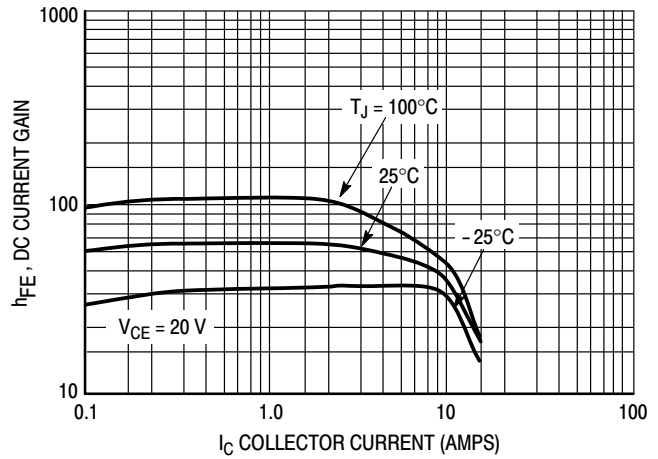
## TYPICAL CHARACTERISTICS

**PNP MJW21193**



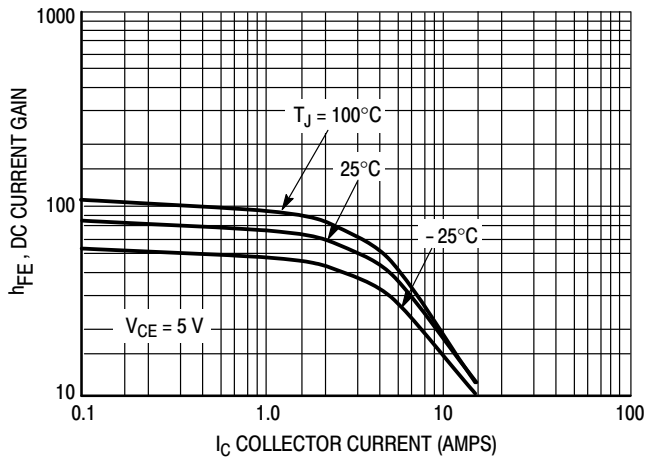
**Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$**

**NPN MJW21194**



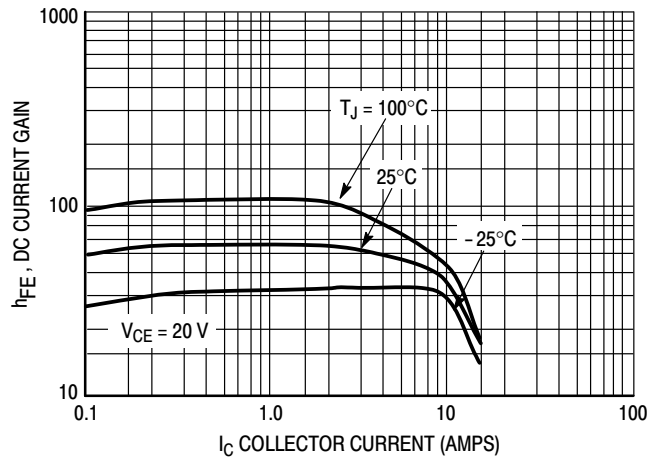
**Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$**

**PNP MJW21193**



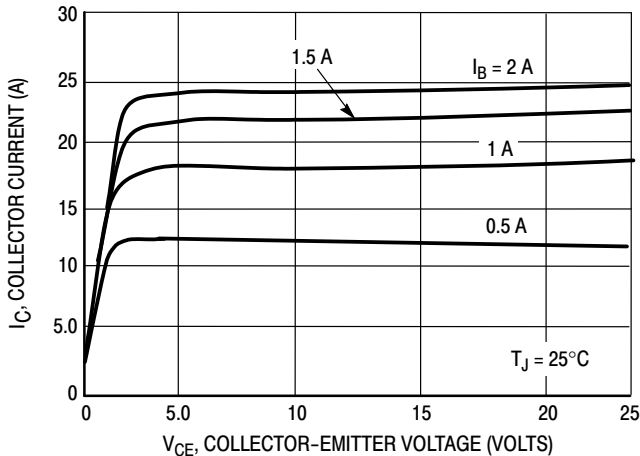
**Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$**

**NPN MJW21194**



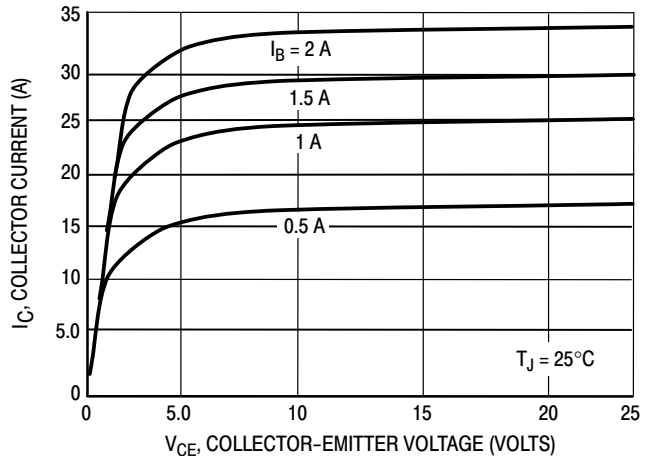
**Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$**

**PNP MJW21193**



**Figure 7. Typical Output Characteristics**

**NPN MJW21194**



**Figure 8. Typical Output Characteristics**

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## TYPICAL CHARACTERISTICS

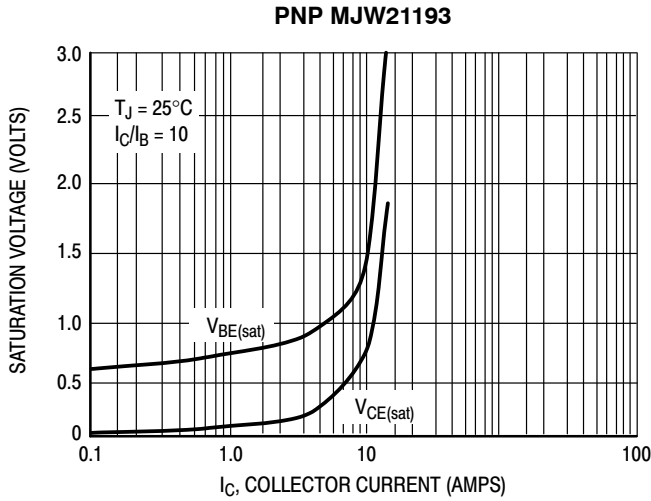


Figure 9. Typical Saturation Voltages

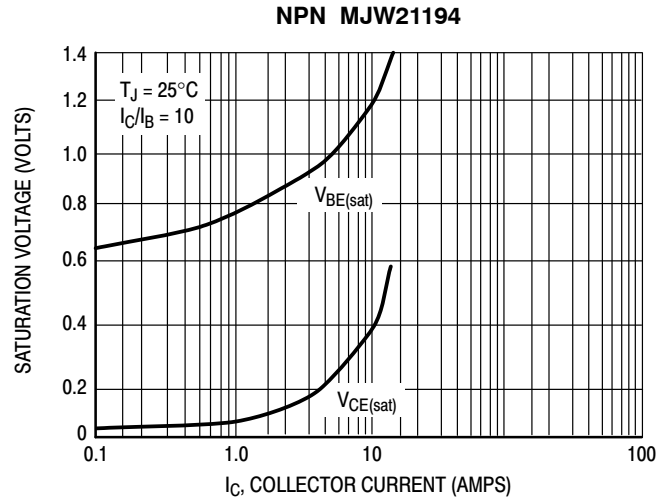


Figure 10. Typical Saturation Voltages

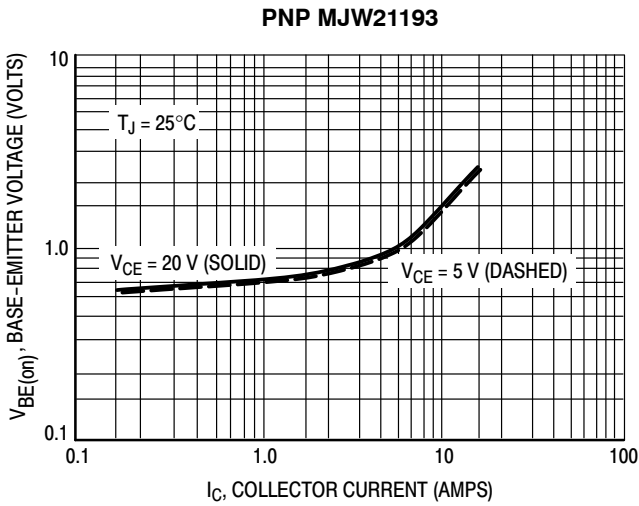


Figure 11. Typical Base-Emitter Voltage

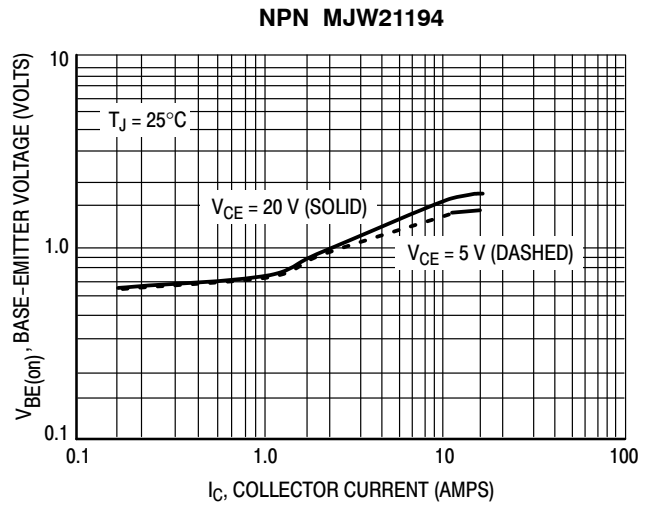


Figure 12. Typical Base-Emitter Voltage

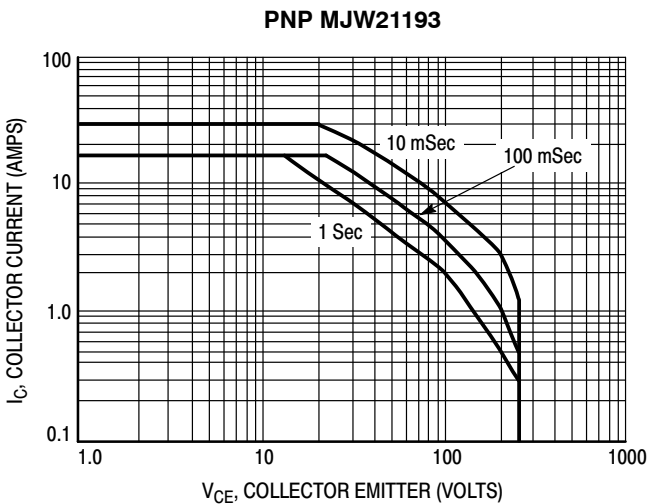


Figure 13. Active Region Safe Operating Area

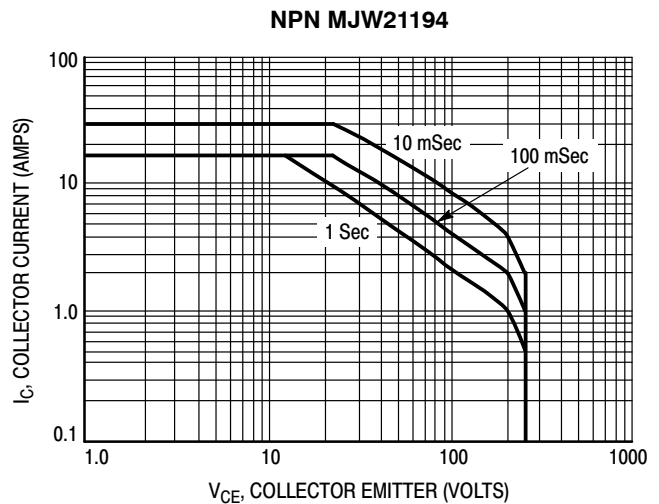


Figure 14. Active Region Safe Operating Area

## MJW21193 (PNP) MJW21194 (NPN)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

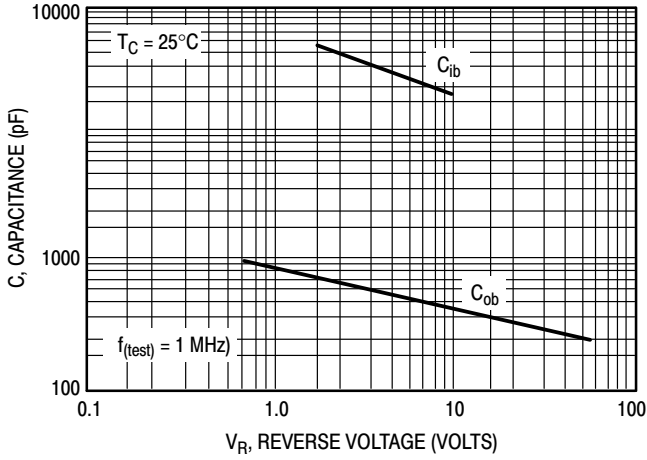


Figure 15. MJW21193 Typical Capacitance

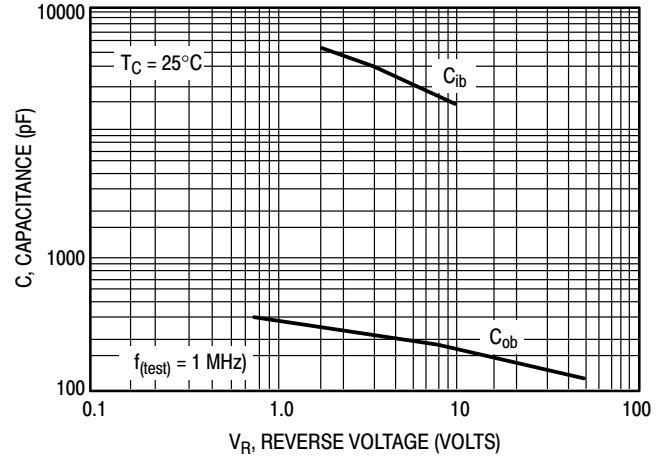


Figure 16. MJW21194 Typical Capacitance

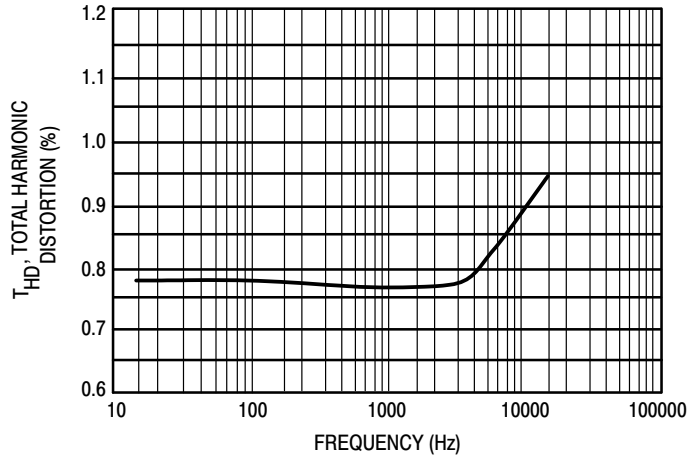
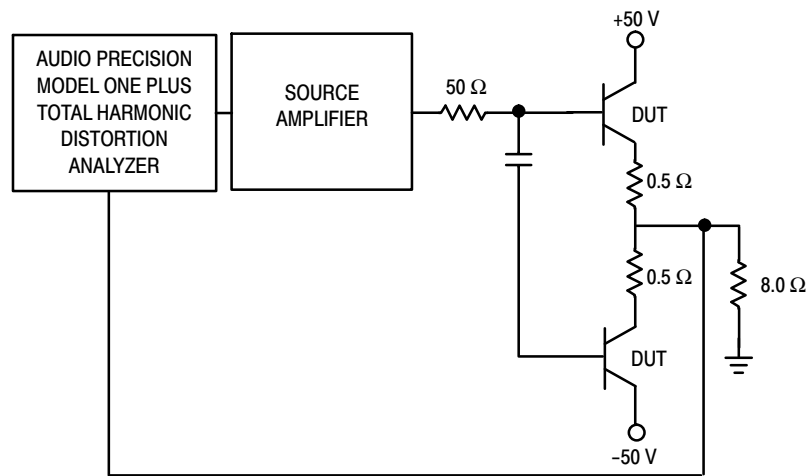


Figure 17. Typical Total Harmonic Distortion

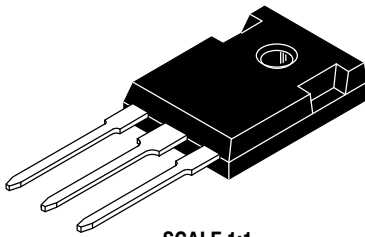
**MJW21193 (PNP) MJW21194 (NPN)**



**Figure 18. Total Harmonic Distortion Test Circuit**

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

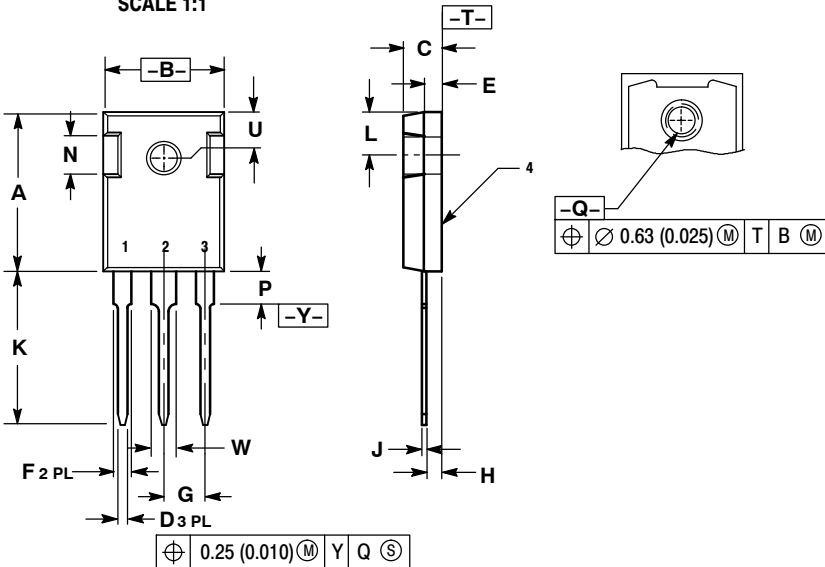
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TO-247  
CASE 340L-02  
ISSUE F

DATE 26 OCT 2011

SCALE 1:1

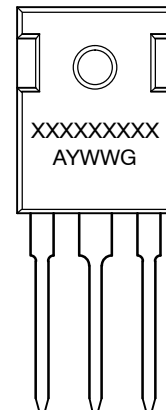


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>  | <p>STYLE 2:<br/>PIN 1. ANODE<br/>2. CATHODE (S)<br/>3. ANODE 2<br/>4. CATHODES (S)</p>               | <p>STYLE 3:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 4:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |
| <p>STYLE 5:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> | <p>STYLE 6:<br/>PIN 1. MAIN TERMINAL 1<br/>2. MAIN TERMINAL 2<br/>3. GATE<br/>4. MAIN TERMINAL 2</p> |  |  |

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	TO-247	PAGE 1 OF 2



ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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