MJF47G

High Voltage Power Transistor

Isolated Package Applications

Designed for line operated audio output amplifiers, switching power supply drivers and other switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

Features

- Electrically Similar to the Popular TIP47
- 250 $V_{CEO(sus)}$
- 1 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation
- This is a Pb−Free Device*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CB}	350	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (Note 1) Test No. 1 Per Figure 10 Test No. 2 Per Figure 11 Test No. 3 Per Figure 12 (for 1 sec, R.H. < 30%, T_A = 25°C)	V_{ISOL}	 4500 3500 1500	V
Collector Current − Continuous − Peak	I_C	1 2	Adc
Base Current − Continuous	I_B	0.6	Adc
Total Power Dissipation (Note 2) @ T_C = 25°C Derate above 25°C	P_D	28.4 0.227	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction−to−Case (Note 2)	$R_{\theta JC}$	4.4	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Proper strike and creepage distance must be provided.
2. Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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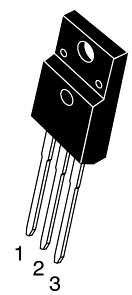
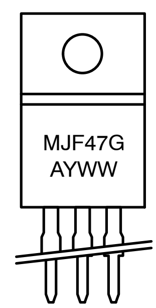
NPN SILICON
POWER TRANSISTOR
1 AMPERE
250 VOLTS, 28 WATTS



TO−220 FULLPACK
CASE 221D
STYLE 2

MARKING DIAGRAM



G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF47G	TO−220 FULLPACK (Pb−Free)	50 Units/Rail

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

October, 2012 − Rev. 6
Publication Order Number:
MJF47/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	−	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	−	0.2	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	I_{CES}	−	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	1	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)	h_{FE}	 30 10	 150 −	−
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	−	1	Vdc
Base−Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (I_C = 0.2 Adc, V_{CE} 10 Vdc, f = 2 MHz)	f_T	10	−	MHz

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

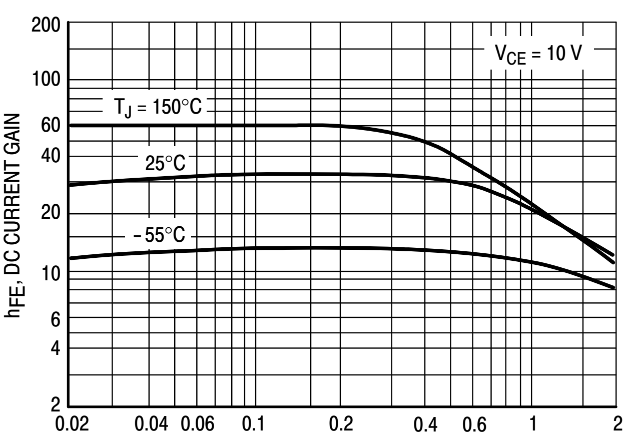


Figure 1. DC Current Gain

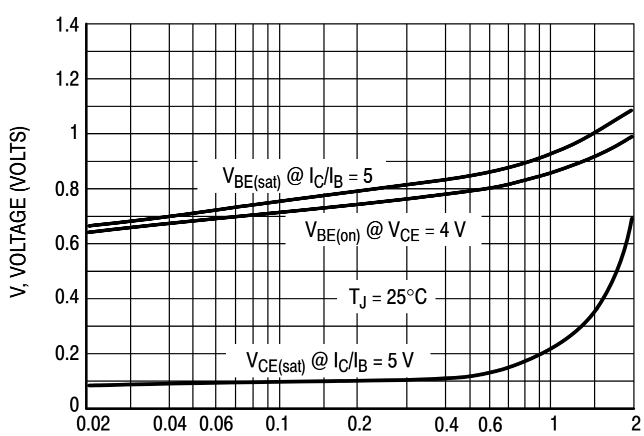


Figure 2. “On” Voltages

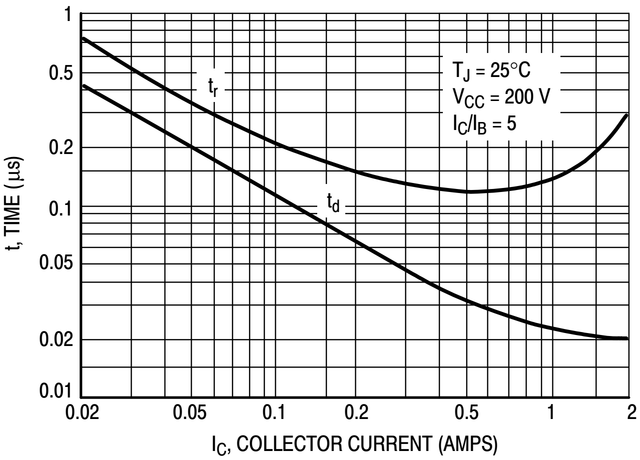


Figure 3. Turn−On Time

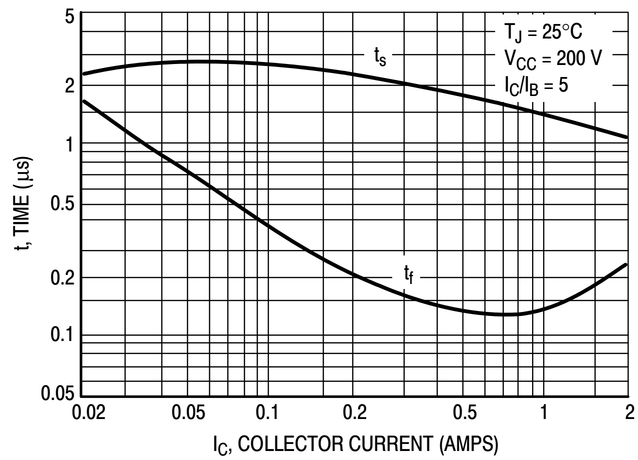


Figure 4. Turn−Off Time

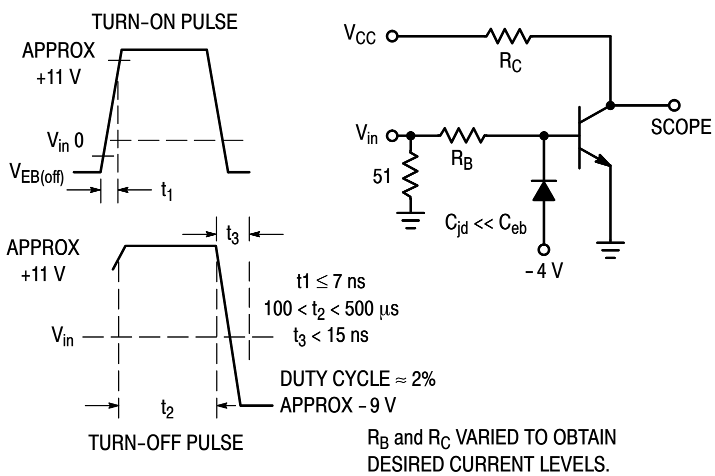


Figure 5. Switching Time Equivalent Circuit

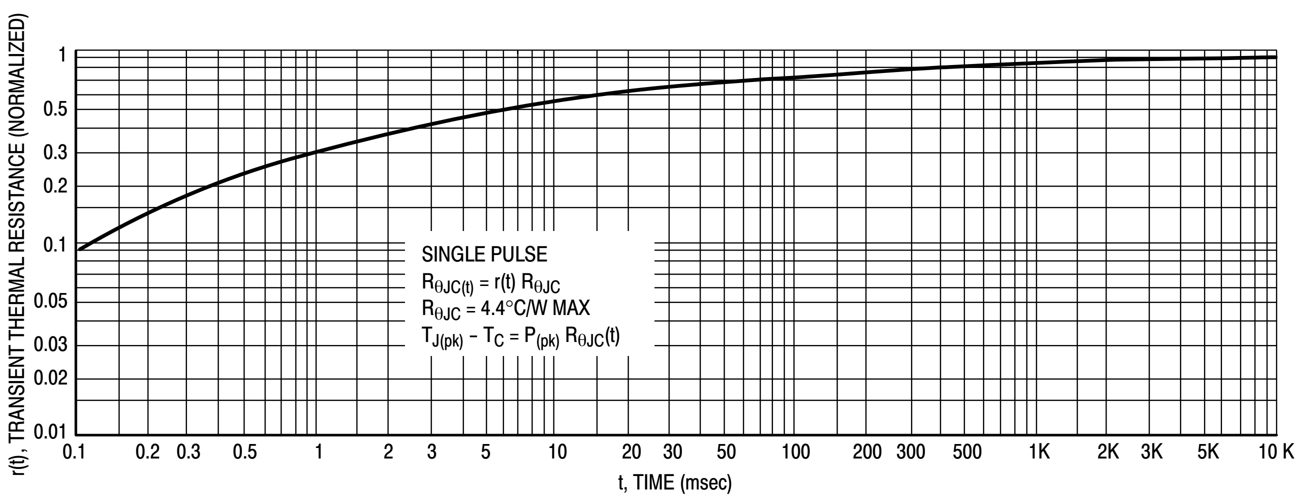


Figure 6. Thermal Response

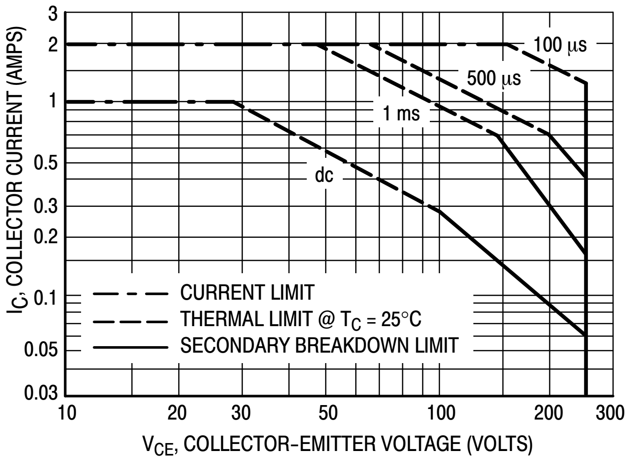


Figure 7. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

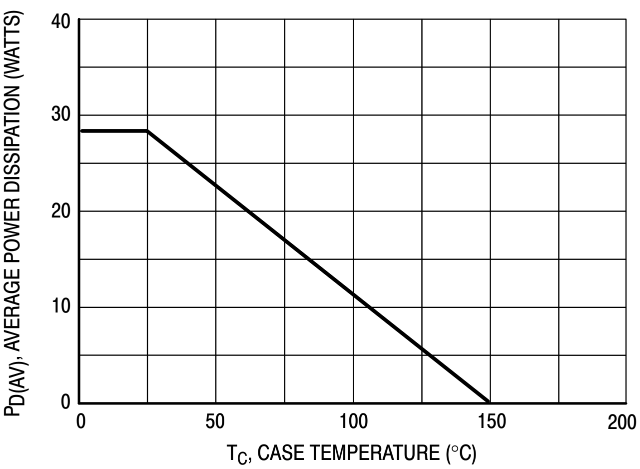


Figure 8. Power Derating

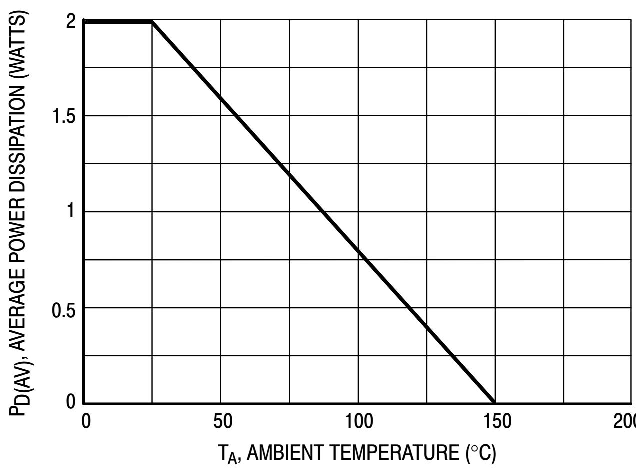


Figure 9. Power Derating

TEST CONDITIONS FOR ISOLATION TESTS*

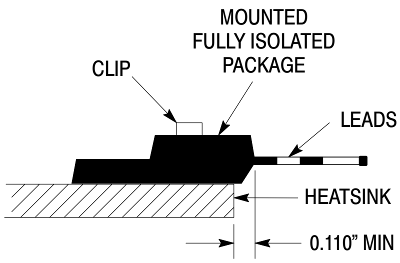


Figure 10. Clip Mounting Position for Isolation Test Number 1

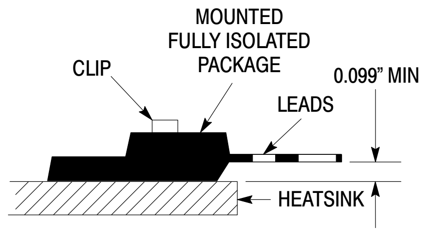


Figure 11. Clip Mounting Position for Isolation Test Number 2

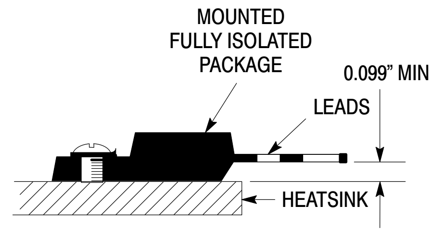


Figure 12. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

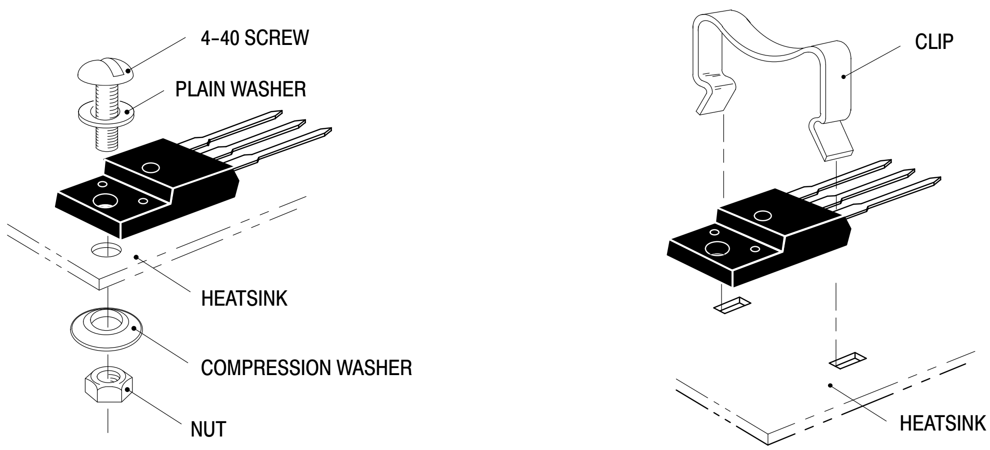


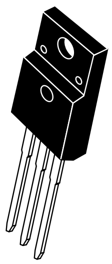
Figure 13. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

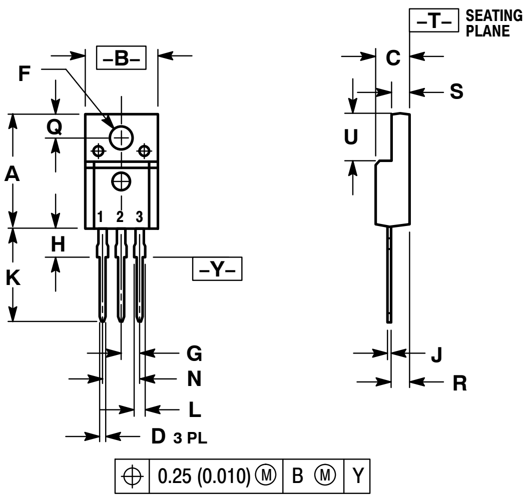
** For more information about mounting power semiconductors see Application Note AN1040.



SCALE 1:1

TO−220 FULLPAK
CASE 221D−03
ISSUE K

DATE 27 FEB 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

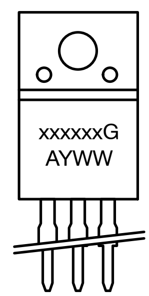
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

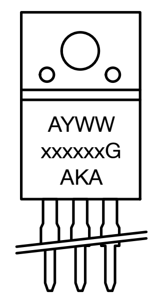
STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

MARKING DIAGRAMS



Bipolar



Rectifier

xxxxxx = Specific Device Code
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

A = Assembly Location
Y = Year
WW = Work Week
xxxxxx = Device Code
G = Pb−Free Package
AKA = Polarity Designator

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