MC74LCX257

Low-Voltage CMOS Quad 2-Input Multiplexer

With 5.0 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The MC74LCX257 is a high performance, quad 2−input multiplexer with 3−state outputs operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX257 inputs to be safely driven from 5.0 V devices.

Four bits of data from two sources can be selected using the Select input. The four outputs present the selected data in the true (non−inverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the Output Enable ($\overline{OE}$) input. Current drive capability is 24 mA at the outputs.
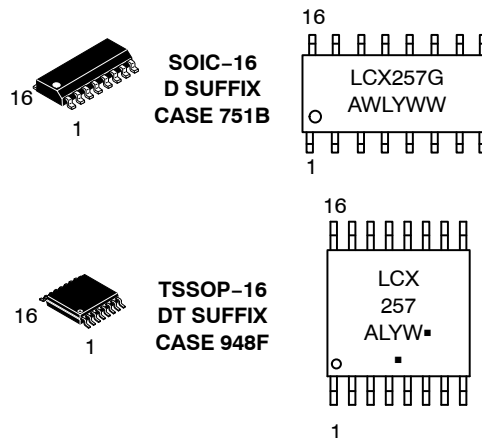
Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5.0 V Tolerant − Interface Capability with 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SOIC−16
D SUFFIX
CASE 751B

```
LCX257G
AWLYWW
```

TSSOP−16
DT SUFFIX
CASE 948F

```
LCX
257
ALYW■
```

A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.
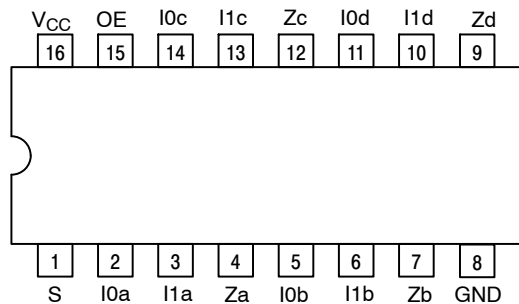
MC74LCX257

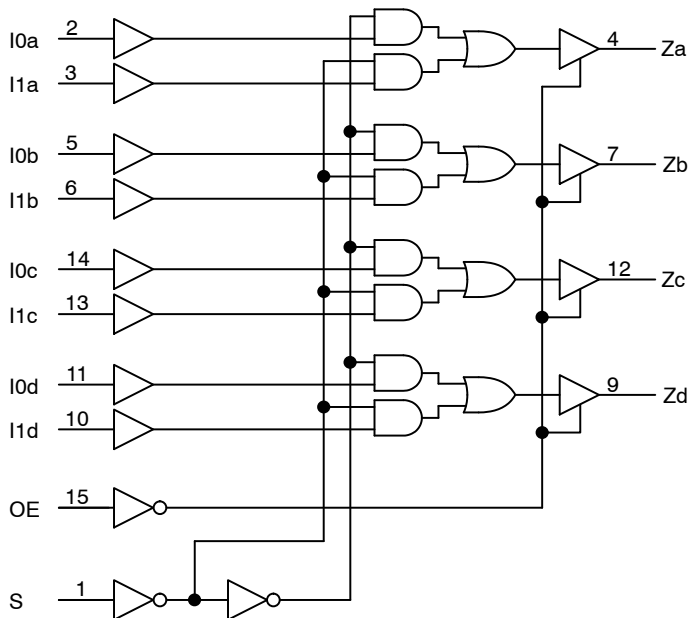**Figure 1. Pinout: 16−Lead Plastic Package**
(Top View)

Figure 2. Logic Diagram

PIN NAMES

Pins	Function
I0n	Source 0 Data Inputs
I1n	Source 1 Data Inputs
$\overline{OE}$	Output Enable Input
S	Select Input
Zn	Outputs

TRUTH TABLE

Inputs				Outputs
$\overline{OE}$	S	I0n	I1n	Zn
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High Voltage Level
L = Low Voltage Level
X = High or Low Voltage Level and Transitions are Acceptable
Z = High Impedance State

For ICC reasons, DO NOT FLOAT Inputs

MC74LCX257

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_I \leq +7.0$	Output in 3−State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Type	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3−State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current V_{CC} = 3.0 V – 3.6 V V_{CC} = 2.7 V – 3.0 V V_{CC} = 2.3 V – 2.7 V			−24 −12 −8	mA
I_{OL}	LOW Level Output Current V_{CC} = 3.0 V – 3.6 V V_{CC} = 2.7 V – 3.0 V V_{CC} = 2.3 V – 2.7 V			+24 +12 +8	mA
T_A	Operating Free−Air Temperature	−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0		10	ns/V

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74LCX257DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LCX257DTG	TSSOP−16 (Pb−Free)	96 Units / Rail
MC74LCX257DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units
V_{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V_{CC} ≤ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = −100 μA	V_{CC} − 0.2		V
		V_{CC} = 2.3 V; I_{OH} = −8 mA	1.8		
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 2.3 V; I_{OL} = 8 mA		0.6	
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 16 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_{OZ}	3−State Output Current	V_{CC} = 3.6 V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0 to 5.5 V		±5	μA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0, V_{IN} = 5.5 V or V_{OUT} = 5.5 V		10	μA
I_{IN}	Input Leakage Current	V_{CC} = 3.6 V, V_{IN} = 5.5 V or GND		±5	μA
I_{CC}	Quiescent Supply Current	V_{CC} = 3.6 V, V_{IN} = 5.5 V or GND		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.3 ≤ V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS t_R = t_F = 2.5 ns; R_L = 500 Ω

Symbol	Parameter	Waveform	Limits V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF Min	Max	V_{CC} = 2.7 V, C_L = 50 pF Min	Max	V_{CC} = 2.5 V ± 0.2 V, C_L = 30 pF Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay In to Zn	1	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	1.5 1.5	7.2 7.2	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn	1, 2	1.5 1.5	7.0 7.0	1.5 1.5	8.5 8.5	1.5 1.5	9.1 9.1	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	3	1.5 1.5	7.0 7.0	1.5 1.5	8.5 8.5	1.5 1.5	9.1 9.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time from High and Low Level	3	1.5 1.5	5.5 5.5	1.5 1.5	6.0 6.0	1.5 1.5	6.6 6.6	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

MC74LCX257

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	T_A = +25°C Typ	T_A = +25°C Max	Units
V_{OLP}	Dynamic LOW Peak Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		0.8 0.6		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		−0.8 −0.6		V

4. Number of outputs defined as "n". Measured with "n−1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF
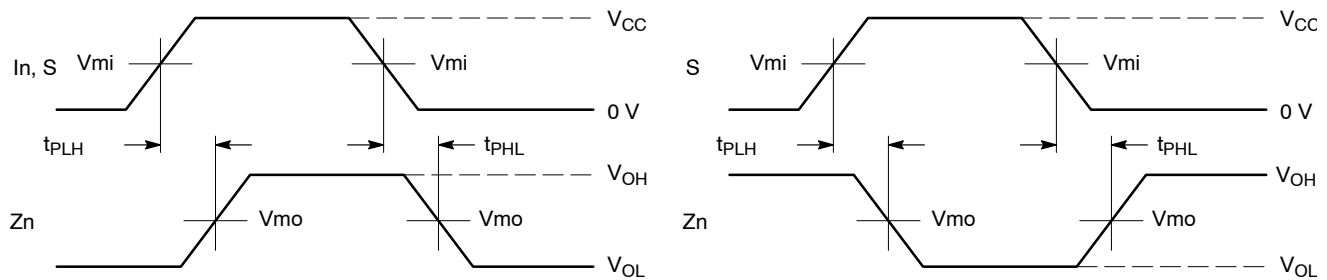
WAVEFORM 1 – NON–INVERTING PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1.0 MHz; t_W = 500 ns

WAVEFORM 2 – INVERTING PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1.0 MHz; t_W = 500 ns
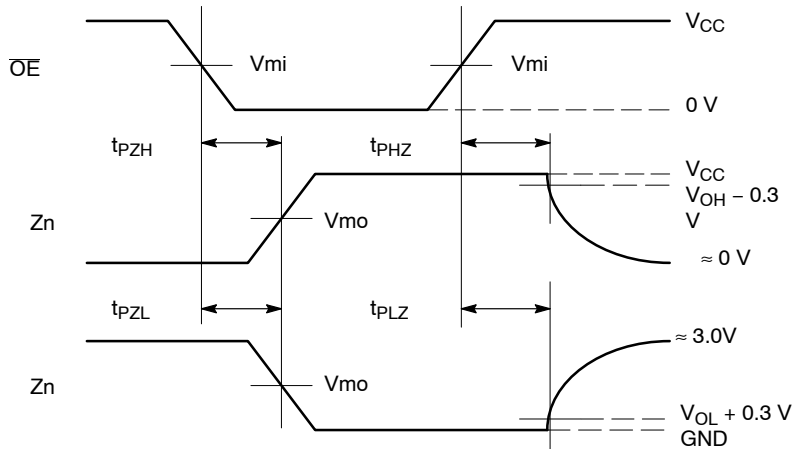
WAVEFORM 3 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1.0 MHz; t_W = 500 ns

Symbol	Vcc 3.3 V ± 0.3 V	Vcc 2.7 V	Vcc 2.5 V ± 0.2 V
Vmi	1.5 V	1.5 V	Vcc/2
Vmo	1.5 V	1.5 V	Vcc/2
V_{HZ}	V_{OL} + 0.3 V	V_{OL} + 0.3 V	V_{OL} + 0.15 V
V_{LZ}	V_{OH} − 0.3 V	V_{OH} − 0.3 V	V_{OH} − 0.15 V

Figure 3. AC Waveforms
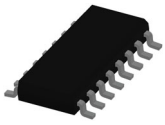
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
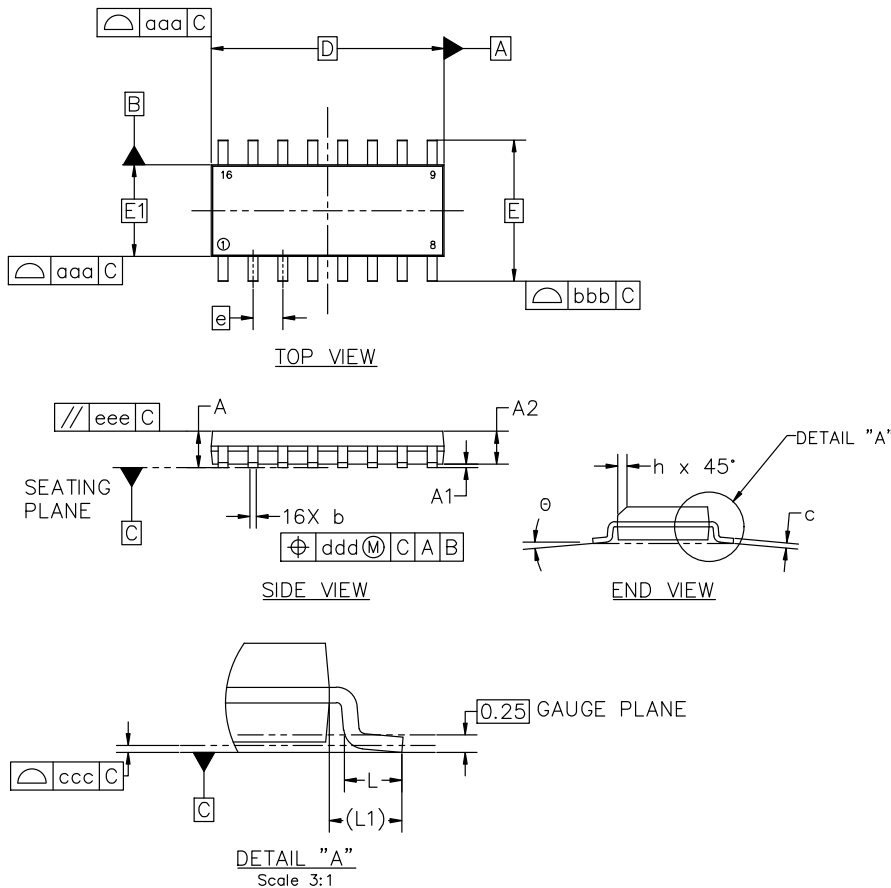
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	———	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	———	7°

TOLERANCE OF FORM AND POSITION	
aaa	0.10
bbb	0.20
ccc	0.10
ddd	0.25
eee	0.10

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE
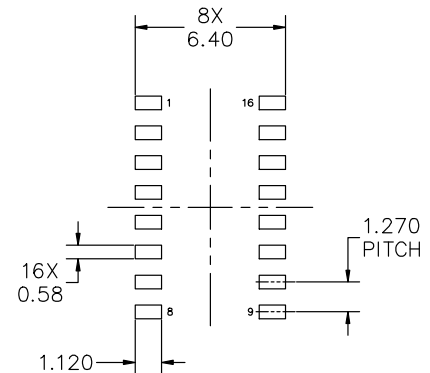
RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR
PB−FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
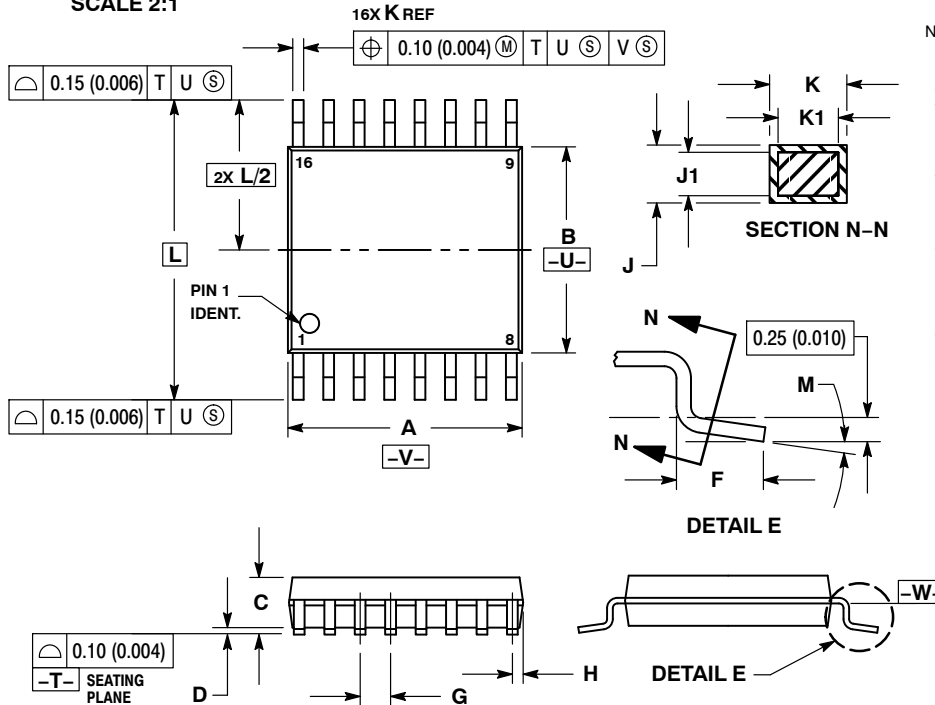AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
Y   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.

STYLE 1:
PIN 1. COLLECTOR
  2. BASE
  3. EMITTER
  4. NO CONNECTION
  5. EMITTER
  6. BASE
  7. COLLECTOR
  8. COLLECTOR
  9. BASE
  10. EMITTER
  11. NO CONNECTION
  12. EMITTER
  13. BASE
  14. COLLECTOR
  15. EMITTER
  16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
  2. ANODE
  3. NO CONNECTION
  4. CATHODE
  5. CATHODE
  6. NO CONNECTION
  7. ANODE
  8. CATHODE
  9. CATHODE
  10. ANODE
  11. NO CONNECTION
  12. CATHODE
  13. CATHODE
  14. NO CONNECTION
  15. ANODE
  16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
  2. BASE, #1
  3. EMITTER, #1
  4. COLLECTOR, #1
  5. COLLECTOR, #2
  6. BASE, #2
  7. EMITTER, #2
  8. COLLECTOR, #2
  9. COLLECTOR, #3
  10. BASE, #3
  11. EMITTER, #3
  12. COLLECTOR, #3
  13. COLLECTOR, #4
  14. BASE, #4
  15. EMITTER, #4
  16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
  2. COLLECTOR, #1
  3. COLLECTOR, #2
  4. COLLECTOR, #2
  5. COLLECTOR, #3
  6. COLLECTOR, #3
  7. COLLECTOR, #4
  8. COLLECTOR, #4
  9. BASE, #4
  10. EMITTER, #4
  11. BASE, #3
  12. EMITTER, #3
  13. BASE, #2
  14. EMITTER, #2
  15. BASE, #1
  16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
  2. DRAIN, #1
  3. DRAIN, #2
  4. DRAIN, #2
  5. DRAIN, #3
  6. DRAIN, #3
  7. DRAIN, #4
  8. DRAIN, #4
  9. GATE, #4
  10. SOURCE, #4
  11. GATE, #3
  12. SOURCE, #3
  13. GATE, #2
  14. SOURCE, #2
  15. GATE, #1
  16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
  2. CATHODE
  3. CATHODE
  4. CATHODE
  5. CATHODE
  6. CATHODE
  7. CATHODE
  8. CATHODE
  9. ANODE
  10. ANODE
  11. ANODE
  12. ANODE
  13. ANODE
  14. ANODE
  15. ANODE
  16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
  2. COMMON DRAIN (OUTPUT)
  3. COMMON DRAIN (OUTPUT)
  4. GATE P-CH
  5. COMMON DRAIN (OUTPUT)
  6. COMMON DRAIN (OUTPUT)
  7. COMMON DRAIN (OUTPUT)
  8. SOURCE P-CH
  9. SOURCE P-CH
  10. COMMON DRAIN (OUTPUT)
  11. COMMON DRAIN (OUTPUT)
  12. COMMON DRAIN (OUTPUT)
  13. GATE N-CH
  14. COMMON DRAIN (OUTPUT)
  15. COMMON DRAIN (OUTPUT)
  16. SOURCE N-CH

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		PAGE 2 OF 2

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

SCALE 2:1

16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

⬠ 0.15 (0.006) T U Ⓢ

2X **L/2**

L

PIN 1
IDENT.

16   9

16   9

1   8

⬠ 0.15 (0.006) T U Ⓢ

A
−V−

B
−U−

K
K1

J1

J

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

C

⬠ 0.10 (0.004)

−T− SEATING
PLANE

D   **G**   **H**

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
---	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
o ALYW

1
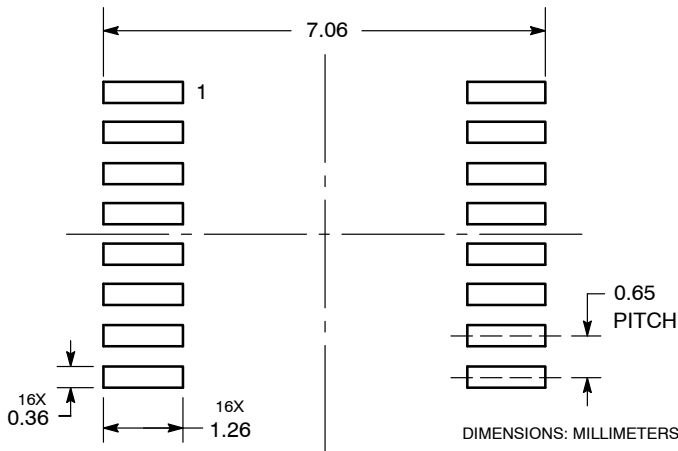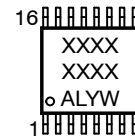
XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98ASH70247A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| DESCRIPTION: | TSSOP−16 | | PAGE 1 OF 1 |

ADDITIONAL INFORMATION

◊