# MC74HCT4094A

# 8-Bit Shift and Store Register with LSTTL Compatible Inputs

## High−Performance Silicon−Gate CMOS

The MC74HCT4094A is a high speed CMOS 8−bit serial shift and storage register. This device consists of an 8−bit shift register and latch with 3−state output buffers. Data is shifted on positive clock (CP) transitions. The data in the shift register is transferred to the storage register when the Strobe (STR) input is high. The output buffers are enabled when the Output Enable (OE) input is set high. Two serial outputs ($QS_1$, $QS_2$) are available for cascading multiple devices.

The MC74HCT4094A can be used to interface TTL or CMOS outputs to high speed CMOS inputs.

### Features

- Wide Operating Voltage Range: 4.5 to 5.5 V
- Low Power Dissipation: $I_{CC}$ = < 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- These are Pb−Free Devices

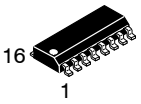
### Typical Applications

- Serial−to−Parallel Conversion
- Remote Control Storage Register

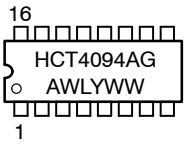
**ON Semiconductor®**

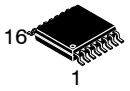
**http://onsemi.com**

**MARKING DIAGRAMS**

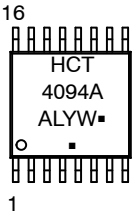



**SOIC−16**
**D SUFFIX**
**CASE 751B**




**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




| | | |
|---|---|---|
| A | = | Assembly Location |
| WL, L | = | Wafer Lot |
| YY, Y | = | Year |
| WW, W | = | Work Week |
| G, ▪ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

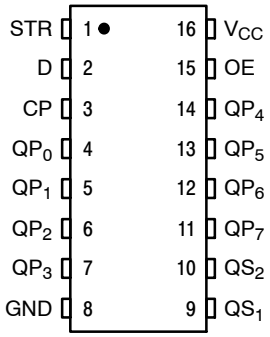



**Figure 1. Pin Assignment**

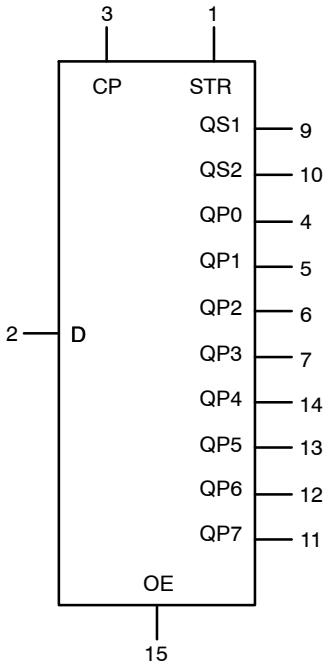



**Figure 2. Logic Symbol**

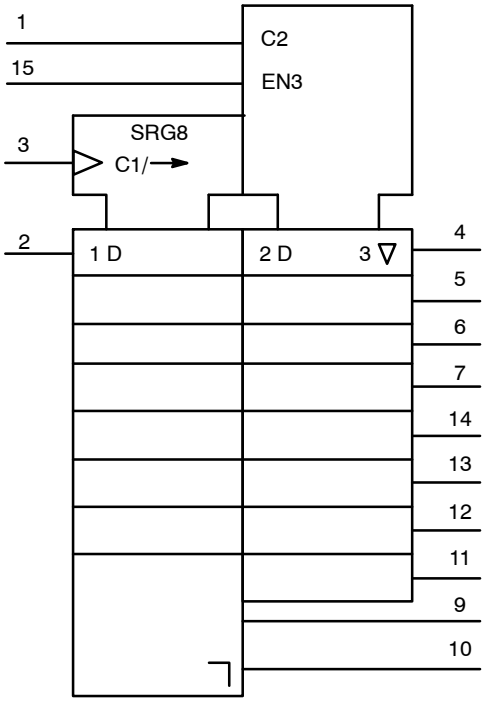



**Figure 3. IEC Logic Symbol**

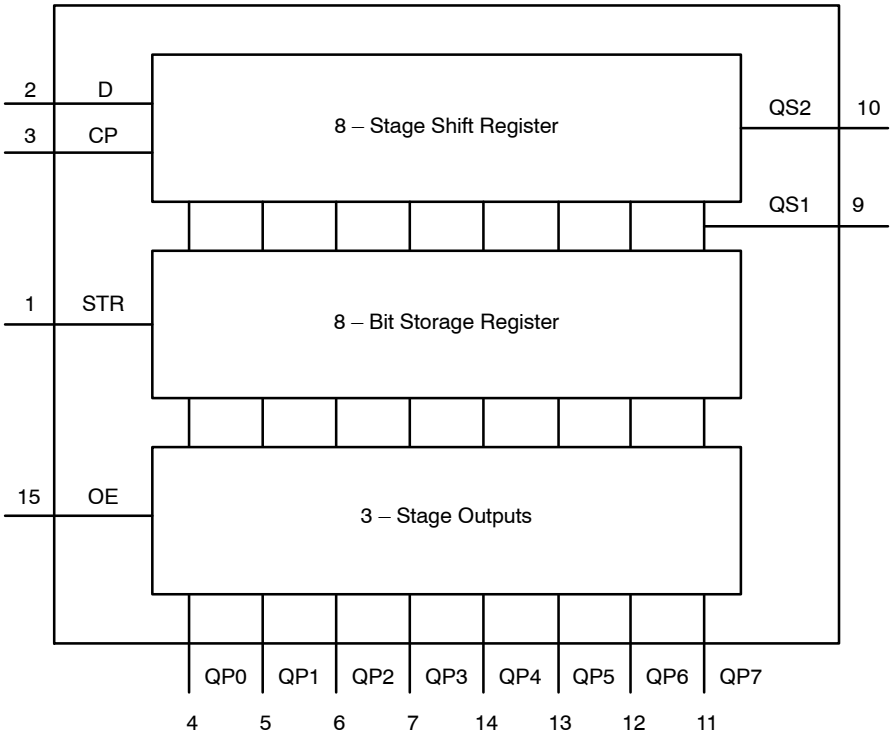



**Figure 4. Functional Diagram**

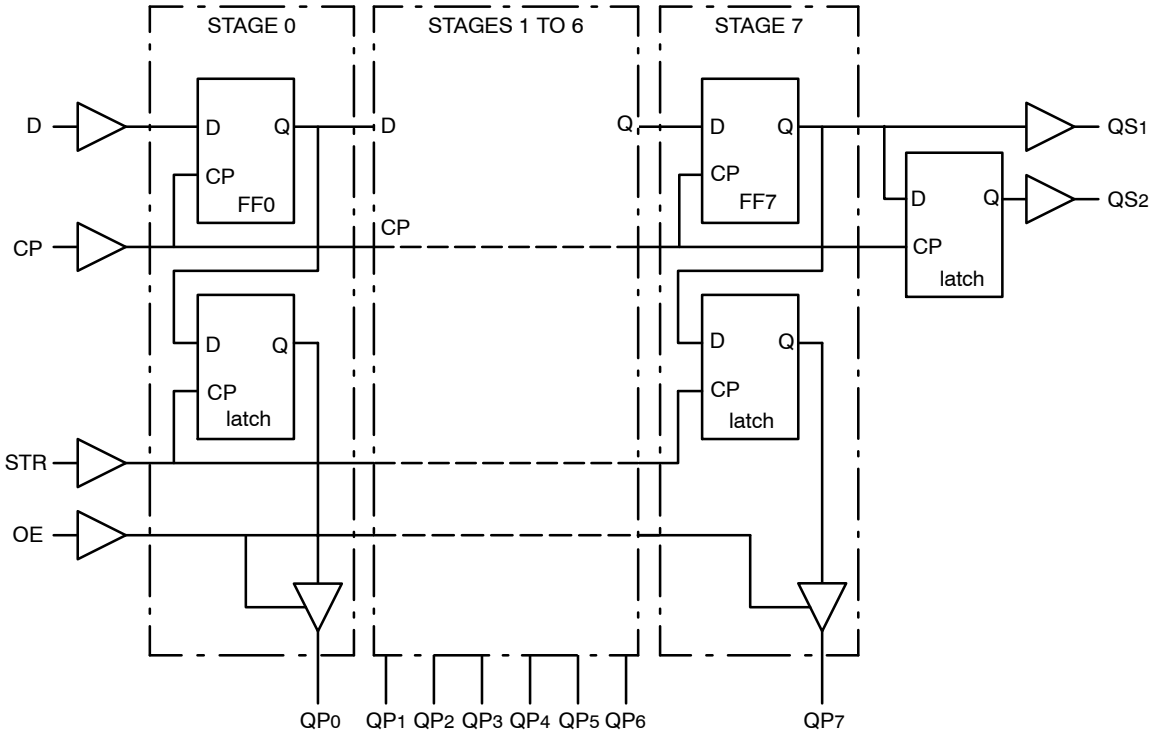



**Figure 5. Logic Diagram**

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 75 | mA |
| $P_D$ | Power Dissipation in Still Air, SOIC Package† | 500 | mW |
| | TSSOP Package† | 450 | |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating – SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | –55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

**FUNCTIONAL TABLE**

| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|---|---|---|---|---|---|---|---|
| **CP** | **OE** | **STR** | **D** | **QP0** | **QPn** | **QS1** | **QS2** |
| ↑ | L | X | X | Z | Z | Q'6 | NC |
| ↓ | L | X | X | Z | Z | NC | QP7 |
| ↑ | H | L | X | NC | NC | Q'6 | NC |
| ↑ | H | H | L | L | QPn−1 | Q'6 | NC |
| ↑ | H | H | H | H | QPn−1 | Q'6 | NC |
| ↓ | H | H | H | NC | NC | NC | QP7 |

**Notes**

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF−state
   NC = no change
   ↑ = LOW−to−HIGH CP transition
   ↓ = HIGH−to−LOW CP transition
   Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

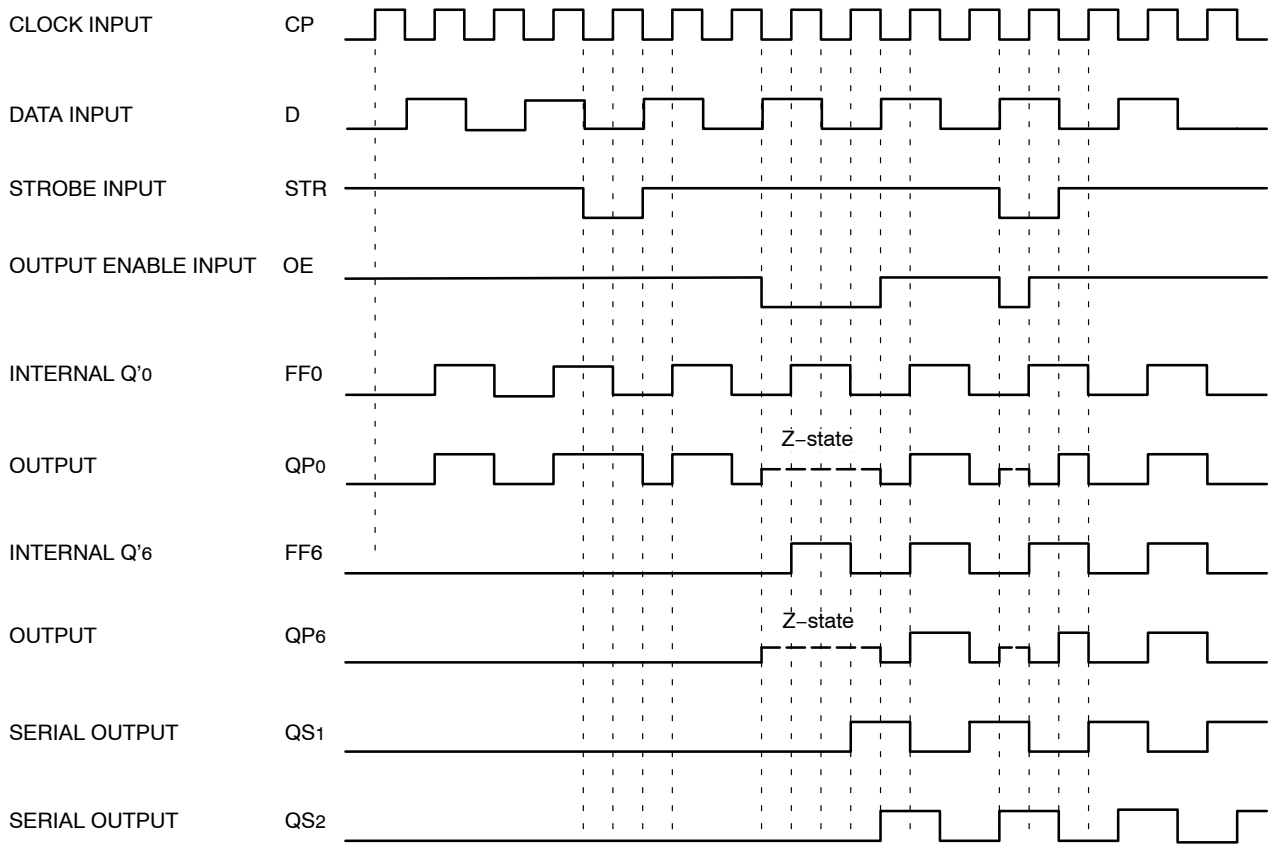



**Figure 6. Timing Diagram**

**DC CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | Guaranteed Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | −55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{OUT}\|$ ≤ 20 μA | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{OUT}\|$ ≤ 20 μA | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 20 μA | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | 5.4 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\|I_{OUT}\|$ = 6 mA | 4.5 | 4.25 | 4.2 | 4.1 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\|I_{OUT}\|$ ≤ 20 μA | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\|I_{OUT}\|$ = 6 mA | 4.5 | 0.25 | 0.3 | 0.4 | |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$ = $V_{CC}$ or GND | 5.5 | ±0.1 | ±1 | ±1 | μA |
| $I_{OZ}$ | Maximum Tri−State Output Leakage Current | $V_{IN}$ = $V_{CC}$ or GND<br>$V_{OUT}$ = $V_{CC}$ or GND | 5.5 | ±0.5 | ±5 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | 5.5 | 4.0 | 40 | 80 | μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0μA | | ≥ −55°C | 25 to 125°C | |
| | | | 5.5 | 2.9 | 2.4 | mA |

**AC CHARACTERISTICS** ($t_f = t_r = 6$ ns, $C_L = 50$ pF)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | Guaranteed Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | −55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay CP to $QS_1$ | Figure 7 | 4.5 | 30 | 38 | 45 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay CP to $QS_2$ | Figure 7 | 4.5 | 27 | 34 | 41 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay CP to $QP_n$ | Figure 7 | 4.5 | 39 | 49 | 59 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay STR to $QP_n$ | Figure 8 | 4.5 | 36 | 45 | 54 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum 3−State Output Enable Time OE to $QP_n$ | Figure 9 | 4.5 | 35 | 44 | 53 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum 3−State Output Enable Time OE to $QP_n$ | Figure 9 | 4.5 | 25 | 31 | 38 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Transition Time | Figure 7 | 4.5 | 18 | 22 | 25 | ns |
| $t_W$ | Minimum Clock Pulse Width High or Low | Figure 7 | 4.5 | 16 | 20 | 24 | ns |
| $t_W$ | Minimum Strobe Pulse Width High | Figure 8 | 4.5 | 16 | 20 | 24 | ns |
| $t_{SU}$ | Minimum Set−up Time D to CP | Figure 10 | 4.5 | 10 | 13 | 15 | ns |
| $t_{SU}$ | Minimum Set−up Time CP to STR | Figure 8 | 4.5 | 20 | 25 | 30 | ns |
| $t_h$ | Minimum Hold Time D to CP | Figure 10 | 4.5 | 3 | 3 | 3 | ns |
| $t_h$ | Minimum Hold Time CP to STR | Figure 8 | 4.5 | 0 | 0 | 0 | ns |
| $f_{MAX}$ | Minimum Clock Pulse Frequency | Figure 7 | 4.5 | 30 | 24 | 20 | MHz |
| $C_{in}$ | Maximum Input Capacitance | | – | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Output Capacitance | | – | 15 | 15 | 15 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 2) | | – | 140 | 140 | 140 | pF |

2. $C_{PD}$ is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC}(\text{operating}) \approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $N_{SW}$ = total number of outputs switching and $f_{IN}$ = switching frequency.

## AC WAVEFORMS

($V_M$ = 1.3 V)

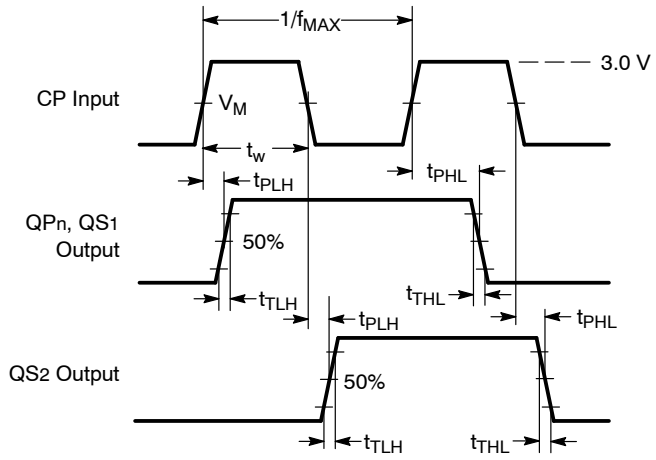



**Figure 7. Waveforms showing the clock (CP) to output (QPn, QS1, QS2) propagation delays, the clock pulse width and the maximum clock frequency.**

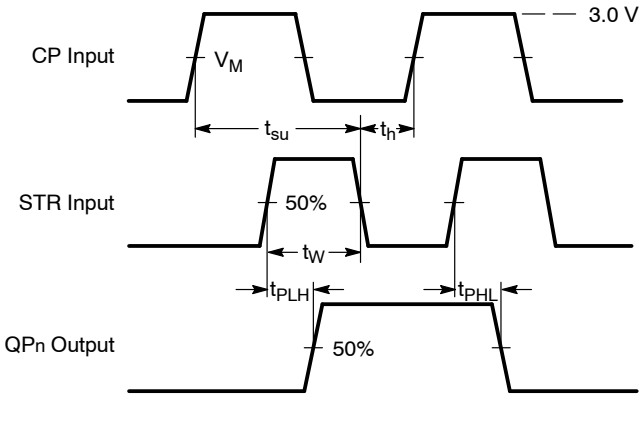



**Figure 8. Waveforms showing the strobe (STR) to output (QPn) propagation delays, the strobe pulse width, the clock set−up and hold times for the strobe input.**

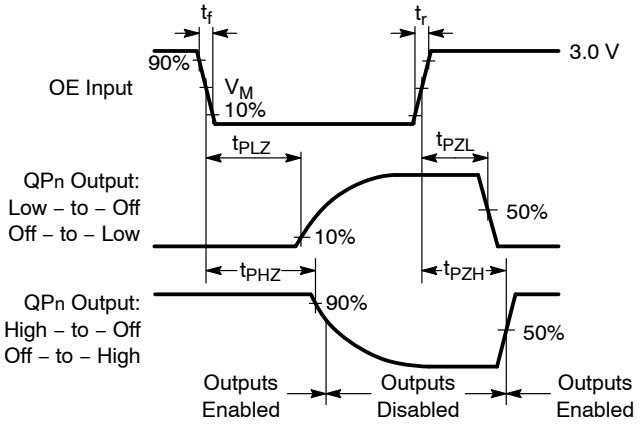
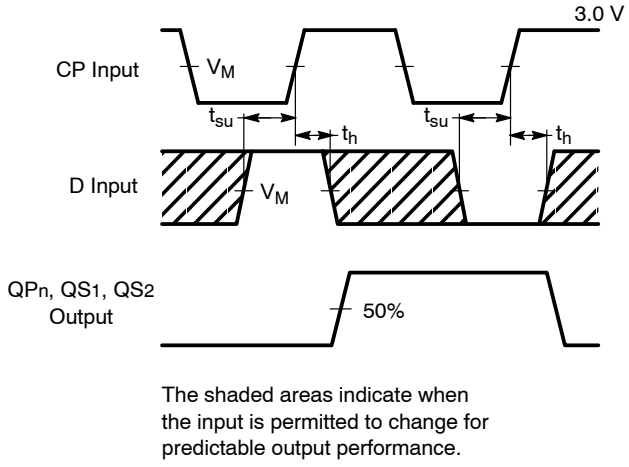



**Figure 9. Waveforms showing the 3−state enable and disable times for input OE.**




The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 10. Waveforms showing the data set−up and hold times for the data input.**

## TEST CIRCUITS

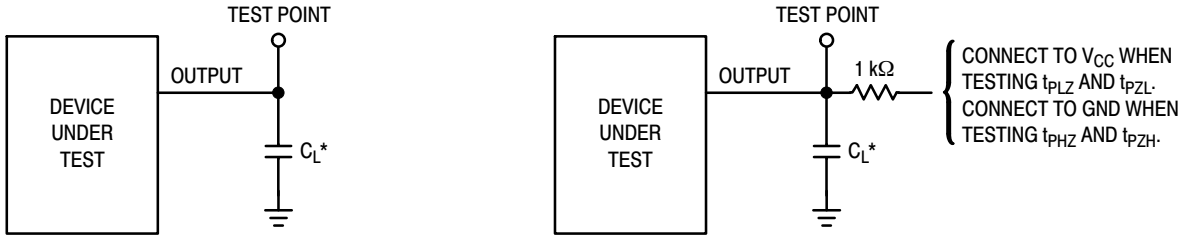
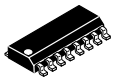



**Figure 11. AC Characteristics Load Circuits**

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74HCT4094ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74HCT4094ADR2G | SOIC−16 (Pb−Free) | 2500 Tape & Reel |
| MC74HCT4094ADT | TSSOP−16* | 96 Units / Rail |
| MC74HCT4094ADTR2G | TSSOP−16* | 2500 Tape & Reel |

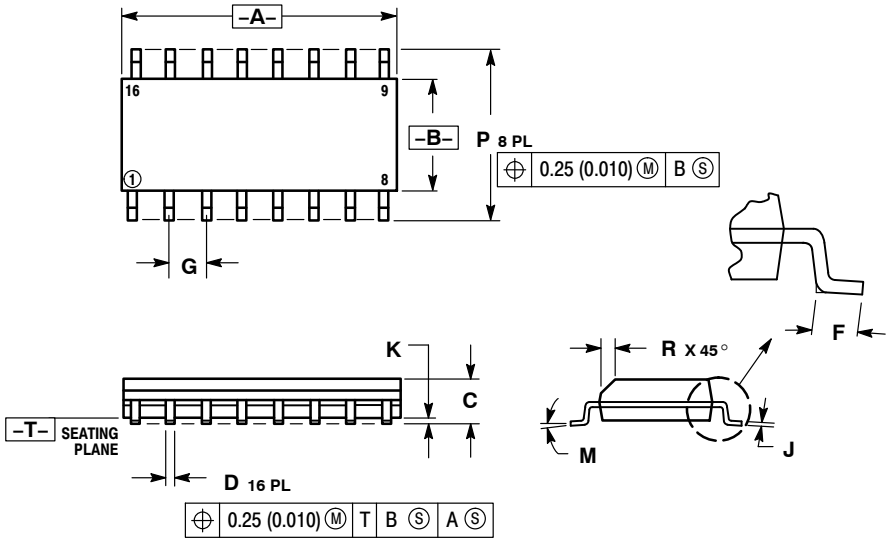
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.



SCALE 1:1

**SOIC–16**
CASE 751B–05
ISSUE K

DATE 29 DEC 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

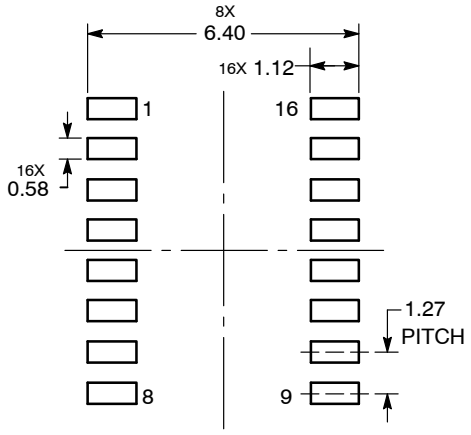
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

**SOLDERING FOOTPRINT**

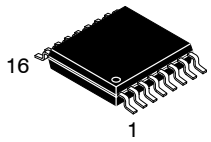



DIMENSIONS: MILLIMETERS

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOIC–16 | PAGE 1 OF 1 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

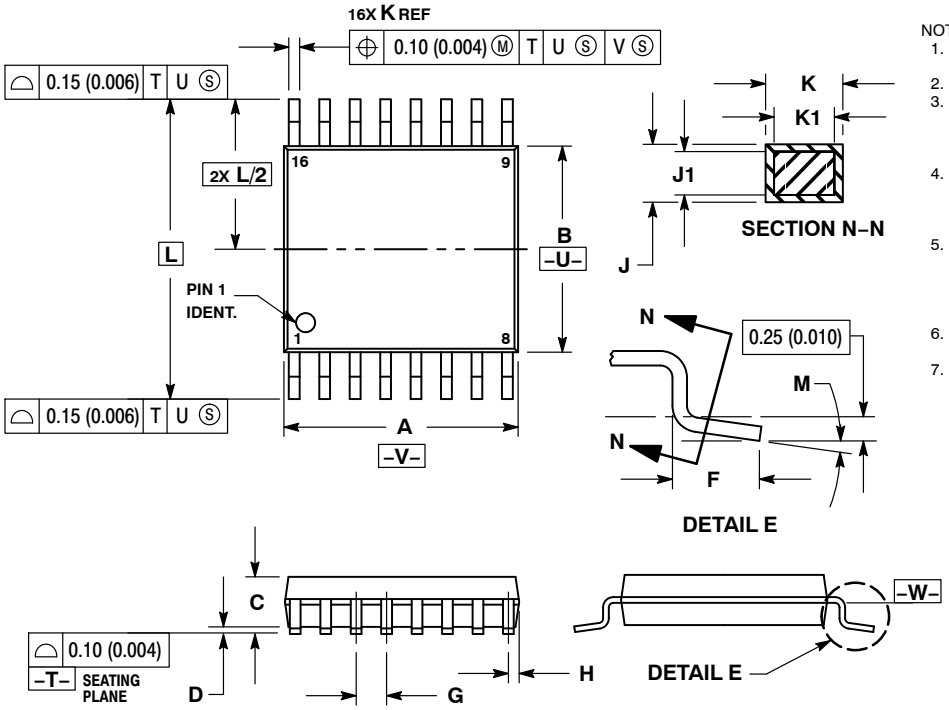
ON Semiconductor®




SCALE 2:1

**TSSOP−16**
CASE 948F−01
ISSUE B

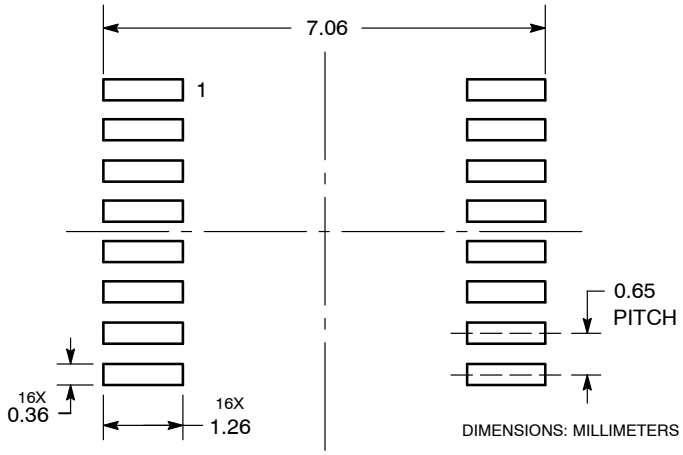
DATE 19 OCT 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

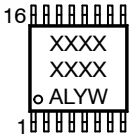
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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