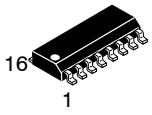
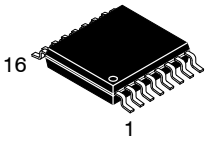
8-Bit Serial or Parallel-Input/ Serial-Output Shift Register

High−Performance Silicon−Gate CMOS

MC74HC165A, MC74HCT165A



SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F

QFN16
MN SUFFIX
CASE 485AW

The MC74HC165A/MC74HCT165A is identical in pinout to the LS165. The MC74HC165A inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT165A may be used as a level converter for interfacing TTL or NMOS outputs to High−Speed CMOS inputs.

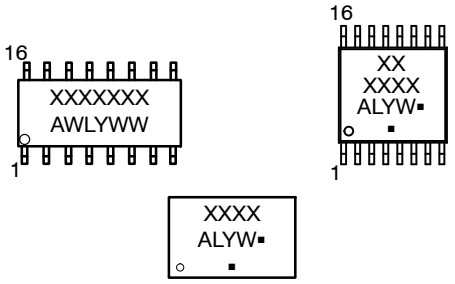
This device is an 8−bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the SERIAL SHIFT/$\overline{\text{PARALLEL LOAD}}$ input is low, the data is loaded asynchronously in parallel. When the SERIAL SHIFT/$\overline{\text{PARALLEL LOAD}}$ input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 2−input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAMS



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

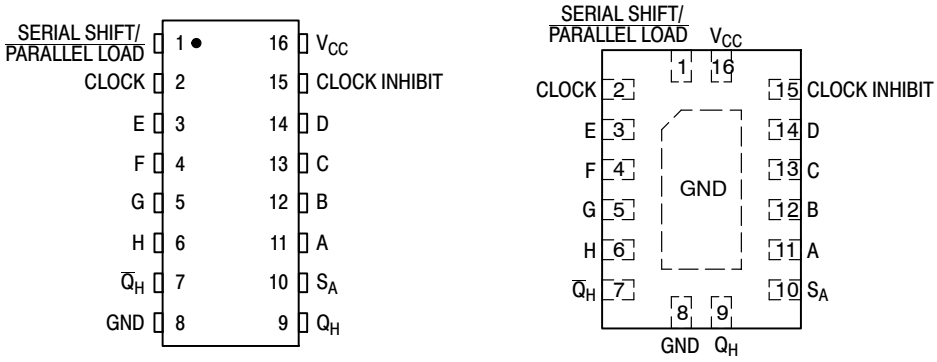


Figure 1. Pin Assignments

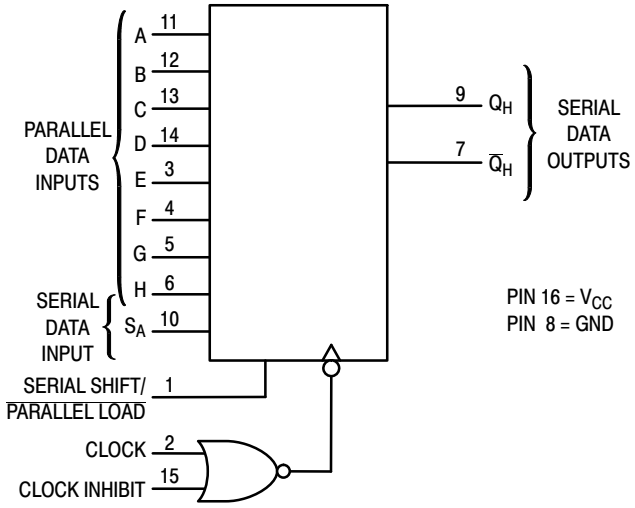


Figure 2. Logic Diagram

FUNCTION TABLE

Inputs					Internal Stages		Output	
Serial Shift/ Parallel Load	**Clock**	**Clock Inhibit**	**S_A**	**A – H**	**Q_A**	**Q_B**	**Q_H**	**Operation**
L	X	X	X	a … h	a	b	h	Asynchronous Parallel Load
H H	↑ ↑	L L	L H	X X	L H	Q_{An} Q_{An}	Q_{Gn} Q_{Gn}	Serial Shift via Clock
H H	L L	↑ ↑	L H	X X	L H	Q_{An} Q_{An}	Q_{Gn} Q_{Gn}	Serial Shift via Clock Inhibit
H H	X H	H X	X X	X X	No Change			Inhibited Clock
H	L	L	X	X	No Change			No Clock

X = don't care Q_{An} – Q_{Gn} = Data shifted from the preceding stage

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage		–0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC–16 QFN16 TSSOP–16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC–16 QFN16 TSSOP–16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm–by–114 mm, 2–ounce copper trace no air flow per JESD51–7.
2. HBM tested to EIA / JESD22–A114–A. CDM tested to JESD22–C101–A. JEDEC recommends that ESD qualification to EIA/JESD22–A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns
MC74HCT					
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time		0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74HC165A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	V
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HC165A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 4)	2.0 3.0 4.5 6.0	6 18 30 35	4.8 17 24 28	4 15 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q_H or $\overline{Q}_H$ (Figures 3 and 4)	2.0 3.0 4.5 6.0	150 52 30 26	190 63 38 33	225 65 45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/$\overline{\text{Parallel Load}}$ to Q_H or $\overline{Q}_H$ (Figures 3 and 5)	2.0 3.0 4.5 6.0	175 58 35 30	220 70 44 37	265 72 53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input H to Q_H or $\overline{Q}_H$ (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 52 30 26	190 63 38 33	225 65 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	40	pF

*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HC165A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 7)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{su}	Minimum Setup Time, Input S_A to Clock (or Clock Inhibit) (Figure 8)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Clock (or Clock Inhibit) (Figure 9)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{su}	Minimum Setup Time, Clock to Clock Inhibit (Figure 10)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_h	Minimum Hold Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Parallel Data Inputs (Figure 7)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Input S_A (Figure 8)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 9)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_{rec}	Minimum Recovery Time, Clock to Clock Inhibit (Figure 10)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_w	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 4)	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
t_w	Minimum Pulse width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 5)	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 4)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

DC ELECTRICAL CHARACTERISTICS (MC74HCT165A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA		≥−55°C	25°C to 125°C	
			5.5	2.9	2.4	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HCT165A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 4)	4.5 5.5	30 35	24 28	20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q_H or $\overline{Q}_H$ (Figures 3 and 4)	4.5 5.5	30 26	38 33	45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/$\overline{\text{Parallel Load}}$ to Q_H or $\overline{Q}_H$ (Figures 3 and 5)	4.5 5.5	35 30	44 37	53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input H to Q_H or $\overline{Q}_H$ (Figures 3 and 6)	4.5 5.5	30 26	38 33	45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	4.5 5.5	15 13	19 16	22 19	ns
C_{in}	Maximum Input Capacitance	−	10	10	10	pF

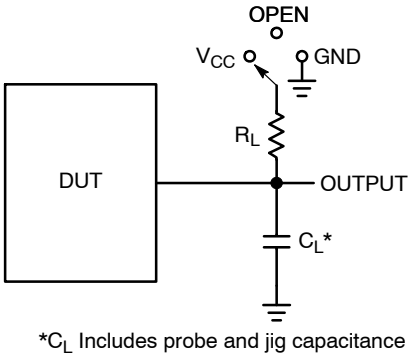
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	40	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HCT165A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 7)	4.5 5.5	15 13	19 16	22 19	ns
t_{su}	Minimum Setup Time, Input S_A to Clock (or Clock Inhibit) (Figure 8)	4.5 5.5	15 13	19 16	22 19	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Clock (or Clock Inhibit) (Figure 9)	4.5 5.5	15 13	19 16	22 19	ns
t_{su}	Minimum Setup Time, Clock to Clock Inhibit (Figure 10)	4.5 5.5	15 13	19 16	22 19	ns
t_h	Minimum Hold Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Parallel Data Inputs (Figure 7)	4.5 5.5	5 5	5 5	5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Input S_A (Figure 8)	4.5 5.5	5 5	5 5	5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 9)	4.5 5.5	5 5	5 5	5 5	ns
t_{rec}	Minimum Recovery Time, Clock to Clock Inhibit (Figure 10)	4.5 5.5	15 13	19 16	22 19	ns
t_w	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 4)	4.5 5.5	15 13	19 16	22 19	ns
t_w	Minimum Pulse width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 5)	4.5 5.5	15 13	19 16	22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 4)	4.5 5.5	500 400	500 400	500 400	ns

SWITCHING WAVEFORMS



*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 3. Test Circuit

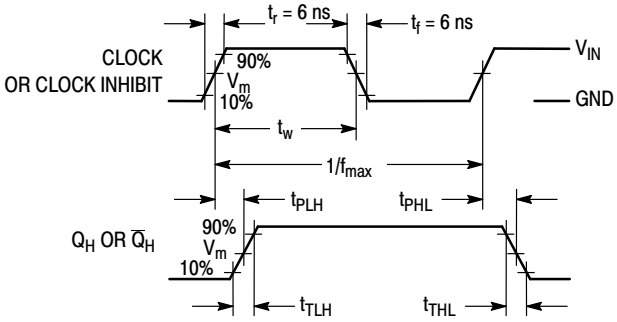


Figure 4. Serial−Shift Mode

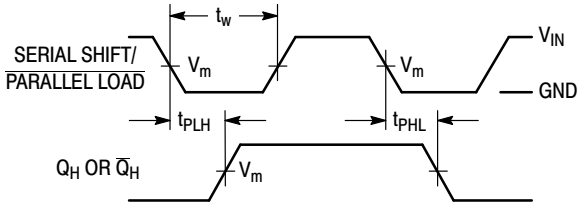


Figure 5. Parallel−Load Mode

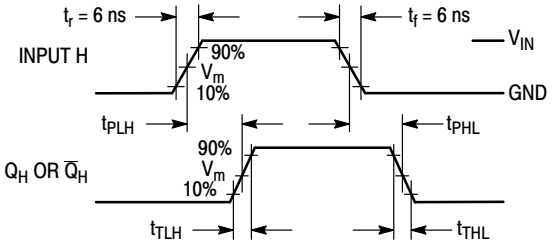


Figure 6. Parallel−Load Mode

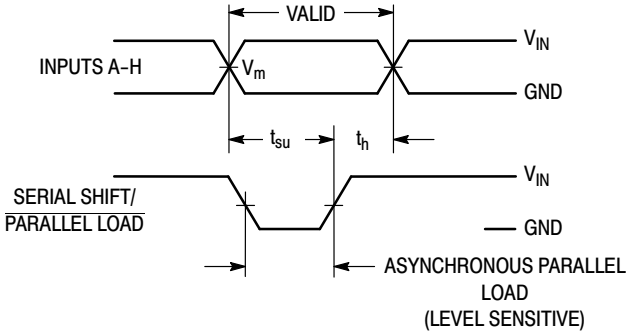


Figure 7. Parallel−Load Mode

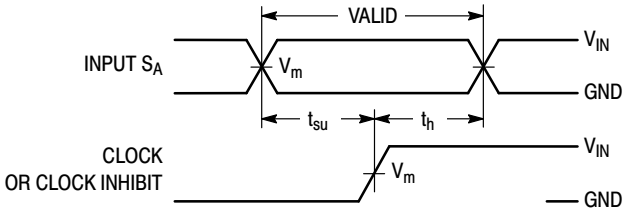


Figure 8. Serial−Shift Mode

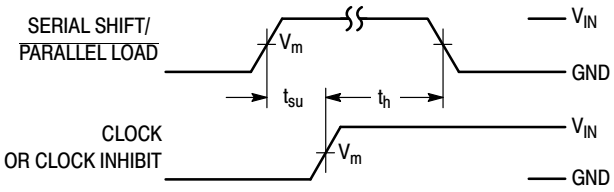


Figure 9. Serial−Shift Mode

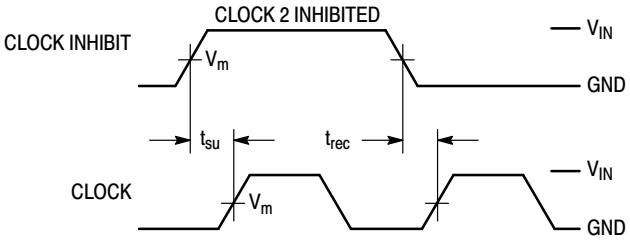


Figure 10. Serial−Shift, Clock−Inhibit Mode

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H (Pins 11, 12, 13, 14, 3, 4, 5, 6)

Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip−flops when the Serial Shift/$\overline{\text{Parallel Load}}$ input is low.

SA (Pin 10)

Serial Data input. When the Serial Shift/$\overline{\text{Parallel Load}}$ input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

CONTROL INPUTS

Serial Shift/$\overline{\text{Parallel Load}}$ (Pin 1)

Data−entry control input. When a high level is applied to this pin, data at the Serial Data input (S_A) are shifted into the register with the rising edge of the Clock. When a low level is applied to this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

Clock, Clock Inhibit (Pins 2, 15)

Clock inputs. These two clock inputs function identically. Either may be used as an active−high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

Q_H, $\overline{Q}_H$ (Pins 9, 7)

Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

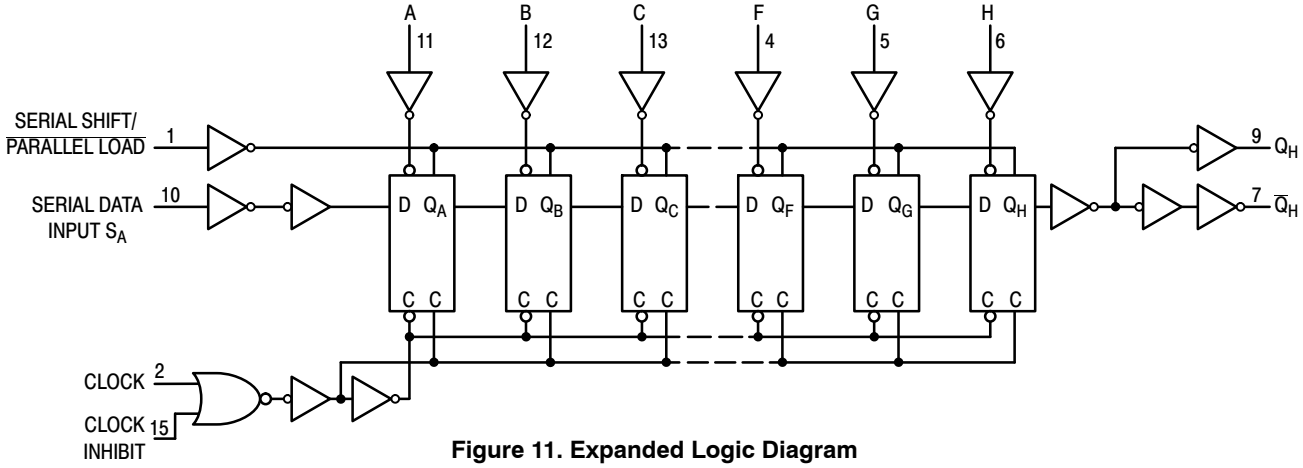


Figure 11. Expanded Logic Diagram

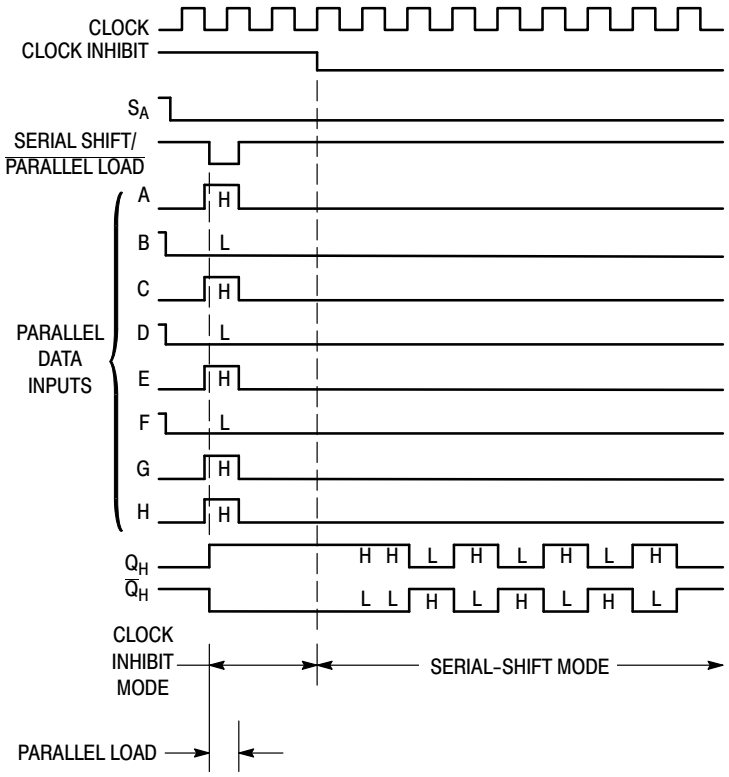


Figure 12. Timing Diagram

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC165ADG	HC165AG	SOIC−16	48 Units / Rail
MC74HC165ADR2G	HC165AG	SOIC−16	2500 / Tape & Reel
MC74HC165ADR2G−Q*	HC165AG	SOIC−16	2500 / Tape & Reel
MC74HC165ADTR2G	HC 165A	TSSOP−16	2500 / Tape & Reel
MC74HC165ADTR2G−Q*	HC 165A	TSSOP−16	2500 / Tape & Reel
MC74HC165AMNTWG	165A	QFN16	3000 / Tape & Reel
MC74HC165AMN2TWG	165A	QFN16	3000 / Tape & Reel
MC74HC165AMN2TWG−Q*	165A	QFN16	3000 / Tape & Reel

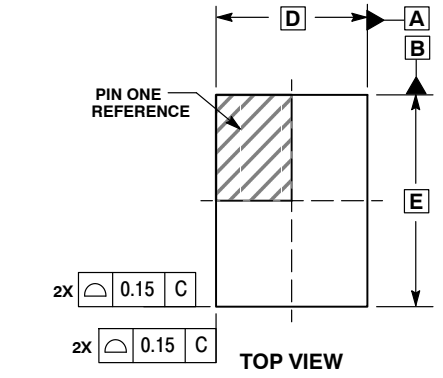
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

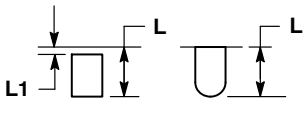
QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

DATE 11 DEC 2008

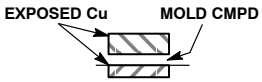
SCALE 2:1



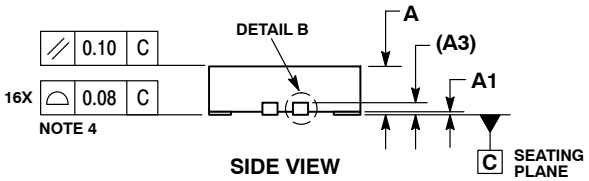
TOP VIEW



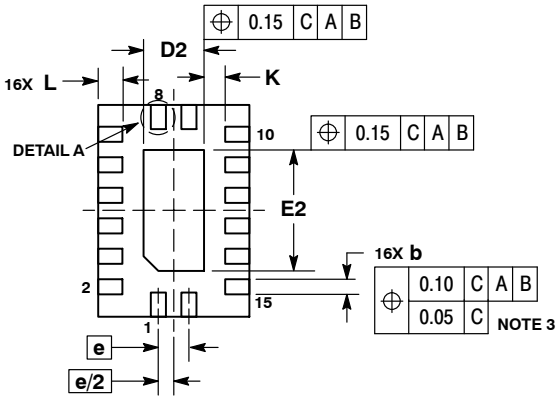
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

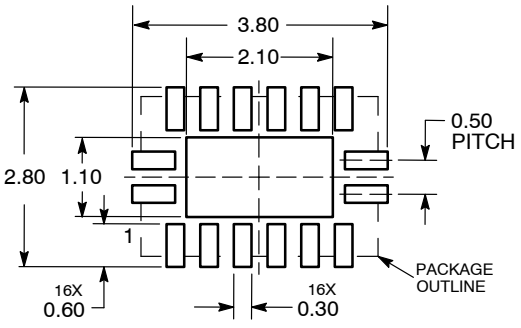
GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

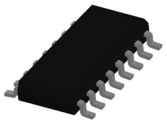
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

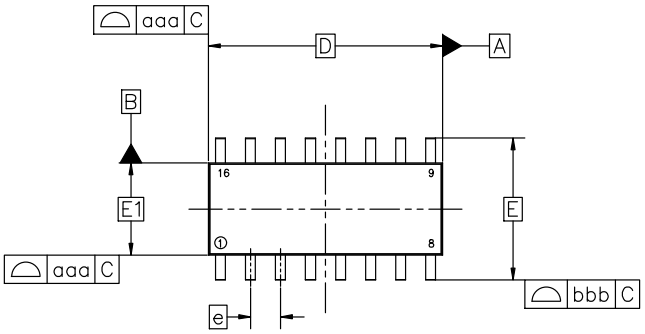
DOCUMENT NUMBER:	**98AON36347E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN16, 2.5X3.5, 0.5P**	**PAGE 1 OF 1**



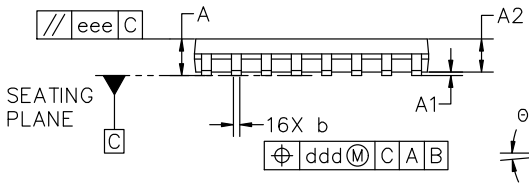
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

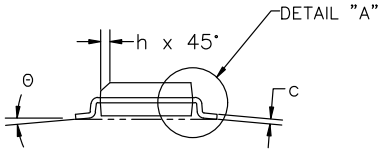
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



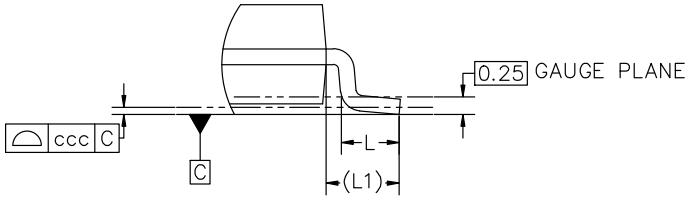
TOP VIEW



SIDE VIEW

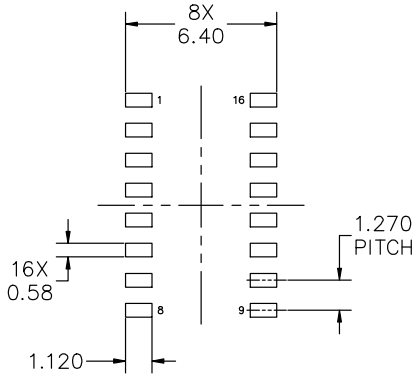


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

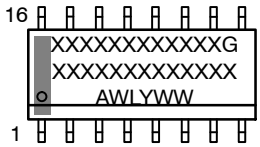
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

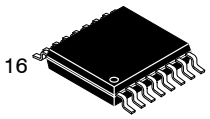
PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

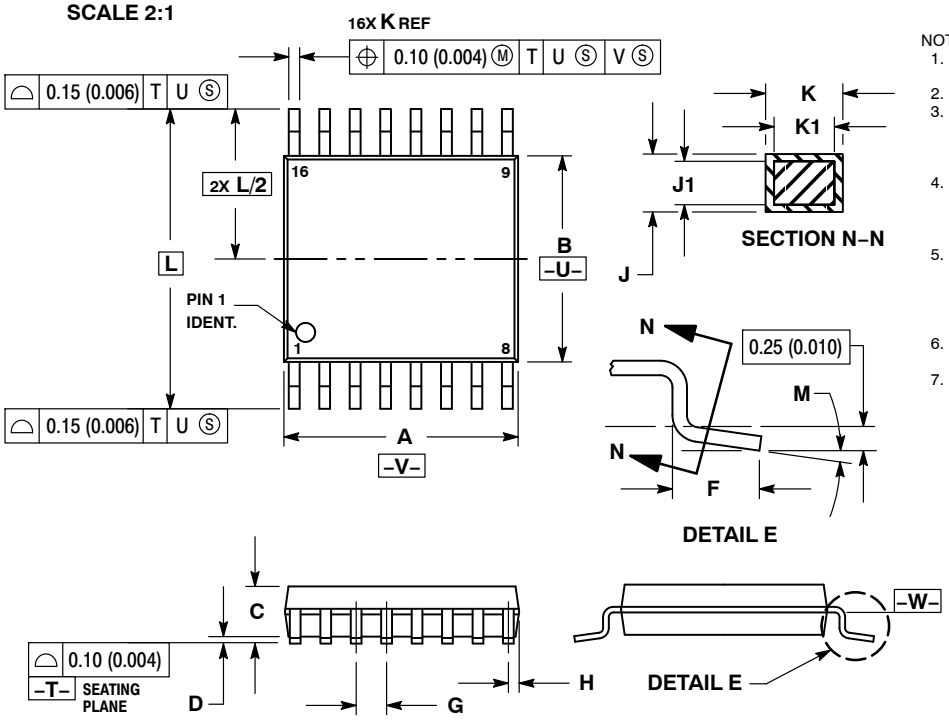
PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

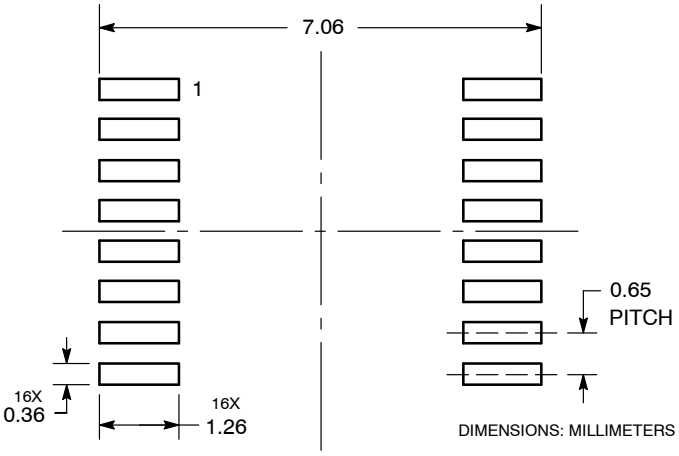
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



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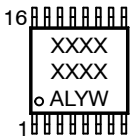
GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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