DATA SHEET
www.onsemi.com

Quad 2-Input AND Gate

High−Performance Silicon−Gate CMOS

MC74AC08, MC74ACT08

Features

- Outputs Source/Sink 24 mA
- ′ACT08 Has TTL Compatible Inputs
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

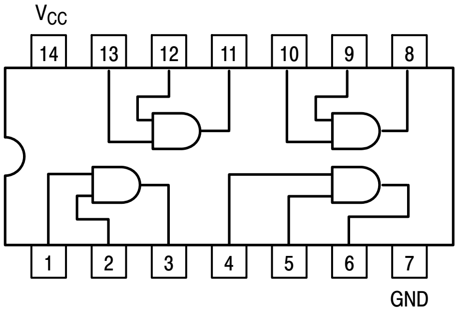
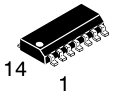
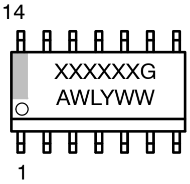


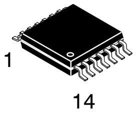
Figure 1. Pinout: 14−Lead Packages Conductors
(Top View)

MARKING DIAGRAMS

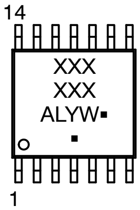


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



XXX = Specific Device Code
A = Assembly Location
WL or L = Wafer Lot
Y = Year
WW or W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

February, 2025 − Rev. 13

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+6.5$	V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
V_O	DC Output Voltage (Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 50	mA
I_O	DC Output Sink/Source Current	± 50	mA
I_{CC}	DC Supply Current per Output Pin	± 50	mA
I_{GND}	DC Ground Current per Output Pin	± 50	mA
T_{STG}	Storage Temperature Range	-65 to $+150$	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction temperature under Bias	$+150$	°C
θ_{JA}	Thermal Resistance (Note 2) SOIC TSSOP	116 150	°C/W
P_D	Power Dissipation in Still Air at 25°C SOIC TSSOP	1077 833	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Charged Device Model (Note 4)	> 2000 > 1000	V
$I_{Latch-Up}$	Latch−Up Performance Above V_{CC} and Below GND at 85°C (Note 5)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51−7.
3. Tested to EIA/JESD22−A114−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current – High		–	–	−24	mA
I_{OL}	Output Current – Low		–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	74AC		74AC	Unit
				T_A = +25°C		T_A = –40°C to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V	3.0	1.5	2.1	2.1	V
			4.5	2.25	3.15	3.15	
			5.5	2.75	3.85	3.85	
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V	3.0	1.5	0.9	0.9	V
			4.5	2.25	1.35	1.35	
			5.5	2.75	1.65	1.65	
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = –50 µA	3.0	2.99	2.9	2.9	V
			4.5	4.49	4.4	4.4	
			5.5	5.49	5.4	5.4	
		V_{IN} = V_{IL} or V_{IH} (Note 3)					V
		I_{OH} –12 mA	3.0	–	2.56	2.46	
		–24 mA	4.5	–	3.86	3.76	
		–24 mA	5.5	–	4.86	4.76	
V_{OL}	Minimum Low Level Output Voltage	I_{OUT} = 50 µA	3.0	0.002	0.1	0.1	V
			4.5	0.001	0.1	0.1	
			5.5	0.001	0.1	0.1	
		V_{IN} = V_{IL} or V_{IH}(Note 3)					V
		I_{OL} 12 mA	3.0	–	0.36	0.44	
		24 mA	4.5	–	0.36	0.44	
		24 mA	5.5	–	0.36	0.44	
I_{IN}	Maximum Input Leakage Current	V_I = V_{CC}, GND	5.5	–	±0.1	±1.0	µA
I_{OLD}	Minimum Dynamic (Note 4) Output Current	V_{OLD} = 1.65 V Max	5.5	–	–	75	mA
I_{OHD}		V_{OHD} = 3.85 V Min	5.5	–	–	–75	mA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	–	4.0	40	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

3. All outputs loaded; thresholds on input associated with output under test.
4. Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V) (Note5)	74AC			74AC		Unit
			T_A = +25°C C_L = 50 pF			T_A = –40°C to +85°C C_L = 50 pF		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.5	1.0	10.0	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
		5.0	1.5	5.5	7.0	1.0	7.5	

5. Voltage Range 3.3 V is 3.3 V ±0.3 V.
   Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	74ACT		74ACT	Unit
				T_A = +25°C		T_A = −40°C to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1 V	4.5	1.5	2.0	2.0	V
		or V_{CC} − 0.1 V	5.5	1.5	2.0	2.0	
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1 V	4.5	1.5	0.8	0.8	V
		or V_{CC} − 0.1 V	5.5	1.5	0.8	0.8	
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = −50 µA	4.5	4.49	4.4	4.4	V
			5.5	5.49	5.4	5.4	
		V_{IN} = V_{IL} or V_{IH} (Note 6)					V
		−24 mA	4.5	–	3.86	3.76	
		−24 mA	5.5	–	4.86	4.76	
V_{OL}	Maximum Low Level Output Voltage	I_{OUT} = 50 µA	4.5	0.001	0.1	0.1	V
			5.5	0.001	0.1	0.1	
		V_{IN} = V_{IL} or V_{IH} (Note 6)					V
		24 mA	4.5	–	0.36	0.44	
		24 mA	5.5	–	0.36	0.44	
I_{IN}	Maximum Input Leakage Current	V_I = V_{CC}, GND	5.5	–	±0.1	±1.0	µA
ΔI_{CCT}	Additional Max. I_{CC}/Input	V_I = V_{CC} − 2.1 V	5.5	0.6	–	1.5	mA
I_{OLD}	Minimum Dynamic (Note 7) Output Current	V_{OLD} = 1.65 V Max	5.5	–	–	75	mA
I_{OHD}		V_{OHD} = 3.85 V Min	5.5	–	–	−75	mA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	–	4.0	40	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. All outputs loaded; thresholds on input associated with output under test.
7. Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V) (Note 8)	74ACT			74ACT		Unit
			T_A = +25°C C_L = 50 pF			T_A = −40°C to +85°C C_L = 50 pF		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.0	–	9.0	1.0	10.0	ns
t_{PHL}	Propagation Delay	5.0	1.0	–	9.0	1.0	10.0	ns

8. Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Test Conditions	Value Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.0 V	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0 V	20	pF

ORDERING INFORMATION

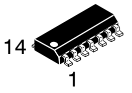
Device	Marking	Package	Shipping†
MC74AC08DG	AC08	SOIC−14 (Pb−Free)	55 Units / Rail
MC74AC08DR2G	AC08	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74AC08DR2G−Q*	AC08	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74AC08DTR2G	AC 08	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
MC74ACT08DG	ACT08	SOIC−14 (Pb−Free)	55 Units / Rail
MC74ACT08DR2G	ACT08	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74ACT08DTR2G	ACT 08	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

SOIC−14 NB

CASE 751A−03
ISSUE L



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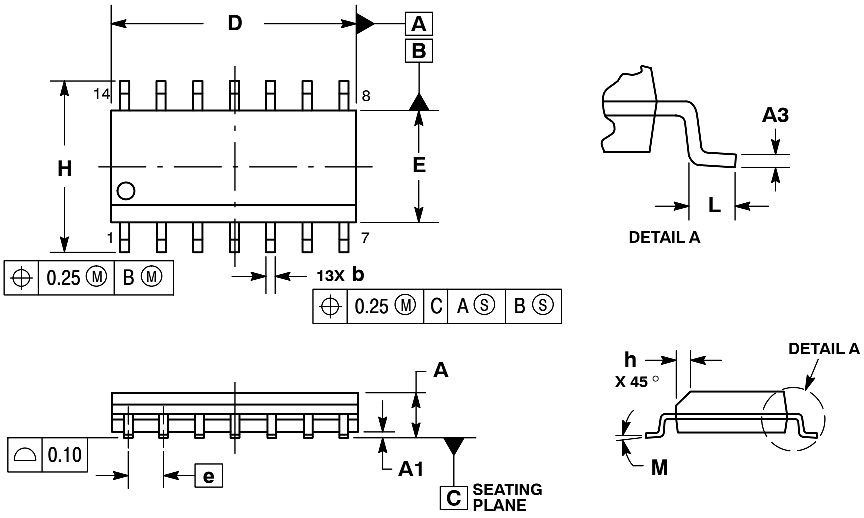
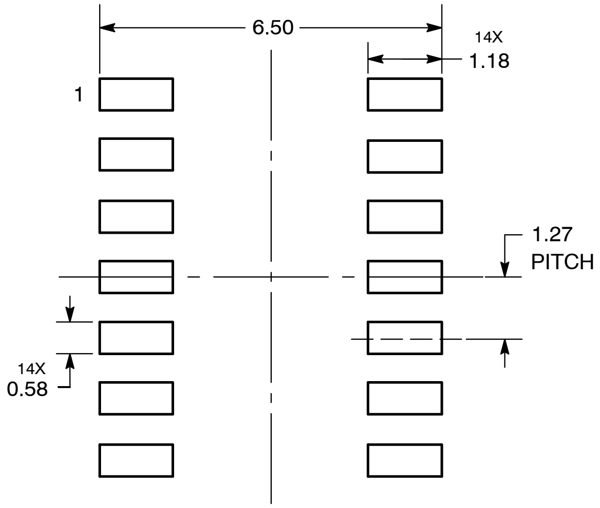
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

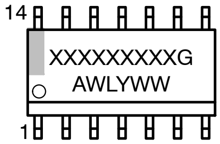
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**	**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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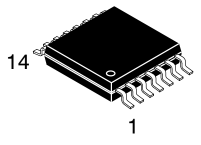
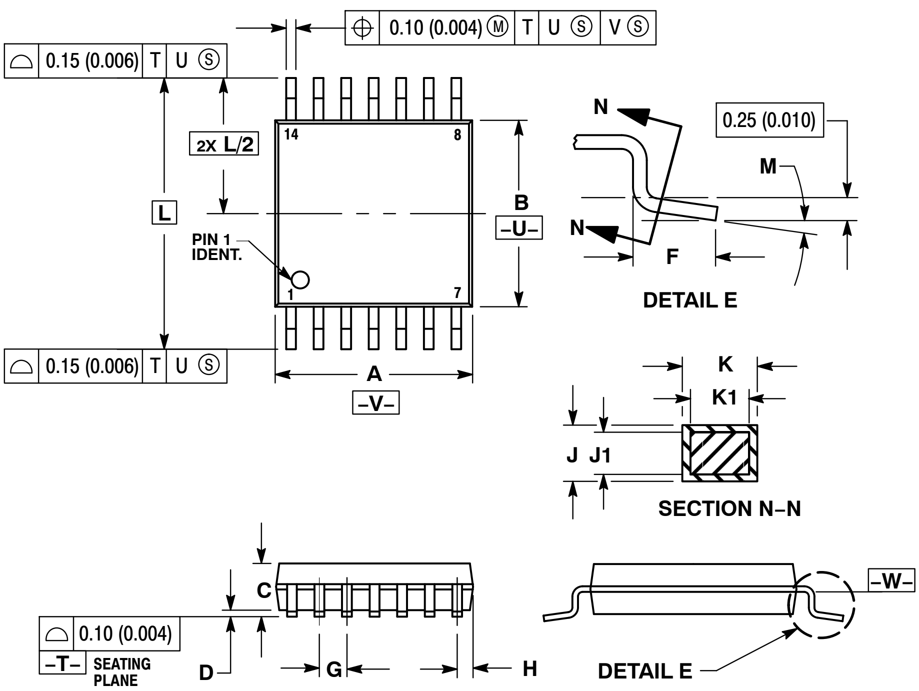
DESCRIPTION:	**SOIC−14 NB**	**PAGE 2 OF 2**



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

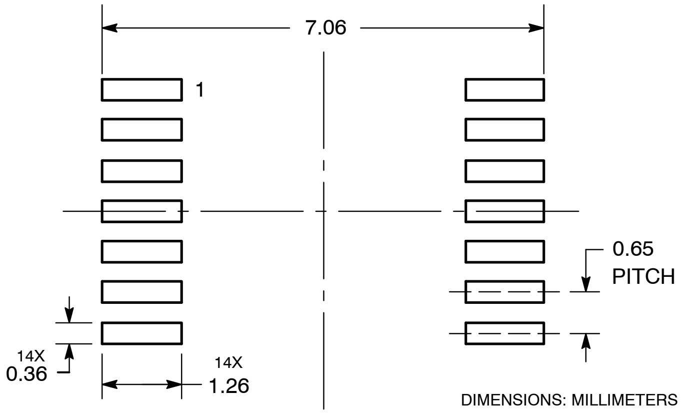
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

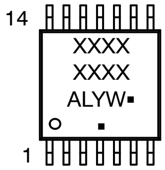
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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