MC100EP140

Phase-Frequency Detector,
3.3 V, ECL

Description
The MC100EP140 is a three state phase frequency-detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. Since the part is designed with fully differential internal gates, the noise is reduced throughout the circuit, especially at high speeds. The basic operation of a Phase/Frequency Detector (PFD) is to “compare” an incoming signal (feedback) to a set reference signal. When the Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which, when subtracted and integrated, provide an error voltage for control of a VCO. Detector states of operation are shown in the Figure 2 and the State Table.

The typical output amplitude of the EP140 is 400 mV, allowing faster switching time and greater bandwidth. For proper operation, the input edge rate of the R and FB inputs should be less than 5 ns.

More information on Phase Lock Loop operation and application can be found in AND8040.

The pinout is shown in Figure 1, the logic diagram in Figure 3, and the typical termination in Figure 5.

Features
• 500 ps Typical Propagation Delay
• Maximum Frequency > 2.1 GHz Typical
• Fully Differential Internally
• Advanced High Band Output Swing of 400 mV
• Transfer Gain: 1.0 mV/Degree at 1.4 GHz
  1.2 mV/Degree at 1.0 GHz
• Rise and Fall Time: 100 ps Typical
• The 100 Series Contains Temperature Compensation
• PECL Mode Operating Range: \( V_{CC} = 3.0 \text{ V to } 3.6 \text{ V} \)
  \( V_{EE} = 0 \text{ V} \)
• NECL Mode Operating Range: \( V_{CC} = 0 \text{ V} \)
  \( V_{EE} = -3.0 \text{ V to } -3.6 \text{ V} \)
• Open Input Default State
• Pb-Free Packages are Available

MARKING DIAGRAMS*

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.
**Table 1. PIN DESCRIPTION**

<table>
<thead>
<tr>
<th>PIN</th>
<th>FUNCTION</th>
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<tbody>
<tr>
<td>D, D</td>
<td>Differential Down Outputs</td>
</tr>
<tr>
<td>U, U</td>
<td>Differential Up Outputs</td>
</tr>
<tr>
<td>R*</td>
<td>ECL Reference Input</td>
</tr>
<tr>
<td>FB*</td>
<td>ECL Feedback Input</td>
</tr>
<tr>
<td>VCC</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>VEE</td>
<td>Negative Supply</td>
</tr>
</tbody>
</table>

* Pins will default LOW when left open.

**Table 2. STATE TABLE**

<table>
<thead>
<tr>
<th>PHASE DETECTOR STATE</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUMP DOWN 2–1–2</td>
<td>R</td>
<td>FB</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>2–1</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>1–2</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>L</td>
</tr>
<tr>
<td>PUMP UP 2–3–2</td>
<td>R</td>
<td>FB</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>2–3</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>3–2</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>L</td>
</tr>
</tbody>
</table>

**Figure 1. 8–Lead Pinout (Top View)**

**Figure 2. Phase Detector Logic Model**

**Figure 3. Logic Diagram**
Table 3. ATTRIBUTES

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Value</th>
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<tbody>
<tr>
<td>Internal Input Pulldown Resistor</td>
<td>75 kΩ</td>
</tr>
<tr>
<td>Internal Input Pullup Resistor</td>
<td>37.5 kΩ</td>
</tr>
<tr>
<td>ESD Protection</td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td>&gt; 200 V</td>
</tr>
<tr>
<td>Charged Device Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)</td>
<td>Pb Pkg Pb–Free Pkg</td>
</tr>
<tr>
<td>Flammability Rating</td>
<td></td>
</tr>
<tr>
<td>Oxygen Index: 28 to 34</td>
<td>UL 94 V–0 @ 0.125 in</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>457 Devices</td>
</tr>
</tbody>
</table>

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition 1</th>
<th>Condition 2</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>PECL Mode Power Supply</td>
<td>VEE = 0 V</td>
<td></td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>VEE</td>
<td>NECL Mode Power Supply</td>
<td>VCC = 0 V</td>
<td></td>
<td>−6</td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>PECL Mode Input Voltage</td>
<td>VEE = 0 V</td>
<td>VCC = 0 V</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>NECL Mode Input Voltage</td>
<td></td>
<td>VI ≤ VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VI ≥ VEE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iout</td>
<td>Output Current</td>
<td>Continuous Surge</td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td></td>
<td>−40 to +85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature Range</td>
<td></td>
<td>−65 to +150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction–to–Ambient)</td>
<td>0 lrpm</td>
<td>SOIC–8</td>
<td>190</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lrpm</td>
<td>SOIC–8</td>
<td>130</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction–to–Case)</td>
<td>Standard Board</td>
<td>SOIC–8</td>
<td>41 to 44</td>
<td>°C/W</td>
</tr>
<tr>
<td>Tsol</td>
<td>Wave Solder</td>
<td>Pb</td>
<td></td>
<td>265</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pb–Free</td>
<td></td>
<td>265</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3$ V, $V_{EE} = 0$ V (Note 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>–40°C</th>
<th>25°C</th>
<th>85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>IEE</td>
<td>Power Supply Current</td>
<td>45</td>
<td>65</td>
<td>85</td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage (Note 3)</td>
<td>2155</td>
<td>2280</td>
<td>2405</td>
</tr>
<tr>
<td>VCL</td>
<td>Output LOW Voltage (Note 3)</td>
<td>1755</td>
<td>1880</td>
<td>2005</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage (Single–Ended)</td>
<td>2075</td>
<td>2420</td>
<td>2075</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage (Single–Ended)</td>
<td>1355</td>
<td>1675</td>
<td>1355</td>
</tr>
<tr>
<td>IH</td>
<td>Input HIGH Current</td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>IL</td>
<td>Input LOW Current</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lrpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with $V_{CC}$, $V_{EE}$ can vary $+0.3$ V to $−0.3$ V.
3. All loading with 50 Ω to $V_{CC} = 2.0$ V.
### Table 6. 100EP DC CHARACTERISTICS, NECL VCC = 0 V, VEE = −3.6 V to −3.0 V (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>−40°C</th>
<th>25°C</th>
<th>85°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>IEE</td>
<td>Power Supply Current</td>
<td>45</td>
<td>65</td>
<td>85</td>
<td>50</td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage (Note 5)</td>
<td>−1145</td>
<td>−1020</td>
<td>−895</td>
<td>−1145</td>
</tr>
<tr>
<td>VOL</td>
<td>Output LOW Voltage (Note 5)</td>
<td>−1545</td>
<td>−1420</td>
<td>−1295</td>
<td>−1545</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage (Single–Ended)</td>
<td>−1225</td>
<td>−880</td>
<td>−1225</td>
<td>−880</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage (Single–Ended)</td>
<td>−1945</td>
<td>−1625</td>
<td>−1945</td>
<td>−1625</td>
</tr>
<tr>
<td>IH</td>
<td>Input HIGH Current</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>IL</td>
<td>Input LOW Current</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with VCC.
5. All loading with 50 Ω to VCC − 2.0 V.

### Table 7. AC CHARACTERISTICS VCC = 0 V; VEE = −3.6 V to −3.0 V or VCC = 3.0 V to 3.6 V; VEE = 0 V (Note 6)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>−40°C</th>
<th>25°C</th>
<th>85°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>fmax</td>
<td>Maximum Frequency (Figure 4)</td>
<td>&gt; 2</td>
<td>&gt; 2</td>
<td>&gt; 2</td>
<td>&gt; 2</td>
</tr>
<tr>
<td>tPLH, tPHL</td>
<td>Propagation Delay to R to U, FB to D</td>
<td>300</td>
<td>400</td>
<td>6002</td>
<td>325</td>
</tr>
<tr>
<td>tJITTER</td>
<td>Cycle–to–Cycle Jitter (Figure 4)</td>
<td>.2</td>
<td>&lt; 1</td>
<td>.2</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>VPP</td>
<td>Input Voltage Swing</td>
<td>400</td>
<td>800</td>
<td>1200</td>
<td>400</td>
</tr>
<tr>
<td>tr, tf</td>
<td>Output Rise/Fall Times (20% − 80%)</td>
<td>Q, Q</td>
<td>50</td>
<td>90</td>
<td>180</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Measured using a 750 mV VPP pk–pk, 50% duty cycle, clock source. All loading with 50 Ω to VCC − 2.0 V.

![Figure 4. fmax/Jitter](http://onsemi.com)
Figure 5. Typical Termination for Output Driver and Device Evaluation
(See Application Note AN8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping¹</th>
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<tbody>
<tr>
<td>MC100EP140D</td>
<td>SOIC-8</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC100EP140DG</td>
<td>SOIC-8 (Pb-Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC100EP140DR2</td>
<td>SOIC-8</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC100EP140DR2G</td>
<td>SOIC-8 (Pb-Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

¹For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BR8011/D.

Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLInPS™ I/O SPICE Modeling Kit
- AN1504/D – Metastability and the ECLInPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1672/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLInPS
- AND8090/D – AC Characteristics of ECL Devices

ECLInPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).
SOIC–8 NB
CASE 751–07
ISSUE AK

DATE 16 FEB 2011

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>DIMMERS</th>
<th>INCHES</th>
<th>MILLIMETERS</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>4.80</td>
<td>0.480</td>
</tr>
<tr>
<td>B</td>
<td>3.60</td>
<td>0.360</td>
</tr>
<tr>
<td>C</td>
<td>1.35</td>
<td>0.135</td>
</tr>
<tr>
<td>D</td>
<td>0.53</td>
<td>0.053</td>
</tr>
<tr>
<td>G</td>
<td>1.27</td>
<td>0.127</td>
</tr>
<tr>
<td>H</td>
<td>0.10</td>
<td>0.010</td>
</tr>
<tr>
<td>J</td>
<td>0.19</td>
<td>0.019</td>
</tr>
<tr>
<td>K</td>
<td>0.40</td>
<td>0.040</td>
</tr>
<tr>
<td>M</td>
<td>0.25</td>
<td>0.025</td>
</tr>
<tr>
<td>N</td>
<td>0.25</td>
<td>0.025</td>
</tr>
<tr>
<td>Z</td>
<td>0.25</td>
<td>0.025</td>
</tr>
<tr>
<td>S</td>
<td>5.80</td>
<td>0.580</td>
</tr>
</tbody>
</table>

*Soldering Footprint*

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "\," may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**
### Style 1:
- **PIN 1.** Emitter
- **PIN 2.** Collector
- **PIN 3.** Collector
- **PIN 4.** Emitter
- **PIN 5.** Emitter
- **PIN 6.** Base
- **PIN 7.** Base
- **PIN 8.** Emitter

### Style 2:
- **PIN 1.** Collector, die #1
- **PIN 2.** Collector
- **PIN 3.** Collector
- **PIN 4.** Collector, die #2
- **PIN 5.** Emitter, die #1
- **PIN 6.** Emitter
- **PIN 7.** Base, die #1
- **PIN 8.** Emitter

### Style 3:
- **PIN 1.** Drain, die #1
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Drain
- **PIN 5.** Source
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

### Style 4:
- **PIN 1.** Anode
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Drain
- **PIN 5.** Source
- **PIN 6.** Source
- **PIN 7.** Source
- **PIN 8.** Common cathode

### Style 5:
- **PIN 1.** Drain
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Drain
- **PIN 5.** Source
- **PIN 6.** Gate
- **PIN 7.** Gate
- **PIN 8.** Source

### Style 6:
- **PIN 1.** Source
- **PIN 2.** External bypass
- **PIN 3.** Third stage source
- **PIN 4.** Ground
- **PIN 5.** Drain
- **PIN 6.** Emitter
- **PIN 7.** Drain
- **PIN 8.** Second stage Vd

### Style 7:
- **PIN 1.** Input
- **PIN 1.** Collector, die #1
- **PIN 2.** Base, die #1
- **PIN 3.** Collector, die #2
- **PIN 4.** Collector, die #2
- **PIN 5.** Collector, die #2
- **PIN 6.** Collector, die #2
- **PIN 7.** Collector, die #2
- **PIN 8.** Collector, die #2

### Style 8:
- **PIN 1.** Collector, die #1
- **PIN 2.** Collector, die #1
- **PIN 3.** Collector, die #1
- **PIN 4.** Collector, die #2
- **PIN 5.** Collector, die #2
- **PIN 6.** Collector, die #2
- **PIN 7.** Collector, die #2
- **PIN 8.** Collector, die #2

### Style 9:
- **PIN 1.** Emitter, common
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #2
- **PIN 1.** Collector, die #2
- **PIN 1.** Collector, die #2
- **PIN 1.** Collector, die #2
- **PIN 1.** Collector, die #2
- **PIN 1.** Collector, die #2

### Style 10:
- **PIN 1.** Ground
- **PIN 1.** Source
- **PIN 1.** Source 1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1

### Style 11:
- **PIN 1.** Source 1
- **PIN 1.** Source 1
- **PIN 1.** Source 1
- **PIN 1.** Source 1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1

### Style 12:
- **PIN 1.** Source
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1
- **PIN 1.** Collector, die #1

### Style 13:
- **PIN 1.** N.C.
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source

### Style 14:
- **PIN 1.** N-source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source

### Style 15:
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1

### Style 16:
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1
- **PIN 1.** Anode 1

### Style 17:
- **PIN 1.** Vcc
- **PIN 2.** V2out
- **PIN 3.** Vout
- **PIN 4.** Txe
- **PIN 5.** Rxe
- **PIN 6.** Vee
- **PIN 7.** Gnd
- **PIN 8.** Acc

### Style 18:
- **PIN 1.** Anode
- **PIN 1.** Anode
- **PIN 1.** Anode
- **PIN 1.** Anode
- **PIN 1.** Gate
- **PIN 1.** Gate
- **PIN 1.** Gate
- **PIN 1.** Gate

### Style 19:
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source

### Style 20:
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Gate
- **PIN 1.** Gate
- **PIN 1.** Gate
- **PIN 1.** Gate

### Style 21:
- **PIN 1.** Cathode 1
- **PIN 2.** Cathode 2
- **PIN 3.** Cathode 3
- **PIN 4.** Cathode 4
- **PIN 5.** Cathode 5
- **PIN 6.** Common anode
- **PIN 7.** Common anode
- **PIN 8.** Cathode 6

### Style 22:
- **PIN 1.** I/O line 1
- **PIN 1.** I/O line 1
- **PIN 1.** Common cathode/vcc
- **PIN 1.** Common cathode/vcc
- **PIN 1.** Common cathode/vcc
- **PIN 1.** Common cathode/vcc
- **PIN 1.** Common cathode/vcc
- **PIN 1.** Common cathode/vcc

### Style 23:
- **PIN 1.** Line 1 in
- **PIN 1.** Line 1 in
- **PIN 1.** Common anode/gnd
- **PIN 1.** Common anode/gnd
- **PIN 1.** Common anode/gnd
- **PIN 1.** Common anode/gnd
- **PIN 1.** Common anode/gnd
- **PIN 1.** Common anode/gnd

### Style 24:
- **PIN 1.** Base
- **PIN 1.** Emitter
- **PIN 1.** Collector/Anode
- **PIN 1.** Collector/Anode
- **PIN 1.** Collector/Anode
- **PIN 1.** Collector/Anode
- **PIN 1.** Collector/Anode
- **PIN 1.** Collector/Anode

### Style 25:
- **PIN 1.** Vin
- **PIN 2.** N/C
- **PIN 3.** Next
- **PIN 4.** Gnd
- **PIN 5.** IoUT
- **PIN 6.** IoUT
- **PIN 7.** IoUT
- **PIN 8.** IoUT

### Style 26:
- **PIN 1.** Gnd
- **PIN 1.** Ilimit
- **PIN 1.** Sw_to_gnd
- **PIN 1.** Sw_to_gnd
- **PIN 1.** Sw_to_gnd
- **PIN 1.** Sw_to_gnd
- **PIN 1.** Sw_to_gnd
- **PIN 1.** Sw_to_gnd

### Style 27:
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain

### Style 28:
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off
- **PIN 1.** Dasic_off

### Style 29:
- **PIN 1.** Base, die #1
- **PIN 2.** Emitter, die #1
- **PIN 3.** Base, die #2
- **PIN 4.** Emitter, die #2
- **PIN 5.** Collector, die #2
- **PIN 6.** Collector, die #2
- **PIN 7.** Collector, die #1
- **PIN 8.** Collector, die #1

### Style 30:
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Drain
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
- **PIN 1.** Source
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