The MAX1720 is a CMOS charge pump voltage inverter that is designed for operation over an input voltage range of 1.15 V to 5.5 V with an output current capability in excess of 50 mA. The operating current consumption is only 67 μA, and a power saving shutdown input is provided to further reduce the current to a mere 0.4 μA. The device contains a 12 kHz oscillator that drives four low resistance MOSFET switches, yielding a low output resistance of 26 Ω and a voltage conversion efficiency of 99%. This device requires only two external 10 μF capacitors for a complete inverter making it an ideal solution for numerous battery powered and board level applications. The MAX1720 is available in the space saving TSOP–6 package.

Features
- Operating Voltage Range of 1.15 V to 5.5 V
- Output Current Capability in Excess of 50 mA
- Low Current Consumption of 67 μA
- Power Saving Shutdown Input for a Reduced Current of 0.4 μA
- Operation at 12 kHz
- Low Output Resistance of 26 Ω
- Space Saving TSOP–6 Package
- Pb–Free Package is Available

Typical Applications
- LCD Panel Bias
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments

This device contains 77 active transistors.  

Figure 1. Typical Application
### MAXIMUM RATINGS*

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range (Vin to GND)</td>
<td>Vin</td>
<td>−0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Range (Vout to GND)</td>
<td>Vout</td>
<td>−6.0 to 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Output Current (Note 1)</td>
<td>Iout</td>
<td>100 mA</td>
<td></td>
</tr>
<tr>
<td>Output Short Circuit Duration (Vout to GND, Note 1)</td>
<td>ISC</td>
<td>Indefinite</td>
<td>sec</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>TJ</td>
<td>150 °C</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation and Thermal Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction−to−Air</td>
<td>RJA</td>
<td>256 °C/W</td>
<td></td>
</tr>
<tr>
<td>Maximum Power Dissipation @ TA = 70 °C</td>
<td>PD</td>
<td>313 mW</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>−55 to 150 °C</td>
<td></td>
</tr>
</tbody>
</table>

*Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

**ESD Ratings**
- ESD Machine Model Protection up to 200 V, Class B
- ESD Human Body Model Protection up to 2000 V, Class 2

### ELECTRICAL CHARACTERISTICS (Vin = 5.0 V, C1 = 10 µF, C2 = 10 µF, TA = −40 °C to 85 °C, typical values shown are for TA = 25 °C unless otherwise noted. See Figure 14 for Test Setup.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage Range (SHDN = Vin, RL = 10 k)</td>
<td>Vin</td>
<td>1.5 to 5.5</td>
<td>1.15 to 6.0</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Supply Current Device Operating (SHDN = 5.0 V, RL = ∞)</td>
<td>Iin</td>
<td>–</td>
<td>67</td>
<td>90</td>
<td>µA</td>
</tr>
<tr>
<td>Supply Current Device Shutdown (SHDN = 0 V)</td>
<td>ISHDN</td>
<td>–</td>
<td>0.4</td>
<td>–</td>
<td>µA</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>fOSC</td>
<td>8.4</td>
<td>12</td>
<td>15.6</td>
<td>kHz</td>
</tr>
<tr>
<td>Output Resistance (Iout = 25 mA, Note 2)</td>
<td>Rout</td>
<td>–</td>
<td>26</td>
<td>50</td>
<td>Ω</td>
</tr>
<tr>
<td>Voltage Conversion Efficiency (RL = ∞)</td>
<td>VEFF</td>
<td>99</td>
<td>99.9</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Power Conversion Efficiency (RL = 1.0 k)</td>
<td>PEFF</td>
<td>–</td>
<td>96</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Shutdown Input Threshold Voltage (Vin = 1.5 V to 5.5 V)</td>
<td>V(R(SHDN))</td>
<td>–</td>
<td>0.6 Vin</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Input Bias Current</td>
<td>pA</td>
<td>–</td>
<td>5.0</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Wake−Up Time from Shutdown (RL = 1.0 k)</td>
<td>tWKUP</td>
<td>–</td>
<td>1.2</td>
<td>–</td>
<td>ms</td>
</tr>
</tbody>
</table>

1. Maximum Package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded. 
   \[ T_J = T_A + (PD \times RJA) \]
2. Capacitors C1 and C2 contribution is approximately 20% of the total output resistance.

http://onsemi.com
Vin, SUPPLY VOLTAGE (V)

1.5  3.0  2.5  2.0  3.5  4.0  4.5  5.0  5.5

Figure 2. Output Resistance vs. Supply Voltage

C1, C2, C3, CAPACITANCE (μF)

0  10  20  30  40  50

Figure 4. Output Current vs. Capacitance

Vin = 1.90 V
Vout = −1.50 V

Vin = 3.15 V
Vout = −2.50 V

Vin = 4.75 V
Vout = −4.00 V

Figure 5. Output Voltage Ripple vs. Capacitance

Vin = 1.5 V
Vout = −4.00 V

Vin = 2.0 V
Vout = −4.00 V

Vin = 3.3 V
Vout = −2.50 V

Vin = 5.0 V
Vout = −1.50 V

Figure 3. Output Resistance vs. Ambient Temperature

Rout, OUTPUT RESISTANCE (Ω)

0  50  100  150  200

Figure 6. Supply Current vs. Supply Voltage

3.0  3.5  4.0  4.5  5.0

Figure 7. Oscillator Frequency vs. Ambient Temperature

TA, AMBIENT TEMPERATURE (°C)

−50  25  10

Vin = 1.5 V
Vout = −4.00 V

Vin = 2.0 V
Vout = −4.00 V

Vin = 3.3 V
Vout = −2.50 V

Vin = 5.0 V
Vout = −1.50 V

Figure 14 Test Setup

I_{\text{in}}, SUPPLY CURRENT (mA)

0  5  10  15  20

Vin = 4.75 V
Vout = −4.00 V

Vin = 3.15 V
Vout = −2.50 V

Vin = 1.90 V
Vout = −1.50 V

Figure 14 Test Setup

R_L = ∞

TA = 25°C

TA = −40°C

TA = 85°C

Vin, SUPPLY VOLTAGE (V)

1.5  2.0  2.5  3.0  3.5  4.0  4.5  5.0

Figure 14 Test Setup

http://onsemi.com
Figure 8. Output Voltage vs. Output Current

Figure 9. Power Conversion Efficiency vs. Output Current

Figure 10. Output Voltage Ripple and Noise

Figure 11. Shutdown Supply Current vs. Ambient Temperature

Figure 12. Supply Voltage vs. Shutdown Input Voltage Threshold

Figure 13. Wakeup Time From Shutdown
**DETAILED OPERATING DESCRIPTION**

The MAX1720 charge pump converter inverts the voltage applied to the Vin pin. Conversion consists of a two-phase operation (Figure 15). During the first phase, switches S2 and S4 are open and S1 and S3 are closed. During this time, C1 charges to the voltage on Vin and load current is supplied from C2. During the second phase, S2 and S4 are closed, and S1 and S3 are open. This action connects C1 across C2, restoring charge to C2.

**APPLICATIONS INFORMATION**

**Output Voltage Considerations**

The MAX1720 performs voltage conversion but does not provide regulation. The output voltage will drop in a linear manner with respect to load current. The value of this equivalent output resistance is approximately 26 Ohm nominal at 25°C with Vin = 5.0 V. Vout is approximately −5.0 V at light loads, and drops according to the equation below:

\[ V_{DROP} = I_{OUT} \times R_{OUT} \]
\[ V_{OUT} = -(V_{IN} - V_{DROP}) \]

**Charge Pump Efficiency**

The overall power conversion efficiency of the charge pump is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. (which vary with input voltage, temperature and oscillator frequency).
2. I^2R losses due to the on–resistance of the MOSFET switches on–board the charge pump.
3. Charge pump capacitor losses due to Equivalent Series Resistance (ESR).
4. Losses that occur during charge transfer from the commutation capacitor to the output capacitor when a voltage difference between the two capacitors exists.

Most of the conversion losses are due to factors 2, 3 and 4. These losses are given by Equation 1.

\[ P_{LOSS(2,3,4)} = I_{OUT}^2 \times R_{OUT} \approx I_{OUT}^2 \times \left[ \frac{1}{(f_{OSC})C_1 + 8R_{SWITCH} + 4ESR_{C1} + ESR_{C2}} \right] \]

(eq. 1)

The 1/(f_{OSC})(C_1) term in Equation 1 is the effective output resistance of an ideal switched capacitor circuit (Figures 16 and 17).

The losses due to charge transfer above are also shown in Equation 2. The output voltage ripple is given by Equation 3.

\[ P_{LOSS} = [0.5C_1(V_{IN}^2 - V_{OUT}^2) + 0.5C_2(V_{RIPPLE}^2 - 2V_{OUT}V_{RIPPLE})] \times f_{OSC} \]

(eq. 2)

\[ V_{RIPPLE} = \frac{I_{OUT}}{(f_{OSC})C_2} + 2(I_{OUT})(ESR_{C2}) \]

(eq. 3)
Capacitor Selection

In order to maintain the lowest output resistance and output ripple voltage, it is recommended that low ESR capacitors be used. Additionally, larger values of C1 will lower the output resistance and larger values of C2 will reduce output voltage ripple. (See Equation 3).

Table 1 shows various values of C1, C2 and C3 with the corresponding output resistance values at 25°C. Table 2 shows the output voltage ripple for various values of C1, C2 and C3. The data in Tables 1 and 2 was measured not calculated.

<table>
<thead>
<tr>
<th>C1 = C2 = C3 (μF)</th>
<th>R_out (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>129.1</td>
</tr>
<tr>
<td>1.4</td>
<td>69.5</td>
</tr>
<tr>
<td>3.3</td>
<td>37.0</td>
</tr>
<tr>
<td>7.3</td>
<td>26.5</td>
</tr>
<tr>
<td>10</td>
<td>25.9</td>
</tr>
<tr>
<td>24</td>
<td>24.1</td>
</tr>
<tr>
<td>50</td>
<td>24</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C1 = C2 = C3 (μF)</th>
<th>Output Voltage Ripple (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>382</td>
</tr>
<tr>
<td>1.4</td>
<td>342</td>
</tr>
<tr>
<td>3.3</td>
<td>255</td>
</tr>
<tr>
<td>7.3</td>
<td>164</td>
</tr>
<tr>
<td>10</td>
<td>132</td>
</tr>
<tr>
<td>24</td>
<td>59</td>
</tr>
<tr>
<td>50</td>
<td>38</td>
</tr>
</tbody>
</table>

Voltage Inverter

The most common application for a charge pump is the voltage inverter (Figure 14). This application uses two or three external capacitors. The C1 (pump capacitor) and C2 (output capacitor) are required. The input bypass capacitor, C3, may be necessary depending on the application. The output is equal to −V_in plus any voltage drops due to loading. Refer to Tables 1 and 2 for capacitor selection. The test setup used for the majority of the characterization is shown in Figure 14.

Layout Considerations

As with any switching power supply circuit, good layout practice is recommended. Mount components as close together as possible to minimize stray inductance and capacitance. Also, use a large ground plane to minimize noise leakage into other circuitry.

Capacitor Resources

Selecting the proper type of capacitor can reduce switching loss. Low ESR capacitors are recommended. The MAX1720 was characterized using the capacitors listed in Table 3. This list identifies low ESR capacitors for the voltage inverter application.

Input Supply Bypassing

The input voltage, V_in, should be capacitively bypassed to reduce AC impedance and minimize noise effects due to the switching internals in the device. If the device is loaded from V_out to GND, it is recommended that a large value capacitor (at least equal to C1) be connected from V_in to GND. If the device is loaded from V_in to V_out, a small (0.7 μF) capacitor between the pins is sufficient.

Figure 18. Voltage Inverter
The MAX1720 primary function is a voltage inverter. The device will convert 5.0 V into −5.0 V with light loads. Two capacitors are required for the inverter to function. A third capacitor, the input bypass capacitor, may be required depending on the power source for the inverter. The performance for this device is illustrated below.

**Figure 19. Inverter Load Regulation, Output Voltage vs. Output Current**

**Figure 20. Cascaded Devices for Increased Negative Output Voltage**

Two or more devices can be cascaded for increased output voltage. Under light load conditions, the output voltage is approximately equal to −\( V_{\text{in}} \) times the number of stages. The converter output resistance increases dramatically with each additional stage. This is due to a reduction of input voltage to each successive stage as the converter output is loaded. Note that the ground connection for each successive stage must connect to the negative output of the previous stage. The performance characteristics for a converter consisting of two cascaded devices are shown below.

**Figure 21. Cascade Load Regulation, Output Voltage vs. Output Current**

<table>
<thead>
<tr>
<th>Curve</th>
<th>( V_{\text{in}} ) (V)</th>
<th>( R_{\text{out}} ) (( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>5.0</td>
<td>140</td>
</tr>
<tr>
<td>B</td>
<td>3.0</td>
<td>174</td>
</tr>
</tbody>
</table>
A single device can be used to construct a negative voltage doubler. The output voltage is approximately equal to \(-2V\text{in}\) minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.

![Figure 22. Negative Output Voltage Doubler](image)

![Figure 23. Doubler Load Regulation, Output Voltage vs. Output Current](image)

![Figure 24. Negative Output Voltage Tripler](image)
A single device can be used to construct a negative voltage tripler. The output voltage is approximately equal to $-3V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.

![Figure 25. Tripler Load Regulation, Output Voltage vs. Output Current](image)

<table>
<thead>
<tr>
<th>Curve</th>
<th>$V_{in}$ (V)</th>
<th>All Diodes</th>
<th>$R_{out}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.0</td>
<td>1N4148</td>
<td>267</td>
</tr>
<tr>
<td>B</td>
<td>3.0</td>
<td>MBRA120E</td>
<td>250</td>
</tr>
<tr>
<td>C</td>
<td>5.0</td>
<td>1N4148</td>
<td>205</td>
</tr>
<tr>
<td>D</td>
<td>5.0</td>
<td>MBRA120E</td>
<td>195</td>
</tr>
</tbody>
</table>

A single device can be used to construct a positive voltage doubler. The output voltage is approximately equal to $2V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.

![Figure 26. Positive Output Voltage Doubler](image)

<table>
<thead>
<tr>
<th>Curve</th>
<th>$V_{in}$ (V)</th>
<th>All Diodes</th>
<th>$R_{out}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.0</td>
<td>1N4148</td>
<td>32</td>
</tr>
<tr>
<td>B</td>
<td>3.0</td>
<td>MBRA120E</td>
<td>26</td>
</tr>
<tr>
<td>C</td>
<td>5.0</td>
<td>1N4148</td>
<td>26</td>
</tr>
<tr>
<td>D</td>
<td>5.0</td>
<td>MBRA120E</td>
<td>21</td>
</tr>
</tbody>
</table>

![Figure 27. Doubler Load Regulation, Output Voltage vs. Output Current](image)
A single device can be used to construct a positive voltage tripler. The output voltage is approximately equal to $3V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.

![Figure 28. Positive Output Voltage Tripler](image)

![Figure 29. Tripler Load Regulation, Output Voltage vs. Output Current](image)

![Figure 30. Load Regulated Negative Output Voltage](image)
A zener diode can be used with the shutdown input to provide closed loop regulation performance. This significantly reduces the converter’s output resistance and dramatically enhances the load regulation. For closed loop operation, the desired regulated output voltage must be lower in magnitude than \(-V_{in}\). The output will regulate at a level of \(-V_z + V_{\text{SHDN}}\). Note that the shutdown input voltage threshold is typically 0.5 \(V_{in}\) and therefore, the regulated output voltage will change proportional to the converter’s input. This characteristic will not present a problem when used in applications with constant input voltage. In this case the zener breakdown was measured at 25 \(\mu\)A. The performance characteristics for the above converter are shown below. Note that the dashed curve sections represent the converter’s open loop performance.

![Graph](image1)

**Figure 31. Load Regulation, Output Voltage vs. Output Current**

**Table 1**

<table>
<thead>
<tr>
<th>Curve</th>
<th>(V_{in}) (V)</th>
<th>(V_z) (V)</th>
<th>(V_{out}) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.3</td>
<td>4.5</td>
<td>−2.8</td>
</tr>
<tr>
<td>B</td>
<td>5.0</td>
<td>6.5</td>
<td>−3.8</td>
</tr>
</tbody>
</table>

![Diagram](image2)

**Figure 32. Line and Load Regulated Negative Output Voltage**
An adjustable shunt regulator can be used with the shutdown input to give excellent closed loop regulation performance. The shunt regulator acts as a comparator with a precise input offset voltage which significantly reduces the converter’s output resistance and dramatically enhances the line and load regulation. For closed loop operation, the desired regulated output voltage must be lower in magnitude than \( -V_{\text{in}} \). The output will regulate at a level of \( -V_{\text{ref}} \left( \frac{R_2}{R_1} + 1 \right) \). The adjustable shunt regulator can be from either the TLV431 or TL431 families. The comparator offset or reference voltage is 1.25 V or 2.5 V respectively. The performance characteristics for the converter are shown below. Note that the dashed curve sections represent the converter’s open loop performance.

![Figure 33. Load Regulation, Output Voltage vs. Output Current](image1)

![Figure 34. Line Regulation, Output Voltage vs. Input Current](image2)

<table>
<thead>
<tr>
<th>Curve</th>
<th>( V_{\text{in}} ) (V)</th>
<th>( R_1 ) (( \Omega ))</th>
<th>( R_2 ) (( \Omega ))</th>
<th>( V_{\text{out}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.0</td>
<td>10 k</td>
<td>5.0 k</td>
<td>−1.8</td>
</tr>
<tr>
<td>B</td>
<td>5.0</td>
<td>10 k</td>
<td>20 k</td>
<td>−3.6</td>
</tr>
</tbody>
</table>

![Figure 35. Paralleling Devices for Increased Negative Output Current](image3)

Capacitors = 10 \( \mu \text{F} \)
An increase in converter output current capability with a reduction in output resistance can be obtained by paralleling two or more devices. The output current capability is approximately equal to the number of devices paralleled. A single shared output capacitor is sufficient for proper operation but each device does require its own pump capacitor. Note that the output ripple frequency will be complex since the oscillators are not synchronized. The performance characteristics for a converter consisting of two paralleled devices is shown below.

<table>
<thead>
<tr>
<th>Curve</th>
<th>$V_{in}$ (V)</th>
<th>$R_{out}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>5.0</td>
<td>14.5</td>
</tr>
<tr>
<td>B</td>
<td>3.0</td>
<td>17</td>
</tr>
</tbody>
</table>

![Figure 36. Parallel Load Regulation, Output Voltage vs. Output Current](image)

The output current capability of the MAX1720 can be extended beyond 600 mA with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $-V_{in}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter are shown below. Note that the output resistance is reduced to $0.9 \, \Omega$.

![Figure 37. External Switch for Increased Negative Output Current](image)

![Figure 38. Current Boosted Load Regulation, Output Voltage vs. Output Current](image)
This converter is a combination of Figures 37 and 32. It provides a line and load regulated output of $-2.36$ V at up to 450 mA with an input voltage of 5.0 V. The output will regulate at a level of $-\text{V}_{\text{ref}} (R_2/R_1 + 1)$. The performance characteristics are shown below. Note, the dashed line is the open loop and the solid line is the closed loop performance.
The MAX1720 can be configured to produce a positive output voltage doubler with current capability in excess of 500 mA. This is accomplished with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $2V_{in}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter is shown below. Note that the output resistance is reduced to 1.9 Ω.

![Figure 43. Positive Doubler with Current Boosted Load Regulation, Output Voltage vs. Output Current](image)

Figure 43. Positive Doubler with Current Boosted Load Regulation, Output Voltage vs. Output Current

This converter is a combination of Figures 42 and the shunt regulator to close the loop. In this case the anode of the regulator is connected to ground. This convert provides a line and load regulated output of 7.6 V at up to 300 mA with an input voltage of 5.0 V. The output will regulate at a level of $V_{ref} \left(\frac{R_2}{R_1} + 1\right)$. The open loop configuration is the dashed line and the closed loop is the solid line. The performance characteristics are shown below.

![Figure 44. Line and Load Regulated Positive Output Voltage Doubler with High Current Capability](image)

Figure 44. Line and Load Regulated Positive Output Voltage Doubler with High Current Capability

![Figure 45. Current Boosted Close Loop Load Regulation, Output Voltage vs. Output Current](image)

Figure 45. Current Boosted Close Loop Load Regulation, Output Voltage vs. Output Current

![Figure 46. Current Boosted Close Loop Line Regulation, Output Voltage vs. Input Voltage](image)

Figure 46. Current Boosted Close Loop Line Regulation, Output Voltage vs. Input Voltage
A single device can be used to split a negative input voltage. The output voltage is approximately equal to \(-\frac{V_{\text{in}}}{2}\). The performance characteristics are shown below. Note that the converter has an output resistance of 10 \(\Omega\).
All of the previously shown converter circuits have only single outputs. Applications requiring multiple outputs can be constructed by incorporating combinations of the former circuits. The converter shown above combines Figures 26 and 32 to form a regulated negative output inverter with a non-regulated positive output doubler. The magnitude of \( V_{\text{out}} \) is controlled by the resistor values and follows the relationship \( -V_{\text{ref}} \left( R_2/R_1 + 1 \right) \). Since the positive output is not within the feedback loop, its output voltage will increase as the negative output load increases. This cross regulation characteristic is shown in the upper portion of Figure 50. The dashed line is the open loop and the solid line is the closed loop configuration for the load regulation. The load regulation for the positive doubler with a constant load on the \( V_{\text{out}} \) is shown in Figure 51.
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor*

TSOP–6
CASE 318G–02
ISSUE V

DATE 12 JUN 2012

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM
LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR
GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D
AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIMENSIONS: MILLIMETERS

NOTES:
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5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

STYLes:

STYLE 1:
- PIN 1: DRAIN
- 2: BASE 1
- 3: GATE
- 4: SOURCE
- 5: DRAIN
- 6: DRAIN

STYLE 2:
- PIN 1: GATE
- 2: DRAIN
- 3: SOURCE
- 4: N/C
- 5: COLLECTOR
- 6: BASE

STYLE 3:
- PIN 1: ENABLE
- 2: N/C
- 3: Vz
- 4: GATE
- 5: V IN
- 6: V OUT

STYLE 4:
- PIN 1: N/C
- 2: V IN
- 3: D IN+
- 4: D IN
- 5: D OUT+
- 6: D OUT

STYLE 5:
- PIN 1: COLLECTOR
- 2: BASE
- 3: SOURCE
- 4: EMITTER
- 5: LOAD
- 6: COLLECTOR

STYLE 6:
- PIN 1: COLLECTOR
- 2: BASE
- 3: SOURCE
- 4: EMITTER
- 5: LOAD
- 6: COLLECTOR

STYLE 7:
- PIN 1: COLLECTOR
- 2: COLLECTOR
- 3: BASE
- 4: N/C
- 5: COLLECTOR
- 6: EMITTER

STYLE 8:
- PIN 1: V BUS
- 2: D(IN)
- 3: D(IN+)
- 4: D(OUT)
- 5: D(OUT+)
- 6: D(OUT)

STYLE 9:
- PIN 1: LOW VOLTAGE GATE
- 2: DRAIN
- 3: SOURCE
- 4: DRAIN
- 5: V BUS
- 6: D(IN+)

STYLE 10:
- PIN 1: D(OUT)+
- 2: GND
- 3: COLLECTOR
- 4: SOURCE
- 5: LOAD
- 6: COLLECTOR

STYLE 11:
- PIN 1: SOURCE 1
- 2: DRAIN 2
- 3: DRAIN 2
- 4: D(IN)
- 5: V BUS
- 6: D(IN+)

STYLE 12:
- PIN 1: I/O
- 2: BASE
- 3: ANODE
- 4: COLLECTOR
- 5: ANODE
- 6: COLLECTOR

STYLE 13:
- PIN 1: GATE 1
- 2: SOURCE 2
- 3: GATE 2
- 4: SOURCE 1
- 5: DRAIN 1
- 6: DRAIN 1

STYLE 14:
- PIN 1: ANODE
- 2: SOURCE
- 3: GATE
- 4: CATHODE/DRAIN
- 5: DRAIN 2
- 6: DRAIN 2

STYLE 15:
- PIN 1: ANODE
- 2: SOURCE
- 3: GATE
- 4: DRAIN
- 5: N/C
- 6: CATHODE

STYLE 16:
- PIN 1: ANODE/CATHODE
- 2: BASE
- 3: EMITTER
- 4: COLLECTOR
- 5: ANODE/CATHODE
- 6: CATHODE

STYLE 17:
- PIN 1: EMITTER
- 2: BASE
- 3: COLLECTOR
- 4: ANODE
- 5: CATHODE
- 6: COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*

Dimensions: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER: 98ASB14888C
DESCRIPTION: TSOP–6

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