



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## LV4912GP — Bi-CMOS LSI Class-D Audio Power Amplifier BTL 2W×1ch

### Overview

The LV4912GP is analog input type digital power amplifier with 2W × 1 channel. By using an original feed back technology, it improves sound quality through it is class-D power amplifier and the LC filter in the output stage can be deleted as application.

### Features

- Enabling output LC filter-less.
- Class-D amplifier system of the output BTL type.
- Improve the sound quality by the use of original feedback technology.
- Realized high efficiency class-D amplifier.
- Reduce the pop sound at ON/OFF state by the use of soft mute function.
- Full complement of built-in protection circuits : over current protection, thermal protection, and low power supply voltage protection circuits.
- Internal oscillation frequency : 280kHz

### Functions

- Output power : 2W(V<sub>D</sub> = 5V, R<sub>L</sub> = 4Ω, THD + N = 10%)
- THD + N : 0.4% (V<sub>D</sub> = 5V, R<sub>L</sub> = 4Ω, f<sub>in</sub> = 1kHz, P<sub>O</sub> = 1W, Filter : AES17)
- Noise : 70μV<sub>rms</sub> (Filter : DIN AUDIO)
- Package : VCT24 (3.5 × 3.5)

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# LV4912GP

## Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

| Parameter                   | Symbol | Conditions                 | Ratings     | Unit             |
|-----------------------------|--------|----------------------------|-------------|------------------|
| Maximum supply voltage      | VD     | Externally applied voltage | 6           | V                |
| Allowable power dissipation | Pd max | Mounted on a board *       | 1           | W                |
| Operating temperature       | Topr   |                            | -20 to +75  | $^\circ\text{C}$ |
| Storage temperature         | Tstg   |                            | -40 to +150 | $^\circ\text{C}$ |

\* When mounted on the specified printed circuit board : 40mm×50mm×1.6mm, glass epoxy

Recommended Operation Conditions at  $T_a = 25^\circ\text{C}$

| Parameter            | Symbol         | Conditions                 | Ratings |     |     | Unit     |
|----------------------|----------------|----------------------------|---------|-----|-----|----------|
|                      |                |                            | min     | typ | max |          |
| Supply voltage range | VD             | Externally applied voltage | 2.7     | 5   | 5.5 | V        |
| Load impedance range | R <sub>L</sub> | Speaker load               | 4       |     |     | $\Omega$ |

Electrical Characteristics at  $T_a = 25^\circ\text{C}$ , VD = 5V, R<sub>L</sub> = 4 $\Omega$ , L = 22 $\mu\text{H}$ , C = 0.33 $\mu\text{F}$

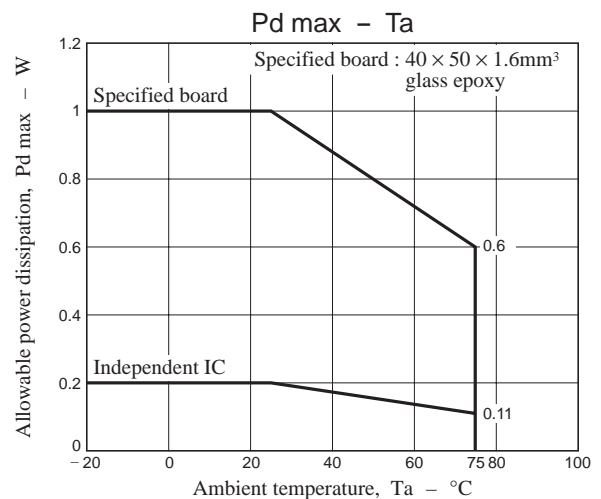
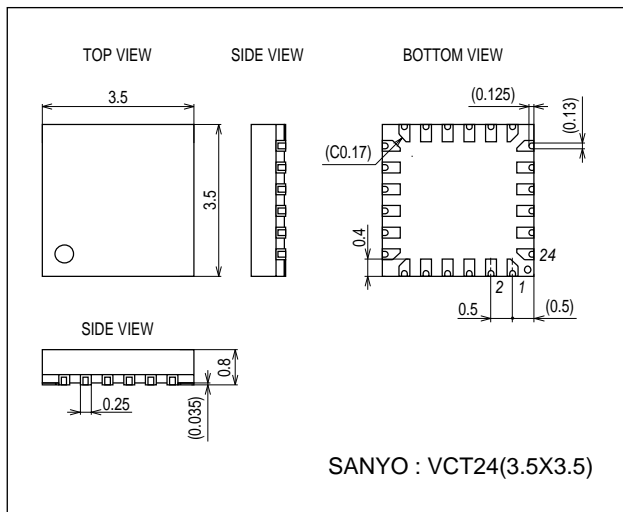
| Parameter  | Symbol            | Conditions   | Ratings |      |      | Unit             |
|--|-------------------|--|---------|------|------|------------------|
|  |                   |  | min     | typ  | max  |                  |
| <b>Operating current</b>                                       |                   |  |         |      |      |                  |
| Standby current  | I <sub>st</sub>   | $\overline{\text{STBY}} = \text{L}$ , $\overline{\text{MUTE}} = \text{L}$ , LC less, R <sub>L</sub> = OPEN |         | 1    | 8    | $\mu\text{A}$    |
| Mute current   | I <sub>mute</sub> | $\overline{\text{STBY}} = \text{H}$ , $\overline{\text{MUTE}} = \text{L}$ , LC less, R <sub>L</sub> = OPEN |         | 4.5  | 7.5  | mA               |
| Quiescent current  | I <sub>CCO</sub>  | $\overline{\text{STBY}} = \text{H}$ , $\overline{\text{MUTE}} = \text{H}$ , LC less, R <sub>L</sub> = OPEN |         | 6    | 10   | mA               |
| <b>Main amplifier</b>  |                   |  |         |      |      |                  |
| Voltage gain   | VG                | fin = 1kHz, V <sub>O</sub> = 0dBm  | 21.5    | 23.5 | 25.5 | dB               |
| Total harmonic distortion                                      | THD+N             | P <sub>O</sub> = 1W, fin = 1kHz, AES17   |         | 0.4  | 0.7  | %                |
| Output power   | P <sub>O</sub>    | THD+N = 10%, fin = 1kHz, AES17   | 1.6     | 2    |      | W                |
| Ripple rejection ratio   | SVRR              | fr = 100Hz, Vr = -15dBm, Rg = 0, DIN AUDIO   | 50      | 60   |      | dB               |
| Noise  | V <sub>NO</sub>   | Rg = 0, DIN AUDIO  |         | 70   | 210  | $\mu\text{Vrms}$ |
| <b>Digital input</b>   |                   |  |         |      |      |                  |
| High-level output voltage                                      | V <sub>IH</sub>   | STBY pin, MUTE pin   | 3       |      |      | V                |
| Low-level output voltage                                       | V <sub>IL</sub>   | STBY pin, MUTE pin   |         |      | 0.3  | V                |
| <b>Protection circuit</b>                                      |                   |  |         |      |      |                  |
| Power supply voltage drop protection circuit upper limit value | UV_UPPER          | VD pin voltage monitor   |         | 2.3  |      | V                |
| Power supply voltage drop protection circuit lower limit value | UV_LOWER          | VD pin voltage monitor   |         | 2.2  |      | V                |

Note : The values of these characteristics were measured in the SANYO test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

## Package Dimensions

unit : mm (typ)

3322A



# LV4912GP

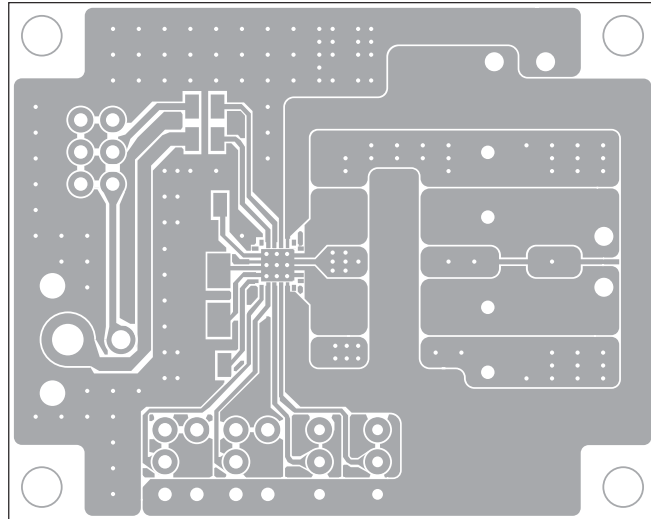
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LV4912GP customer bread board rev.1.0

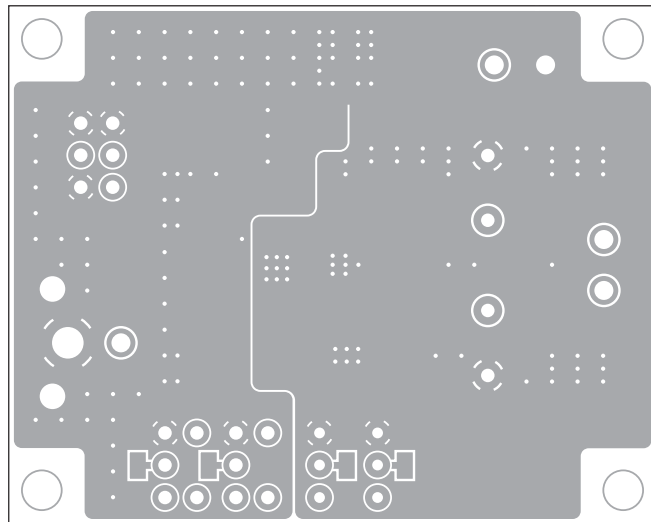
Size : 40mm × 50mm × 1.6mm

Pattern

Top Layer

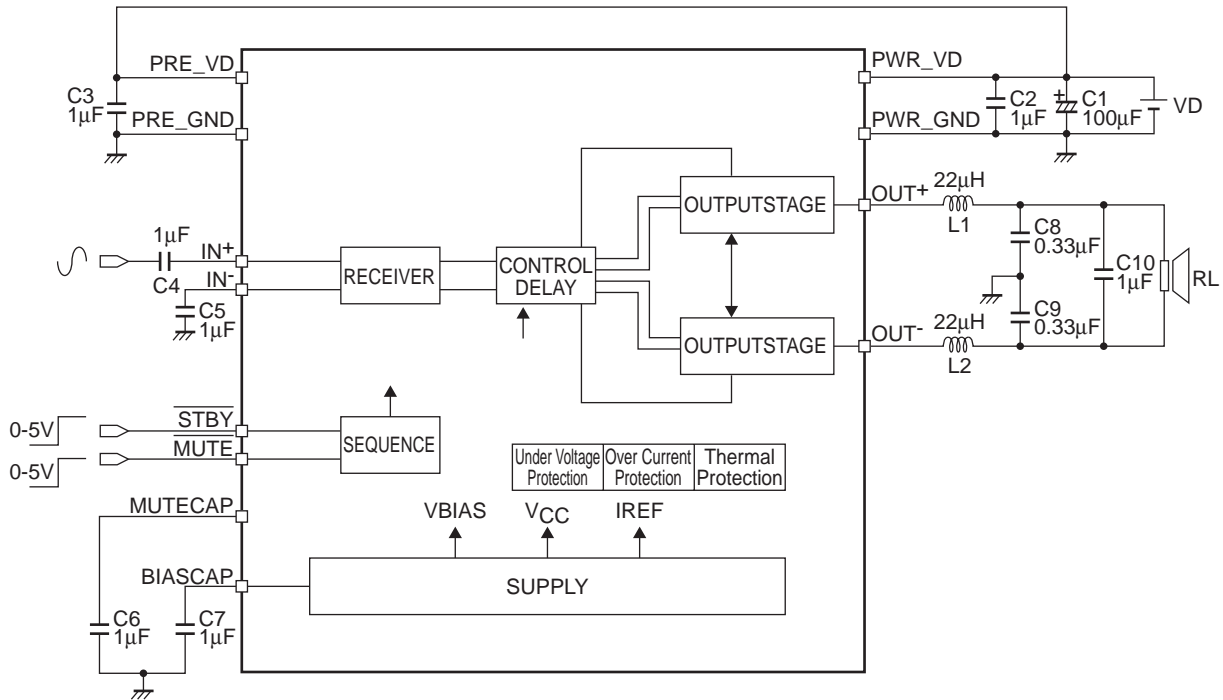


Bottom Layer



# LV4912GP

## Block Diagram and Application Circuit Example ( $R_L = 4\Omega$ )

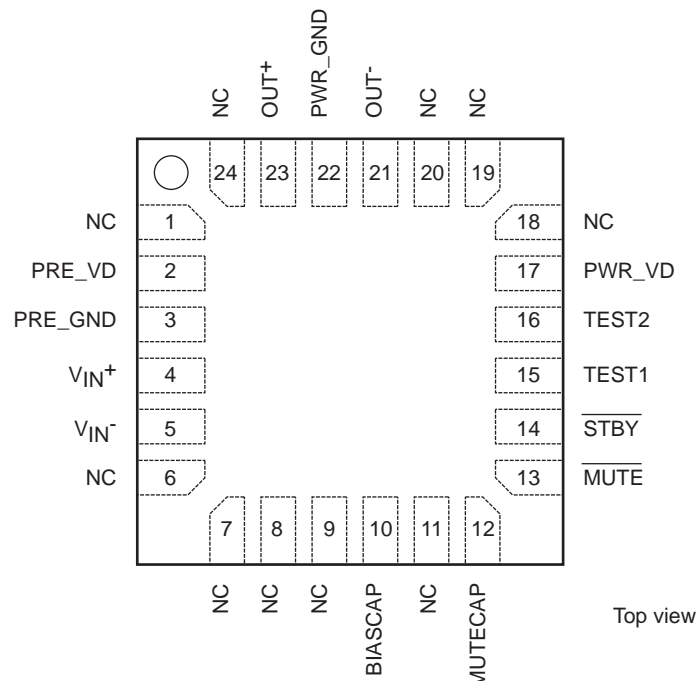


## LV4912GP Application ( $R_L = 4\Omega$ )

### Part List

| Parts Name    | Part No.    | Description Function                                       |
|---------------|-------------|--|
| $C_{VD}$      | C1          | Power supply capacitor for VD                              |
| $C_{VD}$      | C2, C3      | High-frequency cut capacitor for VD                        |
| $C_{IN}$      | C4, C5      | Input capacitor  |
| $C_{MUTE}$    | C6          | Capacitor for soft mute                                    |
| $C_{BIASCAP}$ | C7          | Input coupling capacitor for Internal power supply (VBIAS) |
| $L_O$         | L1, L2      | Output L. P. F. coil                                       |
| $C_O$         | C8, C9, C10 | Output L. P. F. capacitor                                  |

### Pin Assignments



# LV4912GP

## Pin Equivalent Circuit

| Pin No. | Pin Name                     | I/O | Description   | Equivalent Circuit |
|---------|------------------------------|-----|---|--------------------|
| 1       | NC                           |     | No connection   |                    |
| 2       | PRE_VD                       |     | Power supply pin                                      |                    |
| 3       | PRE_GND                      |     | Pre ground  |                    |
| 4       | V <sub>IN</sub> <sup>+</sup> | I   | Input plus  |                    |
| 5       | V <sub>IN</sub> <sup>-</sup> | I   | Input minus   |                    |
| 6       | NC                           |     | No connection   |                    |
| 7       | NC                           |     | No connection   |                    |
| 8       | NC                           |     | No connection   |                    |
| 9       | NC                           |     | No connection   |                    |
| 10      | BIASCAP                      | O   | Internal power supply decoupling capacitor connection |                    |
| 11      | NC                           |     | No connection   |                    |
| 12      | MUTECAP                      | O   | Mute capacitor connection                             |                    |
| 13      | MUTE                         | I   | Mute control pin                                      |                    |

Continued on next page.

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Continued from preceding page.

| Pin No. | Pin Name                 | I/O | Description         | Equivalent Circuit |
|---------|--------------------------|-----|---------------------|--------------------|
| 14      | $\overline{\text{STBY}}$ | I   | Standby control pin |                    |
| 15      | TEST1                    |     | Test pin            |                    |
| 16      | TEST2                    |     | Test pin            |                    |
| 17      | PWR_VD                   |     | Power supply pin    |                    |
| 18      | NC                       |     | No connection       |                    |
| 19      | NC                       |     | No connection       |                    |
| 20      | NC                       |     | No connection       |                    |
| 21      | OUT-                     | O   | Output pin, minus   |                    |
| 22      | PWR_GND                  |     | Power ground        |                    |
| 23      | OUT+                     | O   | Output pin, plus    |                    |
| 24      | NC                       |     | No connection       |                    |

## Description functions

### 1. System Standby

Each bias can be turned on/off by switching the STBY pin (pin 14) into high or low. The bias is turned off when the STBY pin is low. Conversely, the bias is turned on when the STBY pin is high.

| STBY pin (pin 14) | Bias condition |
|-------------------|----------------|
| High              | ON             |
| Low               | OFF            |

### 2. Mute Function

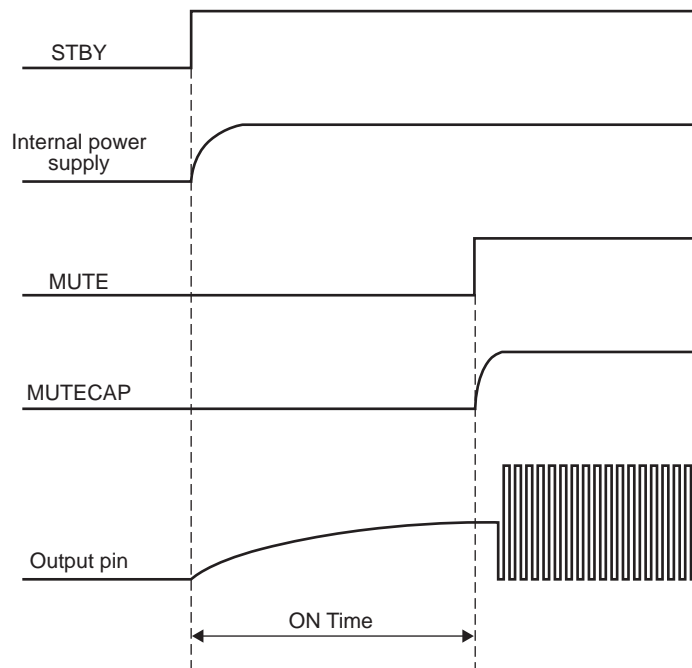
The mute of the output and reduction of power-on popping noise are mainly performed by the use of this function. By switching between high and low on the MUTE pin (pin 13), the output can be muted. The MUTE pin enters the mute mode (PWM output stops) when the MUTE pin is low. Also the MUTE pin enters the operation mode (normal operations) when the MUTE pin is high.

| MUTE pin (pin 13) | Conditions     |
|-------------------|----------------|
| High              | Operation mode |
| Low               | Mute mode      |

We recommend the following sequence for reduction of the popping noise when power is on/off. Also, we recommend the following ON Time and OFF Time when P.4 the application circuit is used.

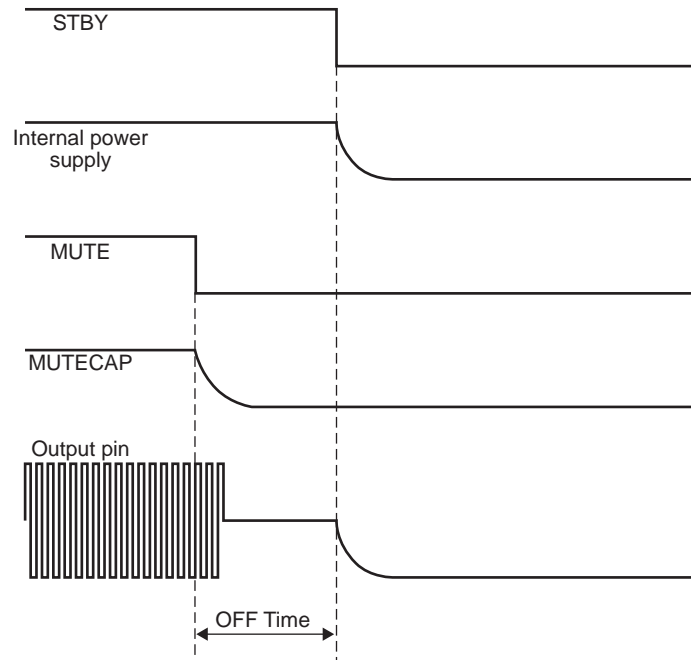
#### (1) Power On sequence

The ON Time should secure more than 150msec for reduction of the popping noise.



## (2) Power Down sequence

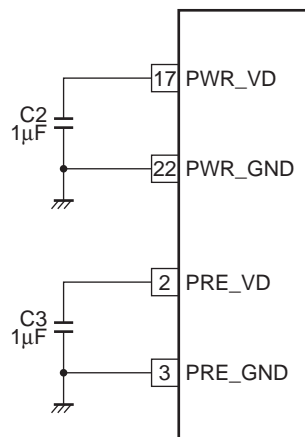
The OFF Time should secure more than 100msec for reduction of the popping noise.



## Capacitors for Power supply and pin arrangement

### 1. Capacitors for power supply

The capacitors C2 and C3 for power supply connected between IC pins must be inserted using the shortest lines possible.

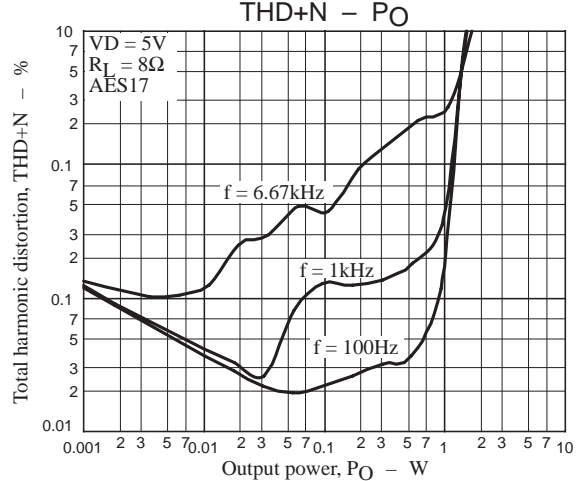
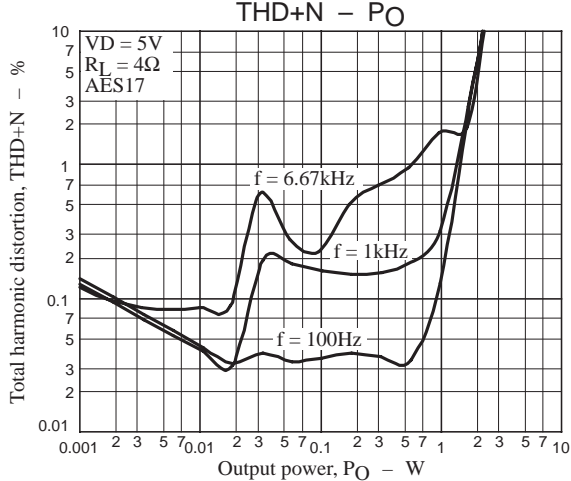
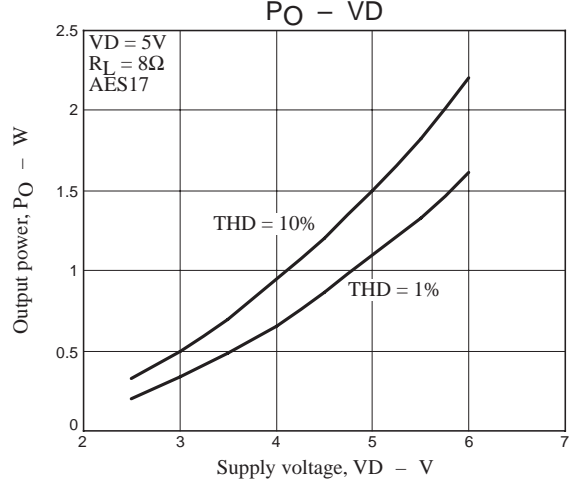
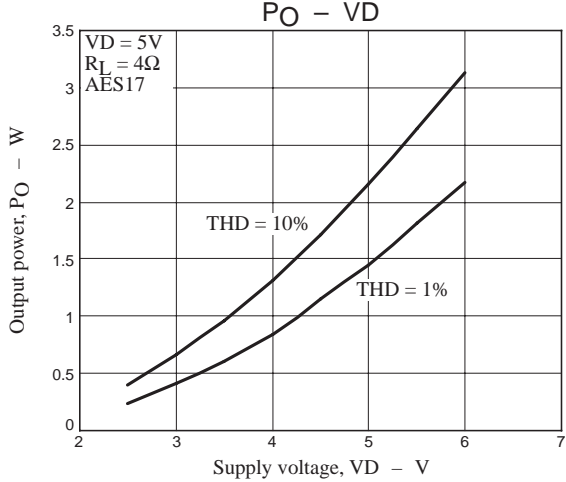
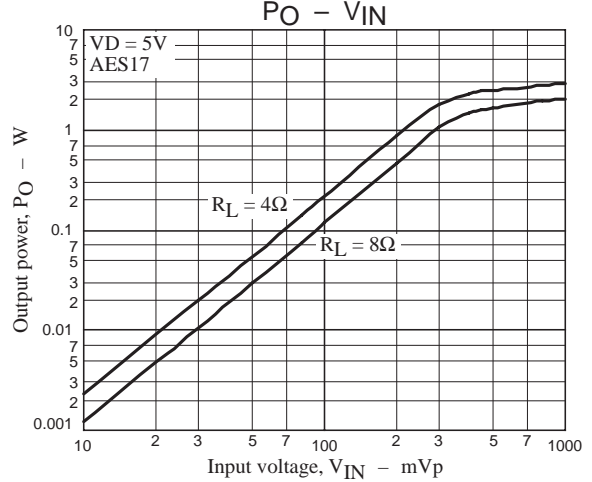
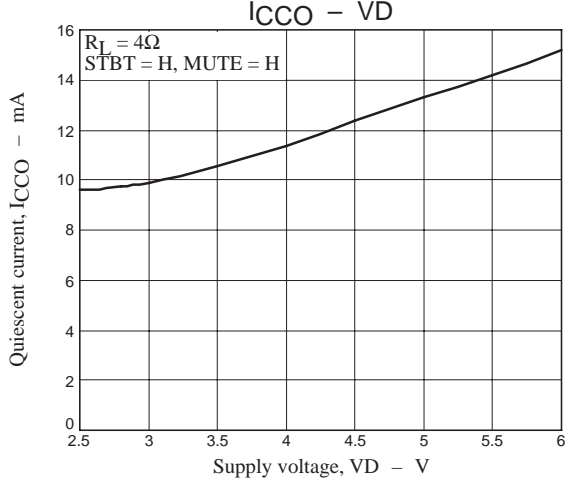
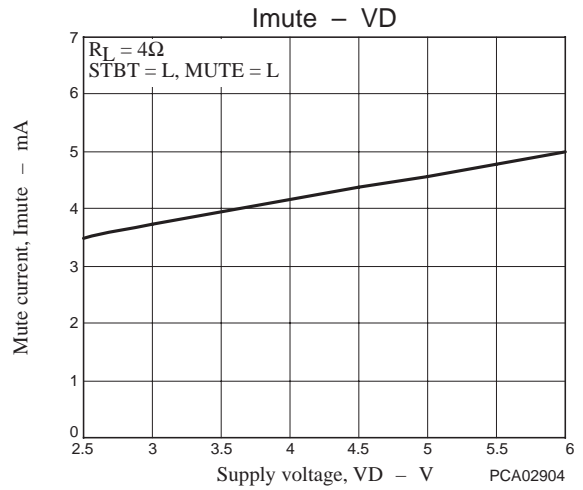
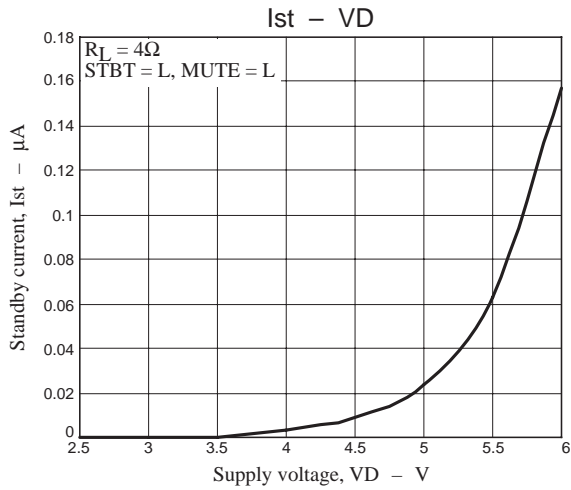


### 2. Pin arrangement of the test pins (pins 15 and 16)

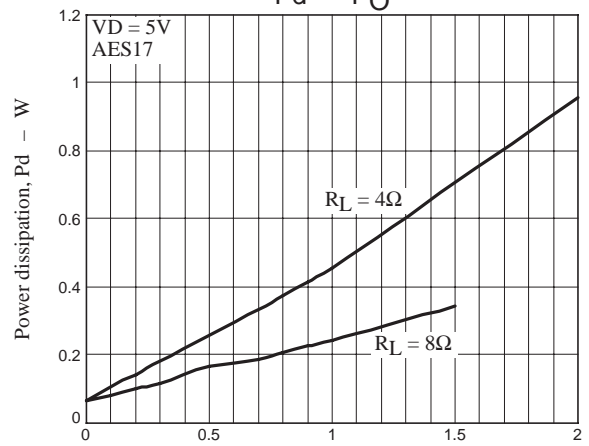
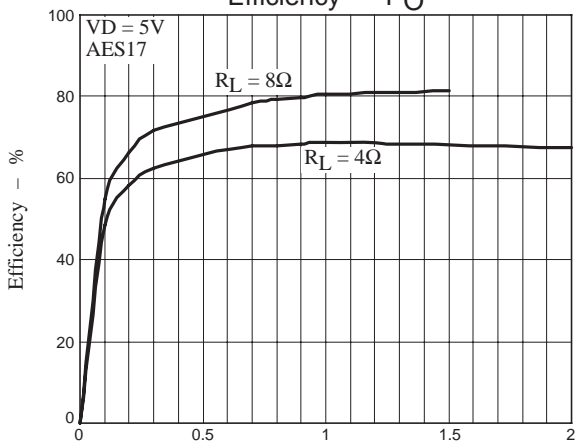
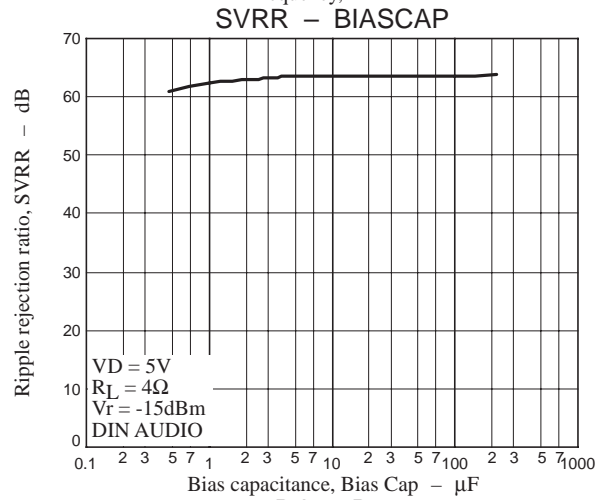
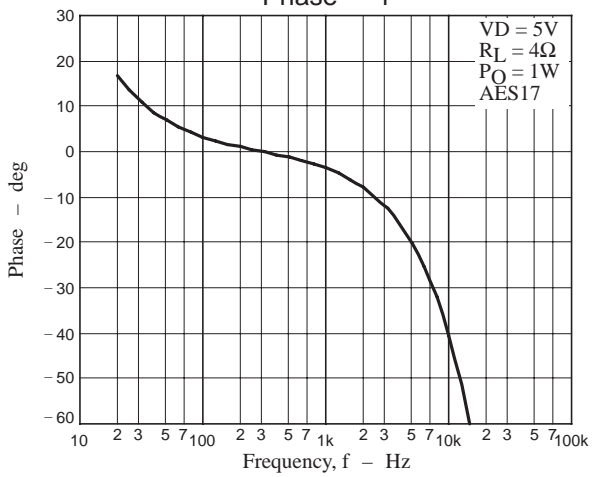
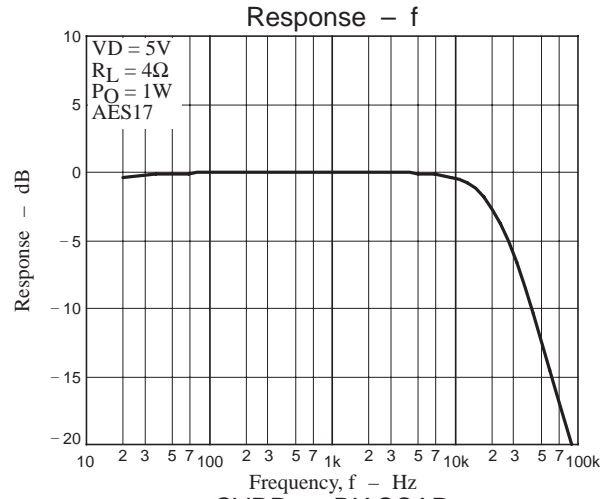
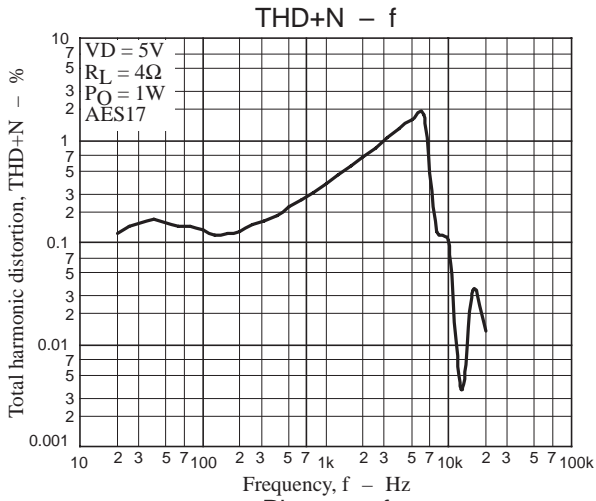
The test pins (pins 15 and 16) are used as pins for testing before shipment. These pins are not used normally. Therefore, these pins must be left open if the pin arrangement is not performed. Please make sure to connect these pins to GNDs if the pin arrangement is performed.



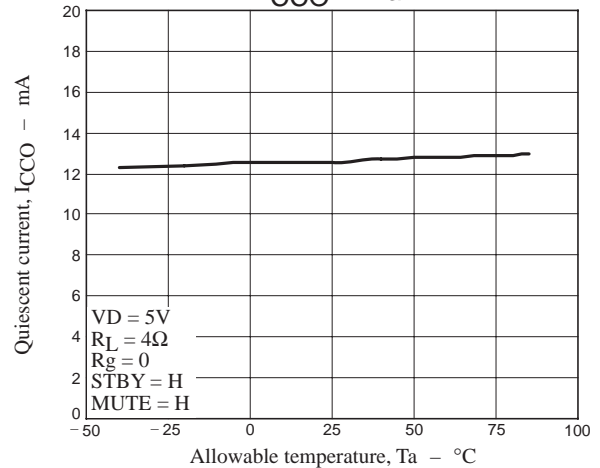
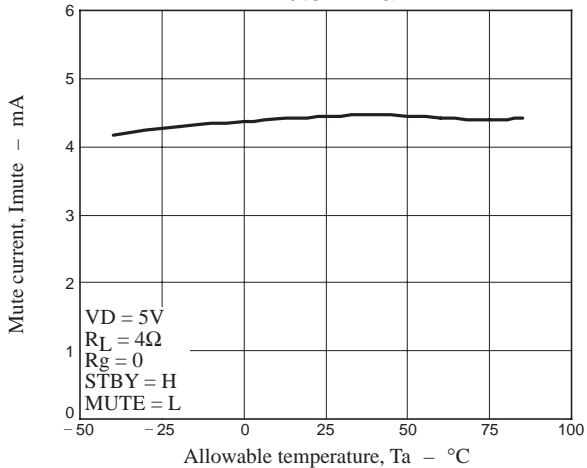
## General Characteristics

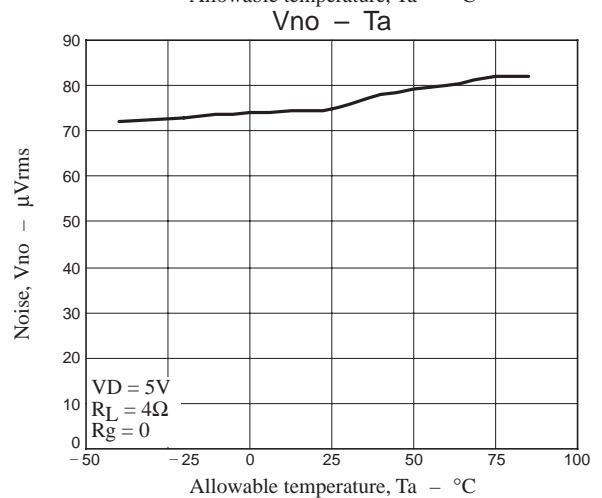
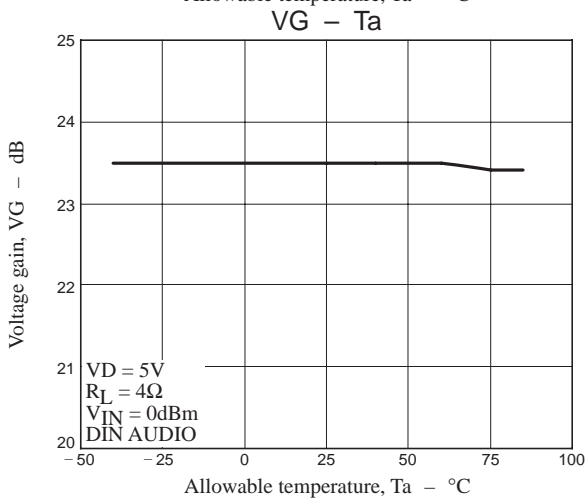
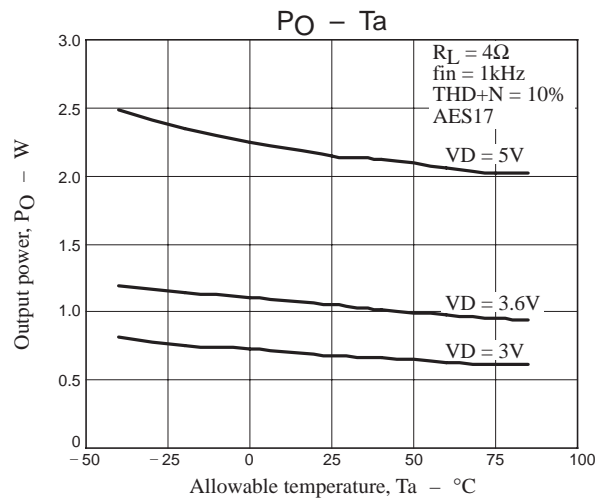
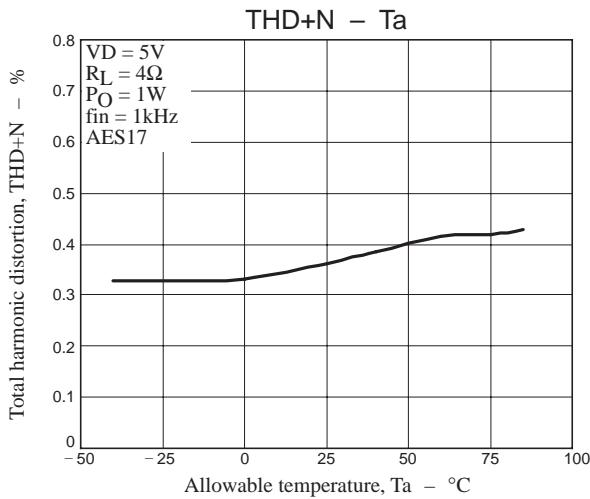


# LV4912GP



## Temperature Characteristics





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