LV11961HA

FAN Motor Driver, Single-phase

Overview
LV11961HA is a driver IC for single-phase fan motor that easily implements direct PWM motor drive system with excellent efficiency. LV11961HA is optimal for fan motor drive in personal computer power supply systems and CPU cooling systems.

Features
• Single-phase full wave drive (built-in power FETs)
• Speed control function by DC voltage input to VTH pin
• Minimum speed adjustment by fixed voltage input to RMI pin
• Soft start-up function by SFS pin
• Regulated voltage output pin for Hall bias
• Built-in lock protector and auto recovery circuit
• FG signal output pin, RD signal output pin
• Built-in TSD (Thermal shutdown) circuit

Typical Applications
• Fan motor units
• Note PCs
• Desk top PCs
• Projectors

ORDERING INFORMATION
Ordering Code:
LV11961HA-AH

Package
HSSOP14 (225mil)
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “‡”, may or may not be present.
## Specifications

### Absolute Maximum Ratings

at $T_a = 25^\circ$C (Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>$V_{CC\text{max}}$</td>
<td></td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Output pin current</td>
<td>$I_{OUT\text{max}}$</td>
<td></td>
<td>1.0</td>
<td>A</td>
</tr>
<tr>
<td>Output pin peak current</td>
<td>$I_{\text{Opeak max}}$</td>
<td>Duty $\leq$ 10%</td>
<td>1.2</td>
<td>A</td>
</tr>
<tr>
<td>Output pin with stand voltage</td>
<td>$V_{OUT\text{max}}$</td>
<td></td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>REG output maximum current</td>
<td>$I_{\text{REGmax}}$</td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>HB output maximum current</td>
<td>$I_{HB\text{max}}$</td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>VTH pin voltage</td>
<td>$V_{TH\text{max}}$</td>
<td></td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>FG/RG output pin voltage</td>
<td>$V_{FG/VR\text{Dmax}}$</td>
<td></td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>FG/RG pin sink current</td>
<td>$I_{FG/IR\text{Dmax}}$</td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Allowable power dissipation</td>
<td>$P_{d\text{max}}$</td>
<td>Mounted on specified board (Note 2)</td>
<td>1.1</td>
<td>W</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>$T_{OP}$</td>
<td>(Note 3)</td>
<td>–40 to +95</td>
<td>$^\circ$C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{STG}$</td>
<td></td>
<td>–55 to +150</td>
<td>$^\circ$C</td>
</tr>
</tbody>
</table>

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Specified board: 114.3mm x 76.1mm x 1.6mm, glass epoxy board
3. Do not exceed $T_{J\text{max}}=150^\circ$C

### Recommendation Operating Condition

at $T_a = 25^\circ$C (Note 4)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating supply voltage</td>
<td>$V_{CC\text{op}}$</td>
<td></td>
<td>3.6</td>
<td>12</td>
</tr>
<tr>
<td>VTH pin input voltage</td>
<td>$V_{TH\text{op}}$</td>
<td></td>
<td>0</td>
<td>$V_{REG}$</td>
</tr>
<tr>
<td>RMI pin input voltage</td>
<td>$V_{RM\text{Iop}}$</td>
<td></td>
<td>0</td>
<td>$V_{REG}$</td>
</tr>
<tr>
<td>IN1/IN2 pin input voltage</td>
<td>$V_{IC\text{M}}$</td>
<td></td>
<td>0.2</td>
<td>$V_{REG}$</td>
</tr>
<tr>
<td>CPWM pin oscillation frequency range</td>
<td>$f_{CP\text{WM}}$</td>
<td></td>
<td>20</td>
<td>100</td>
</tr>
</tbody>
</table>

4. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### Electrical Characteristics

at $T_a = 25^\circ$C, $V_{CC} = 12$V (Note 5)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit current</td>
<td>$I_{CC}$</td>
<td></td>
<td>2.0</td>
<td>3.0</td>
</tr>
<tr>
<td>REG pin voltage</td>
<td>$V_{\text{REG}}$</td>
<td>$I_{\text{REG}}=5$mA</td>
<td>2.80</td>
<td>3.15</td>
</tr>
<tr>
<td>HB pin voltage</td>
<td>$V_{HB}$</td>
<td>$I_{HB}=5$mA</td>
<td>1.08</td>
<td>1.2</td>
</tr>
<tr>
<td>CPWM pin high threshold level</td>
<td>$V_{CP\text{H}}$</td>
<td></td>
<td>2.05</td>
<td>2.15</td>
</tr>
<tr>
<td>CPWM pin low threshold level</td>
<td>$V_{CP\text{L}}$</td>
<td></td>
<td>0.57</td>
<td>0.62</td>
</tr>
<tr>
<td>CPWM amplitude</td>
<td>$D_{CP}$</td>
<td></td>
<td>1.41</td>
<td>1.53</td>
</tr>
<tr>
<td>CPWM pin charge current</td>
<td>$I_{CP\text{PWM}}$</td>
<td>$V_{CP\text{PWM}}=1.4$V</td>
<td>19</td>
<td>24</td>
</tr>
<tr>
<td>CPWM pin discharge current</td>
<td>$I_{CP\text{PWM}}$</td>
<td>$V_{CP\text{PWM}}=1.4$V</td>
<td>–32</td>
<td>–24</td>
</tr>
<tr>
<td>SFS pin charge current</td>
<td>$I_{SFS}$</td>
<td></td>
<td>0.75</td>
<td>1.25</td>
</tr>
<tr>
<td>SFS pin clamp voltage</td>
<td>$V_{SFS\text{CL}}$</td>
<td></td>
<td>0.2</td>
<td>0.4</td>
</tr>
<tr>
<td>Sensitivity to hall input</td>
<td>$V_{HI\text{N}}$</td>
<td>Design target (Note 6)</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>OUT pin low level voltage</td>
<td>$V_{OL}$</td>
<td>$I_{OUT}=200$mA</td>
<td>0.11</td>
<td>0.17</td>
</tr>
<tr>
<td>OUT pin high level voltage</td>
<td>$V_{OH}$</td>
<td>$I_{OUT}=200$mA</td>
<td>0.18</td>
<td>0.27</td>
</tr>
<tr>
<td>FG/RD pin low level voltage</td>
<td>$V_{FG/VR\text{D}}$</td>
<td>$I_{OUT}=3$mA</td>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>FG/RD pin leak current</td>
<td>$I_{FG/IR\text{D}}$</td>
<td>$V_{FG/VR\text{D}}=18$V</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

Continued on next page
5. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Design target: These values are the target value in designs. The parameters are not measured independently.

### Truth table

<table>
<thead>
<tr>
<th>VTH</th>
<th>IN1</th>
<th>IN2</th>
<th>CPWM *1</th>
<th>OUT1</th>
<th>OUT2</th>
<th>FG</th>
<th>RD</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>L (OPEN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>ON</td>
<td>Driving</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>OFF</td>
<td>L</td>
<td>L</td>
<td>ON</td>
<td>Regenerating</td>
</tr>
<tr>
<td>-</td>
<td>L</td>
<td>H</td>
<td>-</td>
<td>L</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>(PWM-ON)</td>
</tr>
<tr>
<td>-</td>
<td>H</td>
<td>L</td>
<td>-</td>
<td>H</td>
<td>OFF</td>
<td>L</td>
<td>OFF</td>
<td>Lock protection</td>
</tr>
</tbody>
</table>

*1 CPWM=H : CPWM>VTH, CPWM=L : CPWM<VTH
Package Dimensions

unit: mm (typ)

HSSOP14 (225mil)
CASE 944AA
ISSUE A

NOTES:
1. The measurements are not to guarantee but for reference only.
2. Land pattern design in Fin area to be altered in response to customer's individual application.

*SOLDERING FOOTPRINT*

(Unit: mm)

0.32

0.65

0.5 ± 0.1

1.0

5.80

www.onsemi.com
LV11961HA

Pdmax-Ta diagram

Board mounted (114.3mm x 76.1mm x 1.6mm, glass epoxy)

Pin Assignment

Package: HSSOP14 (225mil)

- PGND (Frame)
- OUT2 1
- VCC 2
- RMI 3
- VTH 4
- CPWM 5
- FG 6
- RD 7
- 8
- IN1
- 9
- HB
- 10
- IN2
- 11
- REG
- 12
- SFS
- 13
- SGND
- 14
- OUT1

www.onsemi.com
## Pin function

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
<th>Equivalent circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT2</td>
<td>Output for motor drive(2).</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>VCC</td>
<td>Supply voltage input.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RMI</td>
<td>Input to adjust the minimum duty at PWM.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>VTH</td>
<td>Input to control PWM duty.</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CPWM</td>
<td>Output of oscillation for PWM.</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>FG</td>
<td>Output of motor rotational signal.</td>
<td></td>
</tr>
</tbody>
</table>

*Continued on next page*
Continued from preceding page.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
<th>Equivalent circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>RD</td>
<td>Output of motor lock detection.</td>
<td>![Equivalent Circuit for RD]</td>
</tr>
<tr>
<td>8</td>
<td>IN1</td>
<td>Input of hall signal (1).</td>
<td>![Equivalent Circuit for IN1]</td>
</tr>
<tr>
<td>9</td>
<td>HB</td>
<td>Output of regulated voltage for hall bias.</td>
<td>![Equivalent Circuit for HB]</td>
</tr>
<tr>
<td>10</td>
<td>IN2</td>
<td>Input of hall signal (2).</td>
<td>![Equivalent Circuit for IN2]</td>
</tr>
<tr>
<td>11</td>
<td>REG</td>
<td>Output of regulated voltage (3.2V). This voltage supplies power for internal circuits to control.</td>
<td>![Equivalent Circuit for REG]</td>
</tr>
</tbody>
</table>

Continued on next page
Continued from preceding page.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
<th>Equivalent circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>SFS</td>
<td>Input to adjust the time of soft starting.</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
</tr>
<tr>
<td>13</td>
<td>SGND</td>
<td>GND for internal circuits to control.</td>
<td></td>
</tr>
<tr>
<td>Frame</td>
<td>PGMD</td>
<td>GND to power MOSFETs. In addition, these pins contribute for radiation.</td>
<td></td>
</tr>
</tbody>
</table>
Functional description

- Start Up

In the condition that VTH and RMI level is higher than VCPWM level continuously over 1.5ms (typical), IC is in the sleep mode. Once VTH level is lower than VCPWM level, IC turns to be active and goes into the Start-up mode.

In the Start-up mode, PWM duty of OUT1 and 2 in start-up operation is decided by SFS level.

By connecting a capacitor between SFS pin and SGND, the voltage of SFS pin begins to increase soon after IC booting.

After IC booting, PWM output is in the mode of...

Driving (under the condition of SFS > CPWM in the charging period of CPWM)
Regenerating (the discharging period of CPWM and under the condition of SFS < CPWM in the charging period of CPWM)

The higher the voltage of SFS pin is, the larger the driving duty is. So, the driving current increases softly according to the increment of SFS level, as shown in Fig.1. This function is available not only in IC booting but in restart from lock protection.

The motor should begin to rotate by the increment of driving duty. After 8th FG edge from IC booting or restart, the control of PWM duty in outputs switches from SFS level to VTH level, as shown in Fig.2.
- PWM duty control

Duty of PWM output is determined by comparison of CPWM oscillation and DC level which is input to VTH pin.

PWM output is in the mode of ... 
- Driving (under the condition of CPWM > VTH)
- Regenerating (under the condition of CPWM < VTH)

The minimum duty of PWM output is determined by comparison of CPWM oscillation and DC level which is input to RMI pin.

High duty of PWM output is determined by ...
- VTH level (under the condition of RMI > VTH)
- RMI level (under the condition of RMI < VTH)

That is, high duty of PWM output decreases only to the one which is determined by RMI level.

![Diagram of PWM control](image_url)
- Soft switching
This IC operates to switch the driving phase of output softly by changing PWM duty gradually, which is called Soft switching.

The term of Soft switching is 18.75% of FG half cycle each before and after the time of phase switching, as shown in Fig.4 with details.

In case that output turns from PWM operation to constant low side driving, PWM high duty decreases by 12.5% of actual duty every term of PWM action according to VTH level, as shown in Fig.5.

In case that output turns from PWM operation to constant low side driving, PWM high duty decreases by 12.5% of actual duty every term of PWM action according to VTH level.
Similarly in case that output turns from constant low side driving to PWM operation, PWM high duty increases by 12.5% of actual duty every 12.5% of Soft switching term. However fixed regenerating term is inserted in 300 usec(typ) after phase switching, as shown in Fig.6.

**Fig.6**

- **Lock protection and Auto restart**
  In case that the motor is locked, this IC operates to protect the motor from the damage by constant large current.
  If the crossing of each hall signals isn’t detected within a specified period of time, motor driving is cut by turning off the output of high side driving.
  After a specified time from turning off the output, IC retries to operate in Start-up mode, as shown in Fig.7.
- Others
This IC has protective functions which are Under Voltage Lock Out (UVLO) and Over Voltage Protection (OVP).
The active level of UVLO is under 2.9V (typical) at VCC and the return level is over 3.1V (typical). If UVLO is active, Both of OUT1 and OUT2 are under sleep mode.
The active level of OVP is over 19.8V (typical) at VCC and the return level is under 17.8V (typical). If OVP is active, high side of OUT1 and OUT2 is into sleep but low side keeps on operating according to input signals.
Application Circuit Example

Fig. 8

*1  < Wiring of VCC and GND >
PGND (Frame) is connected to power MOSFETs and SGND is to internal circuits. Wiring of those should be separated each other to stabilize SGND by cutting out the influence of the switching noise of power FETs. In the event that external parts for IC are connected to GND, it should be done with SGND.
In addition, PGND (Frame) pins are effective for heat radiation. Therefore, the larger the wiring area of PGND is, the greater the effect is. Considering heat radiation along with the switching noise, the wiring of PGND should be widened as much as possible.
Similarly to PGND, the wiring of VCC should be widened and shortened for suppressing the noise.

*2  < Capacitor for power stabilization >

The capacitor for power stabilization should be enough value to ensure a stable operation. Of course, this capacitor must not be removed.
Under the condition that the value of coil inductance is larger or the value of coil resistance is smaller, the current ripple grows further. Under that condition, it should use the capacitor with larger value to absorb this current ripple. If cannot by capacitor, it must use power-clamp with zener diode.
This capacitor should be set as close to VCC pin and PGND pin as possible.

*3  < Capacitor for stabilization of REG output voltage >

REG output voltage is the regulated voltage as power supplier to inner control circuits. Therefore, it is necessary to stabilize by using a capacitor with enough value for preventing inner control circuits from false operation.
< Hall signal input >
To defend signals against the noise, it is necessary to wire as short as possible from hall sensor to each pin and to connect the capacitor between IN1 and IN2, as shown in Fig.1. Value from 1,000pF to 10,000pF is recommended for C5 in Fig.1. But its value should be selected in consideration with the actual motor action.

\[
\begin{align*}
    f_{CPWM} &= \frac{1}{2} \times \frac{I_{CPWM}}{C_2 \times (V_{CPH} - V_{CPL})} \\
    \text{In the case } C_2 &= 100[pF]; \\
    f_{CPWM=100\,pF} &= \frac{1}{2} \times \frac{25.0 \times 10^{-6}}{100 \times 10^{-12} \times (2.15 - 0.62)} = 81.70[kHz]
\end{align*}
\]

This is the result which is calculated by typical values of each electrical characteristic in this IC. Actually, there is variability which is defined by min/max in electrical characteristics. In addition, there may be some difference between calculated value and actual value because of a parasitic capacitance on the board and so on. Therefore, the value of C2 should be settled with actual operation, in view of those factors.

< Capacitor to adjust the PWM frequency >
The oscillation for PWM control is generated by connecting a capacitor between CPWM and GND. The frequency of this oscillation is calculated as below;

\[
V_{TH} = V_{REG} \times \left\{ \frac{R_2 + R_3}{R_1 + R_2 + R_3} - \frac{R_1 \times R_3}{(R_1 + R_2 + R_3) \times (R_1 + R_2)} \times \frac{D}{100} \right\}
\]

This calculation is justified by the condition that Rds of MN1 << R3. So, a large value of resistor should be selected to R3. But, too large value of R1 – R3 and R4 causes the instability because of the effect of input impedance at VTH pin.

The recommendation value of R1 – R3 and R4 is from 4.7k[ohm] to 47k[ohm].

The cut-off frequency fc by C3 and R4 is calculated as below;

\[
f_c = \frac{1}{2\pi \times C_3 \times R_4}
\]

The actual value of C3 or R4 is better to select more than 50 times the above calculation value to be flatten thoroughly. Furthermore, it is better to do it by the value of C3 because of the effect of input impedance at VTH pin.

< Input to VTH pin >
VTH pin needs to be input DC signal which is from 0V to VREG.

If the external control signal is the pulse type, it should be flatten by the filter and be shifted to suitable level, shown in Fig.1, to input to VTH pin.

In the case that the high duty of PWM signal input in Fig.1 is D [%], VTH input level flatten by the filter is calculated approximately as below;

\[
V_{TH} = V_{REG} \times \left\{ \frac{R_2 + R_3}{R_1 + R_2 + R_3} - \frac{R_1 \times R_3}{(R_1 + R_2 + R_3) \times (R_1 + R_2)} \times \frac{D}{100} \right\}
\]

< Adjustment of the minimum duty of PWM output >
As for the way of RMI input, the divided voltage of REG by resistors, as R6 and R7 shown in Fig.1, is recommended. In addition, it would be better to use a resistor which the value is from 4.7k[ohm] to 47k[ohm], in view of impedance at RMI pin.
If not use this pin, it should be shorted to VTH pin.

*8 < Adjustment of soft starting >
The time $T_{SFS}$ from IC booting to coming up to clamped duty is calculated approximately as below:

$$T_{SFS} = C_4 \times \left( V_{CPH} - V_{SFSCL} \right) / I_{SFS}$$

The value of $C_4$ should be selected in consideration with the start-up characteristic of motor and the time of lock detection.

*9 < RD output >
RD output is N-ch MOSFET with the opened drain. It is “Low level” in motor rotation and “High impedance” in lock detection. If not use, this pin would be better to open.

*10 < FG output >
FG output is N-ch MOSFET with the opened drain. It is the rotational signal made by the hall signal input. If not use, this pin would be better to open.