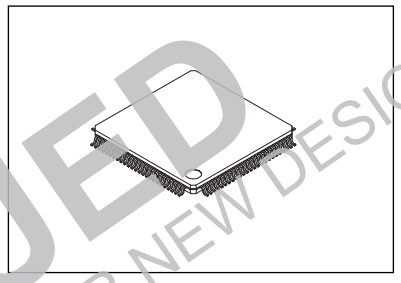
LC88FC3J0A

16-bit Microcontroller
640K-byte Flash ROM / 47.5K-byte RAM / 100-pin

ON Semiconductor®

www.onsemi.com

LC88FC3J0A is a 16-bit Microcontroller with 640K-byte Flash ROM/47.5K-byte RAM in 100-pin package. Main features are infrared remote controller receiver circuit (supports PPM and Manchester encoding), 16 channels of 12-bit resolution ADC, internal reset circuit, CRC circuit and etc. that are software friendly circuits and these peripheral circuit can contribute to less external components. Also, plenty of serial interface circuits (synchronous serial × 3, I^2C × 3, UART × 3) can communicate with other LSIs and are suitable for home appliances and white goods which need complicated control. For software development, there is our original software development environment and with On-Chip Debugging function, it is easy to debug with user's actual application.

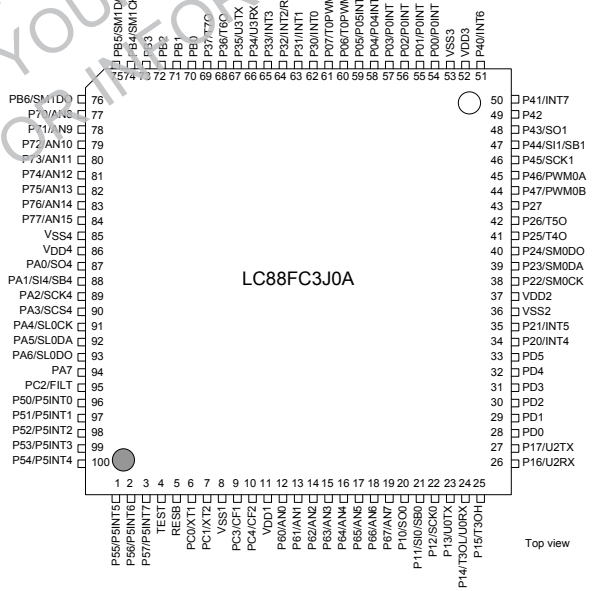


TQFP 100,14X14

Features
- 16-channel 12-bit resolution AD converter
- Infrared remote controller receiver circuit
- CRC operating circuit
- Internal Reset Function

Performance
- 100ns (10.0MHz) V_{DD}=2.7 to 3.6V Ta=–40°C to +85°C

Function Descriptions
- Xstromy16 CPU
  - 4G-byte address space
  - General-purpose registers: 16 bits × 16 registers
- Ports
  - I/O Ports 86
  - Power supply pins 8 (VSS1 to VSS4, VDD1 to VDD4)
- Timer
  - 16-bit timers × 8
  - Base timer serving as a time-of-day clock
- Serial interfaces
  - Synchronous SIO interfaces × 3 (with automatic transmission capability)
  - Single master I^2C/synchronous SIO interface × 2
  - Slave I^2C/synchronous SIO interface
  - Asynchronous SIO (UART) interfaces × 3
- Multifrequency 12-bit PWM modules
- 16-channel 12-bit resolution AD converter
- Watchdog timer
- Infrared remote controller receiver circuit
- CRC operating circuit
- Real time clock
- System clock frequency divider
- CF oscillator circuit, Crystal oscillator circuit, RC oscillator circuit
- 61-source 14-vector interrupt feature
- On-chip debugger function



Pin Assignment (Top view)

Application
- Home audio, White goods

* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION
See detailed ordering and shipping information on page 48 of this data sheet.

Function Details

■ Xstromy16 CPU
- 4G-byte address space
- General-purpose registers : 16 bits × 16 registers

■ Flash ROM
- 655360 × 8 bits
- Programming voltage level : 2.7 to 3.6V.
- Block-erasable in 2K byte units.
- Data written in 2-byte units.

■ RAM
- 48640 × 8 bits

■ Minimum instruction cycle time (tCYC)
- 100 ns (10 MHz), V_{DD} = 2.7 to 3.6V

■ Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units : 86 (P0n, P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAn, PB0 to PB6, PC2, PD0 to PD5)
- Oscillation/normal withstand voltage I/O ports : 4 (PC0, PC1, PC3, PC4)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Power pins : 8 (V_{SS}1 to 4, V_{DD}1 to 4)

■ Timers
- Timer 0 : 16-bit timer that supports PWM/toggle outputs
  <1> 5-bit prescaler
  <2> 8-bit PWM × 2, 8-bit timer + 8-bit PWM mode selectable
  <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator.
- Timer 1 : 16-bit timer with capture registers
  <1> 5-bit prescaler
  <2> May be divided into 2 channels of 8-bit timer
  <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2 : 16-bit timer with capture registers
  <1> 4-bit prescaler
  <2> May be divided into 2 channels of 8-bit timer
  <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3 : 16-bit timer that supports PWM/toggle outputs
  <1> 8-bit prescaler
  <2> 8-bit timer× 2ch or 8-bit timer+8-bit PWM mode selectable
  <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4 : 16-bit timer that supports toggle outputs
  <1> Clock source selectable from system clock and prescaler 0
- Timer 5 : 16-bit timer that supports toggle output
  <1> Clock source selectable from system clock and prescaler 0
- Timer 6 : 16-bit timer that supports toggle outputs
  <1> Clock source selectable from system clock and prescaler 1
- Timer 7 : 16-bit timer that supports toggle output
  <1> Clock source selectable from system clock and prescaler 1
  *Prescaler 0 and 1 are consisted of 4bits and can choose their clock source from OSC0 or OSC1.
- Base timer
  <1> Clock may be selected from OSC0 (32.768 kHz crystal oscillator) and frequency-divided output of system clock.
  <2> Interrupts can be generated in 7 timing schemes.

■ Real time clock

<1> Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leapyear calculation function.
<2> Consisted of Indipendent second-minuit-hour-day-month-yeare-century counters.

■ Serial interfaces

- SIO0 : 8-bit synchronous SIO
  - <1> LSB first/MSB first mode selectable
  - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
  - <6> Wakeup function
- SIO1 : 8-bit synchronous SIO
  - <1> LSB first/MSB first mode selectable
  - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
  - <6> Wakeup function
- SIO4 : 8-bit synchronous SIO
  - <1> LSB first/MSB first mode selectable
  - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
  - <6> Wakeup function
- SMIIC0 : Single master I^2C/8-bit synchronous SIO
  - Mode 0 : Single-master mode communication
  - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
- SMIIC1 : Single master I^2C/8-bit synchronous SIO
  - Mode 0 : Single-master mode communication
  - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
- SLIIC0 : Slave I^2C/8-bit synchronous SIO
  - Mode 0 : I^2C slave mode communication
  - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
  - Note: usable only with the external clock source

- UART0
  - <1> Data length : 8 bits (LSB first)
  - <2> Start bits : 1 bit
  - <3> Stop bits : 1 bit
  - <4> Parity bits : None/even parity/odd parity
  - <5> Transfer rate : 4/8 cycle
  - <6> Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer4 cycle.
  - <7> Full duplex communication

  Note : The "cycle" refers to one period of the baudrate clock source.
- UART2
  - <1> Data length : 8 bits (LSB first)
  - <2> Start bits : 1 bit
  - <3> Stop bits : 1/2 bit
  - <4> Parity bits : None/even parity/odd parity
  - <5> Transfer rate : 8 to 4096 cycle
  - <6> Baudrate source clock: System clock/OSC0/OSC1/P26 input signal
  - <7> Wakeup function
  - <8> Full duplex communication

  Note : The "cycle" refers to one period of the baudrate clock source.
- UART3
  - <1> Data length : 8 bits (LSB first)
  - <2> Start bits : 1 bit
  - <3> Stop bits : 1/2 bit
  - <4> Parity bits : None/even parity/odd parity
  - <5> Transfer rate : 8 to 4096 cycle
  - <6> Baudrate source clock: System clock/OSC0/OSC1/P36 input signal
  - <7> Wakeup function
  - <8> Full duplex communication

  Note : The "cycle" refers to one period of the baudrate clock source.

■ AD converter
- <1> 12/8 bits resolution selectable
- <2> Analog input: 16 channels
- <3> Comparator mode

■ PWM
- PWM0 : Multifrequency 12-bit PWM × 2 channels (PWM0A and PWM0B)
  - <1> 2-channel pairs controlled independently of one another
  - <2> Clock source selectable from system clock or OSC1
  - <3> 8-bit prescaler: TPWMR0= (prescaler value + 1) × clock period
  - <4> 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
  - <5> Fundamental wave PWM mode
    - Fundamental wave period : 16 TPWMR0 to 256 TPWMR0
    - High pulse width : 0 to (Fundamental wave period - TPWMR0)
  - <6> Fundamental wave + additional pulse mode
    - Fundamental wave period : 16 TPWMR0 to 256 TPWMR0
    - Overall period : Fundamental wave period × 16
    - High pulse width : 0 to (Fundamental wave period - TPWMR0)

■ CRC operating circuit

■ Watchdog timer
- <1> Driven by the base timer + internal watchdog timer dedicated counter
- <2> Interrupt or reset mode selectable

■ Infrared Remote Controller Receiver Circuit

1) Noise rejection function (noise filter time constant: Approx. 120μs when the 32.768kHz crystal oscillator is selected as the reference clock source)
2) Supports data encording systems such as PPM (Pulse Position Modulation) and Manchester encording
3) X'tal HOLD mode release function

■ Internal Reset Function

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level can be selected by option configuration.

■ Interrupts (peripheral function)

- 61 sources (33 modules), 14 vector addresses
  <1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  <2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Module
1	08000H	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer 0 (2)
4	0800CH	INT0 (1)
5	08014H	INT1 (1)
6	08018H	INT2 (1) / timer 1 (2) / UART2 (4)
7	0801CH	INT3 (1) / timer 2 (4) / SMIIC0 (1) / SLIIC1 (1)
8	08020H	INT4 (1) / timer 3 (2) / Infared remote control receiver(4)
9	08024H	INT5 (1) / timer 4 (1) / SIO1 (2)
10	0802CH	PWM0 (1) / SMIIC1(1)
11	08030H	ADC (1) / timer 5 (1) / SIO4(2)
12	08034H	INT6 (1) / timer 6 (1) / UART 3 (4)
13	08038H	INT7 (1) / SIO0 (2) / SIO0(2)
14	0803CH	Port 0 (3) / Port 5 (8) / RTC (1) / CRC (1)

- 3 priority levels selectable
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

■ Subroutine stack : RAM area

- Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
- Subroutine calls that do not automatically save PSW: 4 bytes

■ Multiplication/division instructions

- 16 bits × 16 bits (4 tCYC execution time)
- 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
- 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

■ Oscillator circuits

- RC oscillator circuit (internal) : For system clock
- CF oscillator circuit (built-in Rf circuit) : For system clock(OSC1)
- Crystal oscillator circuit (built-in Rf circuit) : For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal) : For system clock (In the case of exception processing)
- VCO oscillator circuit : For timer3, 4, 5, 6, 7 clock

■ System clock divider function

- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

■ Standby function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
  - <1> Oscillation is not stopped automatically.
  - <2> Released by a system reset or occurrence of an interrupt.
- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
  - <1> OSC1, RC, and OSC0 oscillations automatically stop.
  - <2> There are six ways of releasing the HOLD mode:
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established at port 5
    - (5) Having an interrupt established at SIO0, SIO1 or SIO4
    - (6) Having an interrupt established at UART2 or UART3
- HOLDX mode : Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
  - <1> OSC1 and RC oscillations automatically stop.
  - <2> OSC0 maintains the state that is established when the HOLDX mode is entered.
  - <3> There are nine ways of releasing the HOLDX mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6,and INT7 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established at port 5
    - (5) Having an interrupt source established at the base timer circuit
    - (6) Having an interrupt established at SIO0, SIO1 or SIO4
    - (7) Having an interrupt established at UART2 or UATR3
    - (8) Having an interrupt established at Infared remote control receiver.
    - (9) Having an interrupt source established at the real time clock circuit

■ On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

■ Package form

- TQFP100, 14 × 14 : Pb-Free and Halogen Free type

■ Development tools

- On-chip debugger : EOCUIF1 or EOCUIF2 + LC88FC3J0A

■ Programming board

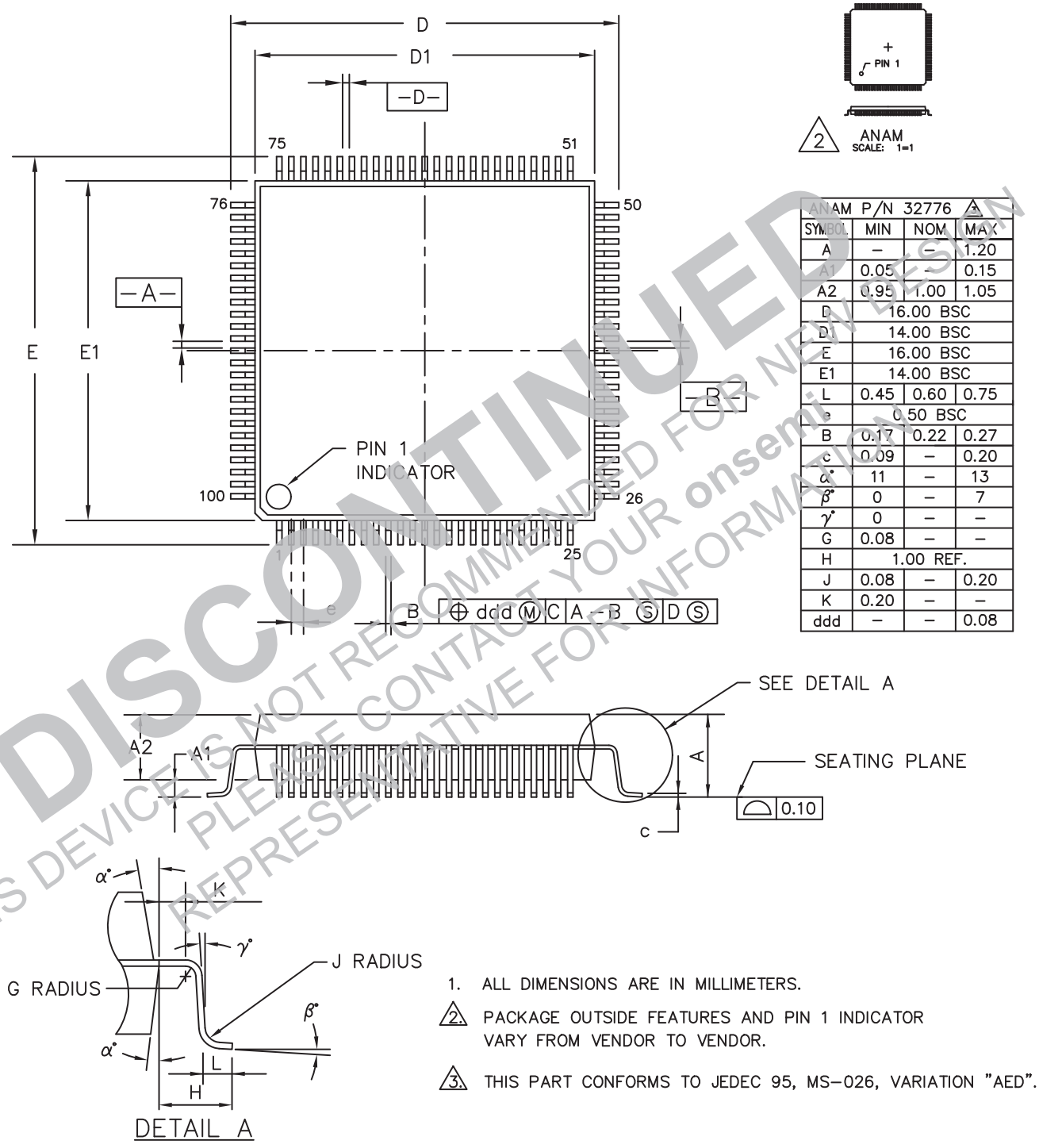
Package	Programming Board
TQFP 100, 14 × 14	W88F52TQ

■ Flash ROM Programmer

Maker		Model	Supported Version	Device
ON Semiconductor	Single / Gang programmer	SKK Type C (SanyoFWS)	Application Version After 1.08A Chip Data Version After 2.51	LC88FC3x0
	On-board Single programmer	FWS-X16DI Type 3	Application Version After 1.08A Chip Data Version After 2.51	LC88FC3x0

Package Dimensions
unit : mm

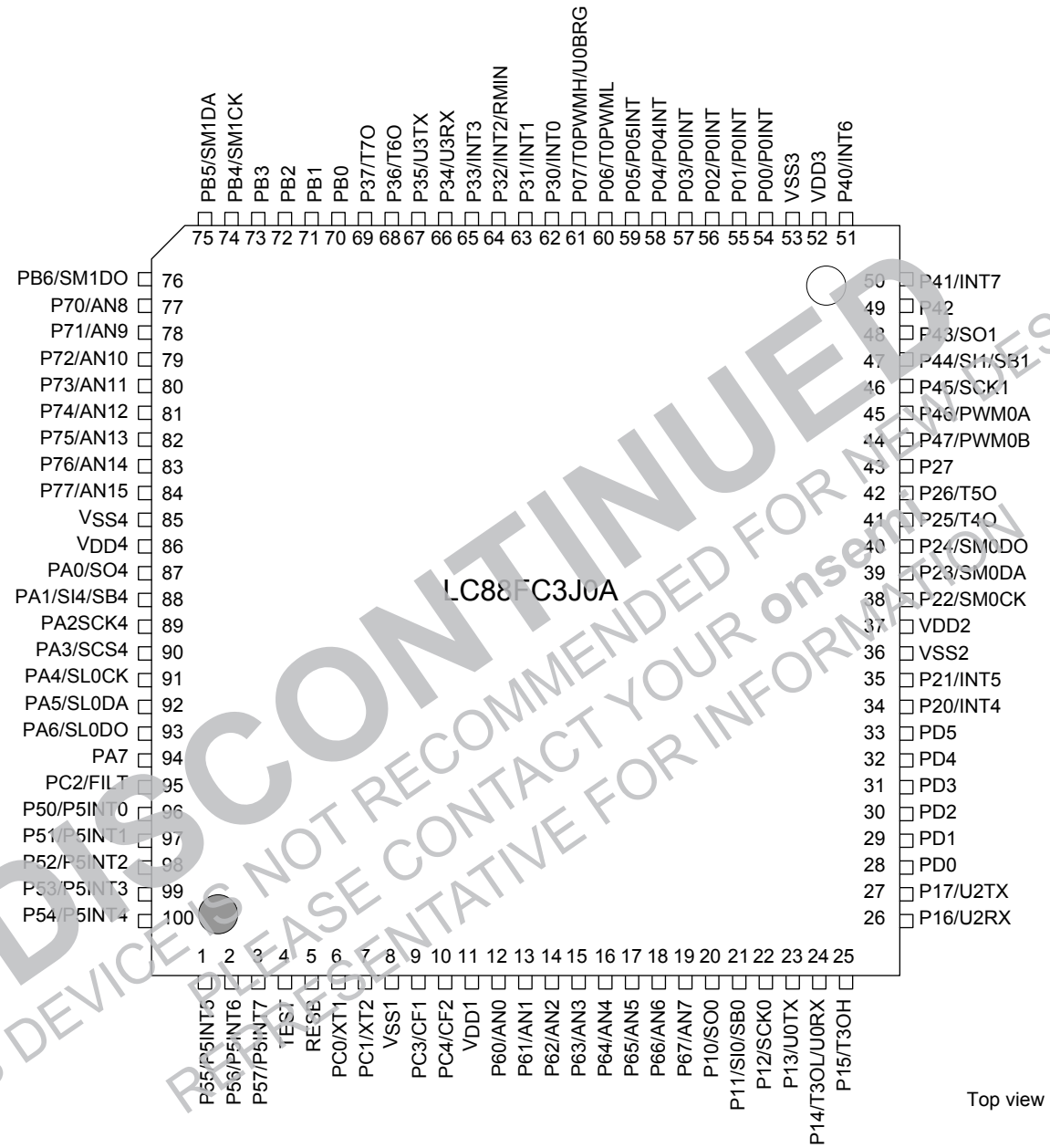
TQFP 100, 14x14
CASE 932AN-01
ISSUE O



ANAM P/N 32776 ⚠2			
SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.95	1.00	1.05
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
B	0.17	0.22	0.27
c	0.09	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–
G	0.08	–	–
H	1.00 REF.		
J	0.08	–	0.20
K	0.20	–	–
ddd	–	–	0.08

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PACKAGE OUTSIDE FEATURES AND PIN 1 INDICATOR VARY FROM VENDOR TO VENDOR.
3. THIS PART CONFORMS TO JEDEC 95, MS−026, VARIATION "AED".

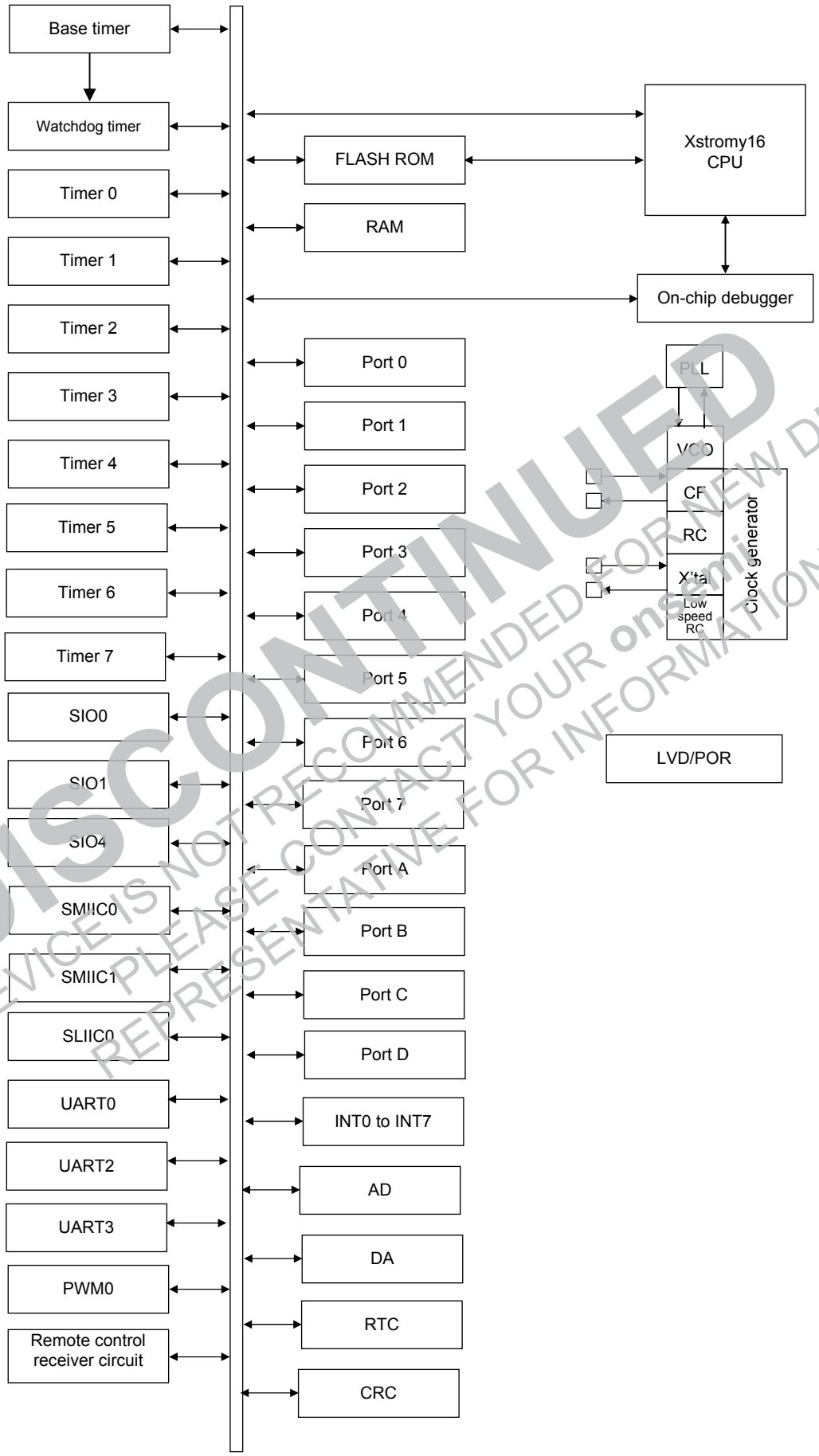
Pin Assignment



Top view

TQFP100,14×14 (Pb-Free and Halogen Free type)

System Block Diagram



Pin Description

Pin Name	I/O	Description
VSS1, VSS2, VSS3, VSS4	–	– power sources
VDD1, VDD2, VDD3, VDD4	–	+ power sources
Port 0 P00 to P07	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・HOLD release input (P00 to P03, P04, P05) ・Port 0 interrupt input (P00 to P03, P04, P05) ・Pin functions P06 : Timer 0L output P07 : Timer 0L output/UART0 clock input
Port 1 P10 to P17	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Pin functions P10 : SIO0 data output P11 : SIO0 data input/pulse input/output P12 : SIO0 clock input/output P13 : UART0 transmit P14 : Timer 3L output/UART0 receive P15 : Timer 3H output P16 : UART2 receive P17 : UART2 transmit
Port 2 P20 to P27	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Pin functions P20 : INT4 input/HOLD release input/timer 3 event input/ timer 2L capture input/timer 2H capture input P21 : INT5 input/HOLD release input/timer 3 event input/ timer 2L capture input/timer 2H capture input P22 : SMIIC0 clock input/output P23 : SMIIC0 bus input/output/data input P24 : SMIIC0 data output (used in 3-wire SIO mode) P25 : Timer 4 output P26 : Timer 5 output Interrupt acknowledge type INT4, INT5 : H level, L level, H edge, L edge, both edges

Continued on next page.

Continued from preceding page.

Pin Name	I/O	Description
Port 3 P30 to P37	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Pin functions P30 : INT0 input/HOLD release/timer 2L capture input P31 : INT1 input/HOLD release/timer 2H capture input P32 : INT2 input/HOLD release/timer 2 event input/timer 2L capture input/ Infrared Remote Controller Receiver input P33 : INT3 input/HOLD release/timer 2 event input/timer 2H capture input P34 : UART3 receive P35 : UART3 transmit P36 : Timer 6 output P37 : Timer 7 output Interrupt acknowledge type INT0 to INT3 : H level, L level, H edge, L edge, both edges
Port 4 P40 to P47	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Pin functions P40 : INT6 input/HOLD release input P41 : INT7 input/HOLD release input P43 : SIO1 data output P44 : SIO1 data input/bus input/output P45 : SIO1 clock input/output P46 : PWM0A output P47 : PWM0Boutput Interrupt acknowledge type INT6, INT7 : H level, L level, H edge, L edge, both edges
Port 5 P50 to P57	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・HOLD release input ・Port 0 interrupt input
Port 6 P60 to P67	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Pin functions AN0 (P60) to AN7 (P67) : AD converter input port
Port 7 P70 to P77	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Pin functions AN8 (P70) to AN15 (P77) : AD converter input port

Continued on next page.

Continued from preceding page.

Pin Name	I/O	Description
Port A PA0 to PA7	I/O	・8-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Multiplexed pin functions PA0 : SIO4 data output PA1 : SIO4 data input/pulse input/output PA2 : SIO4 clock input/output PA3 : SIO4 chip select input PA4 : SLIIC0 clock input PA5 : SLIIC0 bus input/output/data input PA6 : SLIIC0 data output (used in 3-wire SIO mode)
Port B PB0 to PB6	I/o	・7-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units ・Multiplexed pin functions PB4 : SMIIC1 clock input/output PB5 : SMIIC1 bus input/output/data input PB6 : SMIIC1 data output (used in 3-wire SIO mode)
Port C PC0 to PC4	I/O	・5-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units (PC2) ・Pin functions PC0 : 32.768 kHz crystal oscillator input PC1 : 32.768 kHz crystal oscillator output PC2 : FILT of VCO PC3 : Ceramic oscillator input PC4 : Ceramic oscillator output/VCO output
Port D PD0 to PD5	I/O	・6-bit I/O port ・I/O specifiable in 1-bit units ・Pull-up resistors can be turned on and off in 1 bit units
TEST	I/O	・TEST pin ・Used to communicate with on-chip debugger. ・Connects an external 100 kΩ pull-down resistor.
RESB	I/O	Reset pin

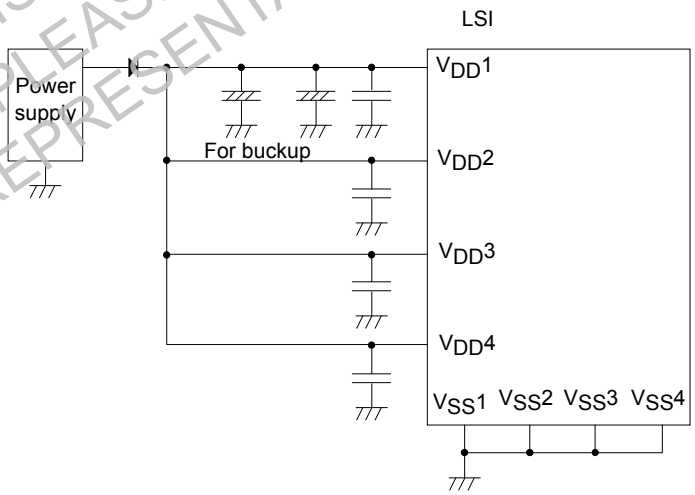
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

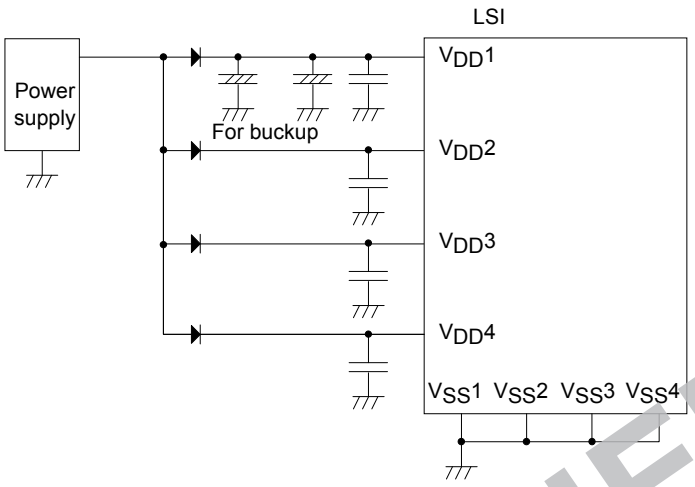
Port Name	Option Selected in Units of	Output Type	Pull-up Resistor
P00 to P07	1 bit	CMOS	Programmable
P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 PA0 to PA7 PB0 to PB6		Able to program special functions'output type from CMOS output or Nch-opendrain	
P60 to P67 P70 to p77 PD0 to PD5 PC2		CMOS	
PC0	–	N-channel open drain (32.768 kHz crystal oscillator input)	None
PC1	–	Nch-open drain (32.768k kHz crystal oscillator output)	None
PC3	–	CMOS (ceramic oscillator input)	None
PC4	–	CMOS (ceramic oscillator output)	None

* Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time.
Be sure to electrically short the VSS1, VSS2, VSS3 and VSS4 pins.

Example 1 : When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2 : When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



■ **Absolute Maximum Ratings** at Ta=25°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter		Symbol	Applicable Pin /Remarks	Conditions		Specification			
					V_{DD} [V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, $V_{DD}4$	$V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$		–0.3		+4.6	V
Input voltage		VI (1)	RESB			–0.3		V_{DD} +0.3	V
Input/output voltage		VIO (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D			–0.3		VDD +0.3	V
High level output current	Peak output current	IOPH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 7, A, D PB2 to PB6	CMOS output selected Per applicable pin		–7.5			mA
		IOPH (2)	P46, P47 PB0, PB1	Per applicable pin		–12.5			mA
		IOPH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		–4.5			mA
	Average output current (Note 1-1)	IOMH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 5, 6, 7, A PB2 to PB6 Ports D	CMOS output selected Per applicable pin		–5			mA
		IOMH (2)	P46, P47 PB0, PB1	Per applicable pin		–10			mA
		IOMH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		–3			mA
	Total output current	ΣIOAH (1)	Pprts 5 PC0 to PC4	Total of currents at applicable pins		–10			mA
		ΣIOAH (2)	Port 6	Total of currents at applicable pins		–10			mA
		ΣIOAH (3)	Port 5, 6 PC0 to PC4	Total of currents at applicable pins		–20			mA
		ΣIOAH (4)	Ports 1,D1 P20 to P21	Total of currents at applicable pins		–20			mA
		ΣIOAH (5)	P22 to P27	Total of currents at applicable pins		–20			mA
		ΣIOAH (6)	Ports 1, 2, D	Total of currents at applicable pins		–40			mA
		ΣIOAH (7)	Ports 4	Total of currents at applicable pins		–20			mA
		ΣIOAH (8)	Ports 0, 3	Total of currents at applicable pins		–20			mA
		ΣIOAH (9)	Ports 0, 3, 4	Total of currents at applicable pins		–40			mA
		ΣIOAH (10)	Ports B, 7	Total of currents at applicable pins		–20			mA
		ΣIOAH (11)	Ports A	Total of currents at applicable pins		–20			mA
		ΣIOAH (12)	Ports 7, A, B	Total of currents at applicable pins		–40			mA

Note 1-1 : Average output current refers to the average of output currents measured for a period of 100 ms.

Continued on next page.

Continued from preceding page.

Parameter		Symbol	Applicable Pin /Remarks	Conditions		Specification			
					V_{DD} [V]	min	typ	max	unit
Low level output current	Peak output current	IOPL (1)	Ports 0, 1, 3, 4 Ports 7, D P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6,	Per applicable pin				15	mA
		IOPL (2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin				20	
		IOPL (3)	Ports 5, 6 PC0 to PC4	Per applicable pin				7.5	
	Average output current (Note 1-1)	IOML (1)	Ports 0, 1, 3, 4 Ports 7, D P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6, PB7	Per applicable pin				12.5	
		IOML (2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin				15	
		IOML (3)	Ports 5, 6 PC0 to PC4	Per applicable pin				5	
	Total output current	ΣIOAL (1)	Ports 5 PC0 to PC2	Total of currents at applicable pins				10	
		ΣIOAL (2)	Port 6 PC3 to PC4	Total of currents at applicable pins				10	
		ΣIOAL (3)	Port 5, 6 PC0 to PC4	Total of currents at applicable pins				20	
		ΣIOAL (4)	Ports 1, D P20, P21	Total of currents at applicable pins				35	
		ΣIOAL (5)	P22 to P27	Total of currents at applicable pins				35	
		ΣIOAL (6)	Ports 1, 2, D	Total of currents at applicable pins				70	
		ΣIOAL (7)	Port 4	Total of currents at applicable pins				35	
		ΣIOAL (8)	Port 0, 3	Total of currents at applicable pins				35	
		ΣIOAL (9)	Port 0, 3, 4	Total of currents at applicable pins				70	
		ΣIOAL (10)	Port 7, B	Total of currents at applicable pins				35	
		ΣIOAL (11)	Port A	Total of currents at applicable pins				35	
		ΣIOAL (12)	Port 7, A, B	Total of currents at applicable pins				70	
Allowable power dissipation		Pd max	TQFP100	Ta=–40 to +85°C Package with thermal resistance bord (Note 1-2)				460	mW
Operating ambient temperature		Topr				–40		+85	°C
Storage ambient temperature		Tstg				–55		+125	

Note 1-1 : Average output current refers to the average of output currents measured for a period of 100 ms.
Note 1-2 : SEMI standerds thermal resistance board (size : 76.1× 114.3 × 1.6 tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ **Allowable Operating Conditions** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Operating supply voltage	V_{DD} (1)	$V_{DD}1=V_{DD}2=V_{DD}3$	0.098µs ≤ tCYC ≤ 66µs		2.7		3.6	V
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3$	RAM and register contents sustained in HOLD mode		2.0		3.6	
High level input voltage	VIH (1)	Ports 0, 1, 2, 3, 4 Port 5, A, B		2.7 to 3.6	$0.3V_{DD}$ +0.7		V_{DD}	
	VIH (2)	Ports 6, 7, D,PC2		2.7 to 3.6	$0.3V_{DD}$ +0.7		V_{DD}	
	VIH (3)	RESB PC0, PC1, PC3, PC4		2.7 to 3.6	$0.75V_{DD}$		V_{DD}	
	VIH (4)	P22, P23, PA4, PA5, PB4, PB5 I2C side		2.7 to 3.6	$0.7V_{DD}$		V_{DD}	
Low level input voltage	VIL (1)	When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=0 Ports 0, 6, 7, D, PC2		2.7 to 3.6	V_{SS}		$0.2V_{DD}$	
	VIL (2)	When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=1		2.7 to 3.6	V_{SS}		$0.2V_{DD}$	
	VIL (3)	CF1, RESB PC0, PC1,PC3, PC4		2.7 to 3.6	V_{SS}		$0.25V_{DD}$	
	VIL (4)	P22, P23, PA4, PA5, PB4, PB5 I2C side		2.7 to 3.6	V_{SS}		$0.3V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC			2.7 to 3.6	0.098		66	µs
External system clock frequency	FEXCF (1)	CF1	・CF2 pin open ・System clock frequency division ratio = 1/1 ・External system clock DUTY50±5%	2.7 to 3.6	0.1		10	MHz
			・CF2 pin open ・System clock frequency division ratio = 1/2	2.7 to 3.6	0.2		20	

Note 2-1 : Relationship between tCYC and oscillation frequency is 1/FmCF when frequency division ratio is 1/1 and 2/FmCF when the ratio is 1/2.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Oscillation frequency range (Note 2-2)	FmCF	PC3(CF1), PC4(CF2)	10 MHz ceramic oscillator mode See Fig. 1.	2.7 to 3.6		10		MHz
	FmRC		Internal RC oscillation	2.7 to 3.6	0.5	1.0	2.0	
	FmSLRC		Internal low-speed RC oscillation	2.7 to 3.6	18	30	45	kHz
	FsX'tal	XT1, XT2	32.768 kHz crystal oscillator mode See Fig. 2.	2.7 to 3.6		32.768		
	FmVCO(1)		VCO oscillator When setting FRQSEL=0 See Fig. 9.	2.7 to 3.6	12		28	MHz
	FmVCO(2)		VCO oscillator When setting FRQSEL=1 See Fig. 9.	2.7 to 3.6	38		70	
	FmVCO(5)		VCO oscillator	2.7 to 3.6		Note 2-3		

Note 2-2 : See Tables 1 and 2 for oscillator constant values.
Note 2-3 : VCO oscillation frequency = Ceramic oscillator frequency × Setting point of SELREF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

■ **Electrical Characteristics** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
High level input current	IIH (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B,C, D RESB	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (including output Tr. off leakage current)	2.7 to 3.6			1	μA
Low level input current	IIL (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (including output Tr. off leakage current)	2.7 to 3.6	–1			
High level output voltage	VOH (1)	Ports 0, 1, 2, 3 Ports 5, 6	IOH=–0.4mA	3.0 to 3.6	V_{DD}–0.4			V
	VOH (2)	Ports A, D, PC2 P40 to P45 PB2 to PB6	IOH=–0.2mA	2.7 to 3.6	V_{DD}–0.4			
	VOH (3)	P46, P47 PB0, PB1	IOH=–1.6mA	3.0 to 3.6	V_{DD}–0.4			
	VOH (4)		IOH=–1.0mA	2.7 to 3.6	V_{DD}–0.4			
	VOH (5)	PC0, PC1, PC3, PC4,	IOH=–1.0mA	3.0 to 3.6	V_{DD}–0.4			
	VOH (6)		IOH=–0.4mA	2.7 to 3.6	V_{DD}–0.4			
Low level output voltage	VOL (1)	Ports 0, 1, 3 , 4 Ports 5, 6, 7, D PC2 P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to PB3, PB6	IOL=1.6mA	3.0 to 3.6			0.4	
	VOL (2)		IOL=1.0mA	2.7 to 3.6			0.4	
	VOL (3)	P22, P23, PA4, PA5, PB4, PB5	IOL=3.0mA	3.0 to 3.6			0.4	
	VOL (4)		IOL=1.3mA	2.7 to 3.6			0.4	
	VOL (5)	PC0, PC1, PC3, PC4,	IOL=1.0mA	3.0 to 3.6			0.4	
	VOL (6)		IOL=0.4mA	2.7 to 3.6			0.4	
Pull-up resistor	Rpu (1)	Ports 0, 1, 2, 3 Ports 4, 5, 6, 7	VOH=0.9V_{DD}	3.0 to 3.6	15	35	80	kΩ
	Rpu (2)	Ports A, B, D, PC2 RESB		2.7 to 3.6	15	35	100	
Hysteresis voltage	VHYS	When ports 1, 2, 3, 4, A, B PnFSAn=1		2.7 to 3.6		0.1V_{DD}		V
Pin capacitance	CP	All pins	Pins other than that under test $V_{IN}=V_{SS}$ f=1 MHz Ta=25°C	2.7 to 3.6		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

■ **Serial I/O Characteristics** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (1)	SCK0 (P12)	・See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (1)				2			
		High level pulse width	tSCKH (1)				2			
			tSCKHA (1)		・Automatic communication mode ・See Fig. 6.		6			
			tSCKHBSY (1a)		・Automatic communication mode ・See Fig. 6.		23			
			tSCKHBSY (1b)		・Mode other than automatic communication mode ・See Fig. 6.		4			
	Output clock	Period	tSCK (2)	SCK0 (P12)	・CMOS output selected ・See Fig. 6.		4			
		Low level pulse width	tSCKL (2)				1/2			tSCK
		High level pulse width	tSCKH (2)				1/2			
			tSCKHA (2)		・Automatic communication mode ・CMOS output selected ・See Fig. 6.	2.7 to 3.6	6			tCYC
			tSCKHBSY (2a)		・Automatic communication mode ・CMOS output selected ・See Fig. 6.		4		23	
			tSCKHBSY (2b)		・Mode other than automatic communication mode ・See Fig. 6.		4			
Serial input	Data setup time		tsDI (1)	SI0 (P11), SB0 (P11)	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (1)				0.03			
Serial output	Input clock	Output delay time	tdD0 (1)	SO0 (P10), SB0 (P11)	・(Note 4-1-2)	2.7 to 3.6			1tCYC +0.05	
	Output clock		tdDO (2)		・(Note 4-1-2)				1tCYC +0.05	

Note 4-1-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (3)	SCK0 (P12)	・See Fig. 6.	2.7 to 3.6	2			tCYC
		Low level pulse width	tSCKL (3)				1			
		High level pulse width	tSCKH (3)				1			
			tSCKHBSY (3)				2			
Serial input	Data setup time		tsDI (2)	SI0 (P11), SB0 (P11)	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			μs
	Data hold time		thDI (2)				0.03			
Serial output	Input clock	Output delay time	tdD0 (3)	SO0 (P10), SB0 (P11)	・(Note 4-2-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-2-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (4)	SCK1 (P45)	・See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (4)				2			
		High level pulse width	tSCKH (4)				2			
			tSCKHA (4)		・Automatic communication mode ・See Fig. 6.		6			
			tSCKHBSY (4a)		・Automatic communication mode ・See Fig. 6.		23			
			tSCKHBSY (4b)		・Mode other than automatic communication mode ・See Fig. 6.		4			
	Output clock	Period	tSCK (5)	SCK1 (P45)	・CMOS output selected ・See Fig. 6.		4			tSCK
		Low level pulse width	tSCKL (5)				1/2			
		High level pulse width	tSCKH (5)				1/2			
			tSCKHA (5)		・Automatic communication mode ・CMOS output selected ・See Fig. 6.	2.7 to 3.6	6			tCYC
			tSCKHBSY (5a)		・Automatic communication mode ・CMOS output selected ・See Fig. 6.		4		23	
			tSCKHBSY (5b)		・Mode other than automatic communication mode ・See Fig. 6.		4			
Serial input	Data setup time		tsDI (3)	SI1 (P44), SB1 (P44)	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (3)				0.03			
Serial output	Input clock	Output delay time	tdDO (4)	SO1 (P43), SB1 (P44)	・(Note 4-3-2)	2.7 to 3.6			1tCYC +0.05	
	Output clock		tdDO (5)		・(Note 4-3-2)				1tCYC +0.05	

Note 4-3-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-3-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (6)	SCK1 (P45)	・See Fig. 6.	2.7 to 3.6	2			tCYC
		Low level pulse width	tSCKL (6)				1			
		High level pulse width	tSCKH (6)				1			
			tSCKHBSY (6)				2			
Serial input	Data setup time		tsDI (4)	SI1 (P44), SB1 (P44)	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (4)				0.03			
Serial output	Input clock	Output delay time	tdD0 (6)	SO1 (P43), SB1 (P44)	・(Note 4-4-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-4-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-4-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO4 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-5-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (7)	SCK4 (PA2)	・See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (7)				2			
		High level pulse width	tSCKH (7)				2			
			tSCKHA (7)		・Automatic communication mode ・See Fig. 6.		6			
			tSCKHBSY (7a)		・Automatic communication mode ・See Fig. 6.		23			
			tSCKHBSY (7b)		・Mode other than automatic communication mode ・See Fig. 6.		4			
	Output clock	Period	tSCK (8)	SCK4 (PA2)	・CMOS output selected ・See Fig. 6.	2.7 to 3.6	4			tSCK
		Low level pulse width	tSCKL (8)				1/2			
		High level pulse width	tSCKH (8)				1/2			
			tSCKHA (8)		・Automatic communication mode ・CMOS output selected ・See Fig. 6.		6			tCYC
			tSCKHBSY (8a)		・Automatic communication mode ・CMOS output selected ・See Fig. 6.		4		23	
			tSCKHBSY (8b)		・Mode other than automatic communication mode ・See Fig. 6.		4			
Serial input	Data setup time		tsDI (5)	SI4 (PA1), SB4 (PA1)	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (5)				0.03			
Serial output	Output delay time	Input clock	tdDO (7)	SO4 (PA0), SB14(PA1)	・(Note 4-5-2)	2.7 to 3.6			1tCYC +0.05	
		Output clock	tdDO (8)		・(Note 4-5-2)				1tCYC +0.05	

Note 4-5-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-5-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO4 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-6-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (9)	SCK4 (P45)	・See Fig. 6.	2.7 to 3.6	2			tCYC
		Low level pulse width	tSCKL (9)				1			
		High level pulse width	tSCKH (9)				1			
			tSCKHBSY (9)				2			
Serial input	Data setup time		tsDI (6)	SI4 (P44), SB4 (P44)	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (6)				0.03			
Serial output	Input clock	Output delay time	tdD0 (9)	SO4 (P43), SB4(P44)	・(Note 4-6-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-6-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-6-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SMIIC0 Simple SIO Mode Input/Output Characteristics (Note 4-7-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (10)	SM0CK (P22)	See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (10)				2			
		High level pulse width	tSCKH (10)				2			
	Output clock	Period	tSCK (11)	SM0CK (P22)	・CMOS output selected ・See Fig. 6.	2.7 to 3.6	4			tSCK
		Low level pulse width	tSCKL (11)				1/2			
		High level pulse width	tSCKH (11)				1/2			
Serial input	Data setup time		tsDI (7)	SM0DA (P23),	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (7)				0.03			
Serial output	Output delay time		tdD0 (10)	SM0DO (P24), SM0DA (P23)	・Specified with respect to falling edge of SIOCLK ・Specified as interval up to time when output state starts changing. ・See Fig. 6.	2.7 to 3.6			1tCYC +0.05	

Note 4-7-1 : These specifications are theoretical values. Add margin depending on its use.

SMIIC0 I²C Mode Input/Output Characteristics (Note 4-8-1) (Note 4-8-2) (Note 4-8-4)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK (P22)	・See Fig. 8.	2.7 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK (P22)	・Specified as interval up to time when output state starts changing.	2.7 to 3.6	10			tSCL
		Low level pulse width	tSCLLx				1/2			
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6			1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6	2.5			Tfilt
	Output		tBUFx	SM0CK (P22) SM0DA (P23)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		5.5			µs
					・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK (P22) SM0DA (P23)	・When SMIIC register control bit I2CSHDS=0 ・See Fig. 8.	2.7 to 3.6	2.0			Tfilt
					・When SMIIC register control bit I2CSHDS=1 ・See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK (P22) SM0DA (P23)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		4.1			µs
					・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6	1.0			Tfilt
	Output		tSU;STAx	SM0CK (P22) SM0DA (P23)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		5.5			µs
					・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.6			

Parameter		Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	typ	max	Unit
Stop condition setup time	Input	tSU;STO	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6	1.0			Tfilt
	Output	tSU;STOx	SM0CK (P22) SM0DA (P23)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		4.9			µs
				・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.1			
Data hold time	Input	tHD;DAT	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6	0			Tfilt
	Output	tHD;DATx	SM0CK (P22) SM0DA (P23)	・Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU;DAT	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6	1			Tfilt
	Output	tSU;DATx	SM0CK (P22) SM0DA (P23)	・Specified as interval up to time when output state starts changing.		tSCL-1.5Tfilt			
SM0CK and SM0DA pins fall time	Input	tF	SM0CK (P22) SM0DA (P23)	・See Fig. 8.	2.7 to 3.6			300	ns
	Output	tF	SM0CK (P22) SM0DA (P23)	・When SMIIC register control bits PSLW=1, P5V=1	3	20+0.1Cb (Note 4-8-3)		250	
				・SM0CK, SM0DA port output FAST mode ・Cb ≤ 100pF	3.0 to 3.6			100	

Note 4-8-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-8-2 : The value of Tfilt is determined by the values of the register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range :

250 ns ≥ Tfilt > 140 ns

Note 4-8-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 100 pF

Note 4-8-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows :

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 1

SCL frequency setting ≤ 100 kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows :

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400 kHz

SMIIC1 Simple SIO Mode Input/Output Characteristics (Note 4-9-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (12)	SM0CK (PB4)	See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (12)				2			
		High level pulse width	tSCKH (12)				2			
	Output clock	Period	tSCK (13)	SM0CK (PB4)	・CMOS output selected ・See Fig. 6.	2.7 to 3.6	4			tSCK
		Low level pulse width	tSCKL (13)				1/2			
		High level pulse width	tSCKH (13)				1/2			
Serial input	Data setup time		tsDI (8)	SM0DA (PB5),	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (8)				0.03			
Serial output	Output delay time		tdD0 (12)	SM0DO (PB6), SM0DA (PB5)	・Specified with respect to falling edge of SIOCLK ・Specified as interval up to time when output state starts changing. ・See Fig. 6.	2.7 to 3.6			1tCYC +0.05	

Note 4-9-1 : These specifications are theoretical values. Add margin depending on its use.

SMIIC1 I²C Mode Input/Output Characteristics (Note 4-10-1) (Note 4-10-2) (Note 4-10-4)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	typ	max	unit
Clock	Input clock	Period	tSCL	SM1CK (PB4)	・See Fig. 8.	2.7 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM1CK (PB4)	・Specified as interval up to time when output state starts changing.	2.7 to 3.6	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6			1	Tfilt
Bus release time between start and stop		Input	tBUF	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6	2.5			Tfilt
		Output	tBUFx	SM1CK (PB4) SM1DA (PB5)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		5.5			µsec
					・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time		Input	tHD;STA	SM1CK (PB4) SM1DA (PB5)	・When SMIIC register control bit, I2CSHDS=0 ・See Fig. 8.	2.7 to 3.6	2.0			Tfilt
					・When SMIIC register control bit I2CSHDS=1 ・See Fig. 8.		2.5			
		Output	tHD;STAx	SM1CK (PB4) SM1DA (PB5)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		4.1			µsec
					・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time		Input	tSU;STA	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6	1.0			Tfilt
		Output	tSU;STAx	SM1CK (PB4) SM1DA (PB5)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		5.5			µsec
					・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.6			

Parameter		Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	typ	max	unit
Stop condition setup time	Input	tSU;STO	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6	1.0			Tfilt
	Output	tSU;STOx	SM1CK (PB4) SM1DA (PB5)	・Standard clock mode ・Specified as interval up to time when output state starts changing.		4.9			µsec
				・High-speed clock mode ・Specified as interval up to time when output state starts changing.		1.1			
Data hold time	Input	tHD;DAT	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6	0			Tfilt
	Output	tHD;DATx	SM1CK (PB4) SM1DA (PB5)	・Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU;DAT	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6	1			Tfilt
	Output	tSU;DATx	SM1CK (PB4) SM1DA (PB5)	・Specified as interval up to time when output state starts changing.		1tSCL-1.5Tfilt			
SM0CK and SM0DA pins fall time	Input	tF	SM1CK (PB4) SM1DA (PB5)	・See Fig. 8.	2.7 to 3.6			300	ns
	Output	tF	SM1CK (PB4) SM1DA (PB5)	・When SMIIC register control bits PSLW=1, PHV=1	3	20+0.1Cb (Note 4-10-3)		250	
				・SM0CK, SM0DA port output FAST mode ・Cb ≤ 100pF	3 to 3.6			100	

Note 4-10-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-10-2 : The value of Tfilt is determined by the values of the register SMIC1BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range :

250 ns ≥ Tfilt > 140 ns

Note 4-10-3 : Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 100 pF

Note 4-10-4 : The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows :

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 1

SCL frequency setting ≤ 100 kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC1BRG as follows :

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400 kHz

SLIIC0 Simple SIO Mode Input/Output Characteristics (Note 4-11-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification			
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (13)	SL0CK (PA4)	See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (13)				2			
		High level pulse width	tSCKH (13)				2			
Serial input	Data setup time		tsDI (9)	SL0DA (PA5),	・Specified with respect to rising edge of SIOCLK ・See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (9)				0.03			
Serial output	Output delay time		tdD0 (13)	SL0DO (PA6), SL0DA (PA5)	・Specified with respect to falling edge of SIOCLK ・Specified as interval up to time when output state starts changing. ・See Fig. 6.	2.7 to 3.6			1tCYC +0.05	

Note 4-11-1 : These specifications are theoretical values. Add margin depending on its use.

SLIIC1 I²C Mode Input/Output Characteristics (Note 4-12-1) (Note 4-12-2)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	Min	typ	max	unit
Clock	Input clock	Period	tSCL	SL0CK (PA4)	・See Fig. 8.	2.7 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
SL0CK and SL0DA pins input spike suppression time			tsp	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6			1	Tfilt
Bus release time between start and stop	Input		tBUF	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6	2.5			Tfilt
Start/restart condition hold time	Input		tHD;STA	SL0CK (PA4) SL0DA (PA5)	・When SMIIC register control bit, I2CSHDS=0 ・See Fig. 8.	2.7 to 3.6	2.0			Tfilt
					・When SMIIC register control bit I2CSHDS=1 ・See Fig. 8.		2.5			
Restart condition setup time	Input		tSU;STA	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6	1.0			Tfilt
Stop condition setup time	Input		tSU;STO	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6	1.0			Tfilt
Data hold time	Input		tHD;DAT	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6	0			Tfilt
	Output		tHD;DATx	SL0CK (PA4) SL0DA (PA5)	・Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input		tSU;DAT	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6	1			Tfilt
	Output		tSU;DATx	SL0CK (PA4) SL0DA (PA5)	・Specified as interval up to time when output state starts changing.		1tSCL-1.5Tfilt			

Parameter		Symbol	Applicable Pin/Remarks	Conditions	Specification				
					V_{DD} [V]	Min	typ	max	Unit
SL0CK and SL0DA pins fall time	Input	tF	SL0CK (PA4) SL0DA (PA5)	・See Fig. 8.	2.7 to 3.6			300	ns
	Output	tF	SL0CK (PA4) SL0DA (PA5)	・When SLIIC0 register control bits PSLW=1, PHV=1	3	20+0.1Cb (Note 4-12-3)		250	
				・SL0CK, SL0DA port output FAST mode ・Cb ≤ 100pF	3.0 to 3.6			100	

Note 4-12-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-12-2 : The value of Tfilt is determined by the values of the register SLIC0PCNT, bits 5 and 4 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range :

250 ns ≥ Tfilt > 140 ns

Note 4-12-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 100 pF

UART0 Operating Conditions at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR0	U0RX (P13), U0TX (P14), U0BRG (P07)		2.7 to 3.6	4		8	tBGCYC

Note 4-9 : tBGCYC denotes one cycle of the baudrate clock source.

UART2 Operating Conditions at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR2	U2RX (P16), U2TX (P17),		2.7 to 3.6	8		4096	tBGCYC

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

UART3 Operating Conditions at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR3	U3RX (P34), U3TX (P35),		2.7 to 3.6	8		4096	tBGCYC

Note 4-10 : tBGCYC denotes one cycle of the baudrate clock source.

■ **Pulse Input Conditions** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH (1) tPIL (1)	INT0 (P30), INT1 (P31), INT2 (P32), INT3 (P33), INT4 (P20), INT5 (P21), INT6 (P40), INT7 (P41)	・Interrupt source flag can be set. ・Event inputs for timers 2 and 3 are enabled.	2.7 to 3.6	2			tCYC
	tPIL (2)	RESB	Resetting is enabled.	2.7 to 3.6	10			µs

■ **AD Converter Characteristics** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

12-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60) to AN7 (P67), AN8 (P70) to AN15 (P77)		2.7 to 3.6		12		bit
Absolute accuracy	ETAD		(Note 6-1)	2.7 to 3.6			±16	LSB
Conversion time	TCAD12		Conversion time calculated	3.0 to 3.6	64		115	µs
				2.7 to 3.6	128		230	
Analog input voltage range	VAIN			2.7 to 3.6	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.7 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.7 to 3.6	–1			

– Conversion time calculation formula : TCAD12 = ($\frac{52}{\text{AD division ratio}}$ +2) × tCYC

8-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60) to AN7 (P67), AN8 (P70) to AN15 (P77)		2.7 to 3.6		8		bit
Absolute accuracy	ETAD		(Note 6-1)	2.7 to 3.6			±1.5	LSB
Conversion time	TCAD8		Conversion time calculated	3.0 to 3.6	39		71	µs
				2.7 to 3.6	79		140	
Analog input voltage range	VAIN			2.7 to 3.6	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.7 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.7 to 3.6	–1			

– Conversion time calculation formula : TCAD8 = ($\frac{52}{\text{AD division ratio}}$ +2) × tCYC

Note 6-1 : The quantization error (±1/2LSB) is excluded from the absolute accuracy.
Note 6-2 : The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.
The conversion time is twice the normal value when one of the following conditions occurs:
- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

■ **Consumption Current Characteristics** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$
typ : 3.3V

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP (1)	$V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$	・FmCF=10 MHz ceramic oscillator mode ・FmX'tal=32.768 kHz crystal oscillator mode ・System clock set to 10 MHz ・Internal RC oscillation stopped ・1/1 frequency division mode	2.7 to 3.6		5.0	12.0	mA
	IDDOP (2)		・FmCF=0Hz (oscillation stopped) ・FmX'tal=32.768 kHz crystal oscillator mode ・System clock set to internal RC oscillation ・1/1 frequency division mode	2.7 to 3.6		0.8	2.1	
	IDDOP (3)		・FmCF=0Hz (oscillation stopped) ・FmX'tal=32.768 kHz crystal oscillator mode ・System clock set to 32.768 kHz ・Internal RC oscillation stopped ・1/1 frequency division mode	2.7 to 3.6		30	136	μA

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT (1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$	・HALT mode ・FmCF=10 MHz ceramic oscillator mode ・FmX'tal=32.768 kHz crystal oscillator mode ・System clock set to 10 MHz ・Internal RC oscillation stopped ・1/1 frequency division mode	2.7 to 3.6		1.5	3.2	mA
	IDDHALT (2)		・HALT mode ・FmCF=0Hz (oscillation stopped) ・FmX'tal=32.768 kHz crystal oscillator mode ・System clock set to internal RC oscillation ・1/1 frequency division mode	2.7 to 3.6		0.2	0.8	
	IDDHALT (3)		・HALT mode ・FmCF=0Hz (oscillation stopped) ・FmX'tal=32.768 kHz crystal oscillator mode ・System clock set to 32.768 kHz ・Internal RC oscillation stopped ・1/1 frequency division mode	2.7 to 3.6		8.5	78	μA

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
HOLD mode consumption current	IDDHOLD (1)	V_{DD}1	HOLD mode ・CF1=VDD or open (external clock mode)	2.7 to 3.6		0.2	50	μA
	IDDHOLD (2)		HOLD mode ・CF1=VDD or open (external clock mode) ・LVD option selected	2.7 to 3.6		1.2	53	
HOLDX mode consumption current	IDDHOLD (3)		HOLDX mode ・CF1=VDD or open (external clock mode) ・FmX'tal=32.768 kHz crystal oscillator mode	2.7 to 3.6		4.6	71	
	IDDHOLD (4)		HOLDX mode ・CF1=VDD or open (external clock mode) ・FmX'tal=32.768 kHz crystal oscillator mode ・LVD option selected	2.7 to 3.6		5.6	74	

Note 7-1 : The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

■ F-ROM Programming Characteristics at Ta=+10 to +55°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW (1)	V_{DD}1	・Microcontroller erase current current is excluded.	2.7 to 3.6			10	mA
Onboard programming time	tFW (1)		・2K-byte erase operation	2.7 to 3.6			25	ms
	tFW (2)		・2-byte programming operation	2.7 to 3.6			45	μs

■ **Power-on Reset (POR) Characteristics** at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				Option selected voltage	min	typ	max	unit
Por release voltage	PORRL		・Select from option. (Note 8-1)	2.57V	2.47	2.57	2.72	V
				2.87V	2.77	2.87	3.02	
Detction voltage unknown state	POUKS		・See Fig 10. (Note 8-2)			0.7	0.95	
Power supply rise time	PORIS		・Power supply rise time from 0V to 1.6V.				100	ms

Note8-1 : The POR release level can be selected out of 2 levels only when the LVD reset function is disabled.
Note8-2 : POR is in an unknown state before transistors start operation.

■ **Low Voltage Detection Reset (LVD) Characteristics**
at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

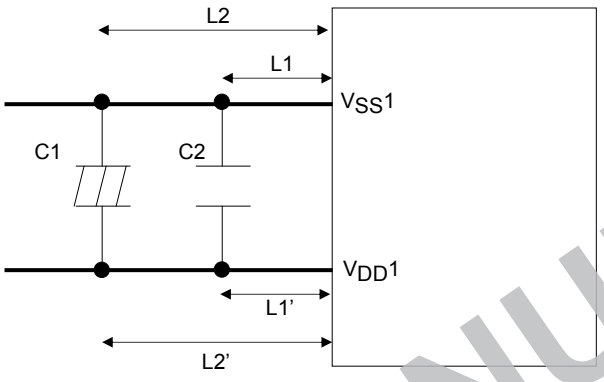
Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				Option selected voltage	min	typ	max	unit
LVD reset voltage (Note 9-1)	LVDET		・Select from option. (Note 9-2) ・See Fig 11.	2.81V	2.71	2.81	2.96	V
LVD hysteresis width	LVHYS			2.81V		60		mV
Detection voltage unknown state	LVUKS		・See Fig 11. (Note 9-3)			0.7	0.95	V
Low voltage detection minimum width (Replay sensitivity)	TLVDW		・LVDET-0.5V ・See Fig 12.		0.2			ms

Note9-1 : LVD reset voltage specification values do not include hysteresis voltage.
Note9-2 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.
Note9-3 : LVD is in an unknown state before transistors start operation.

■ Power Pin Treatment Conditions 1 ($V_{DD}1$, $V_{SS}1$)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins :

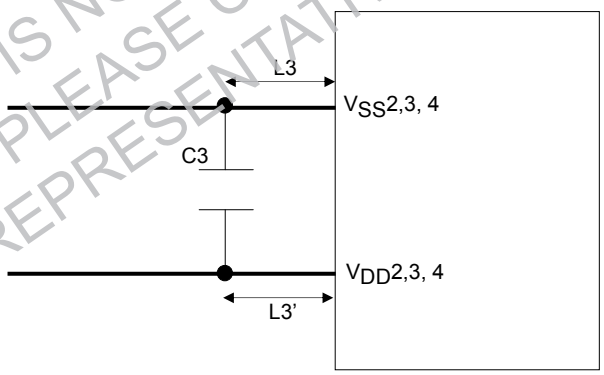
- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
  The capacitance of C2 should be approximately 0.1μF or larger.
- The $V_{DD}1$ and $V_{SS}1$ traces must be thicker than the other traces.



■ Power Pin Treatment Conditions 2 ($V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4)

Connect capacitors that meet the following condition between the $V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4 pins :

- Connect among the $V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4 pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1μF or larger.
- The $V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4 traces must be thicker than the other traces.



■ Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
10 MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	OPEN	680	2.2 to 2.6	0.02	0.2	C1, C2 integrated type
		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4)

■ Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768 kHz	EPSON TOYOCOM	MC-306	10	10	Open	330K	2.2 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note : The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

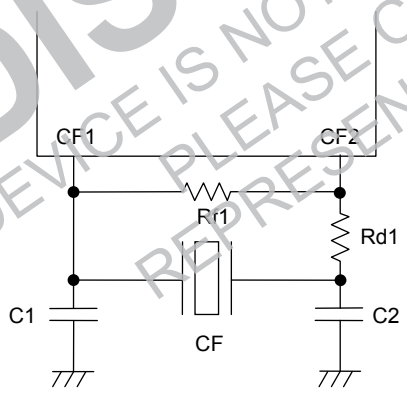


Figure 1. CF oscillator circuit

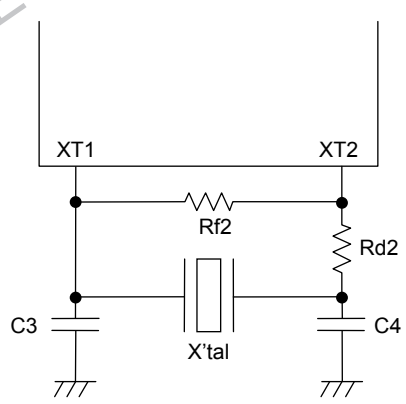


Figure 2. XT Oscillator Circuit

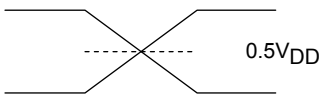
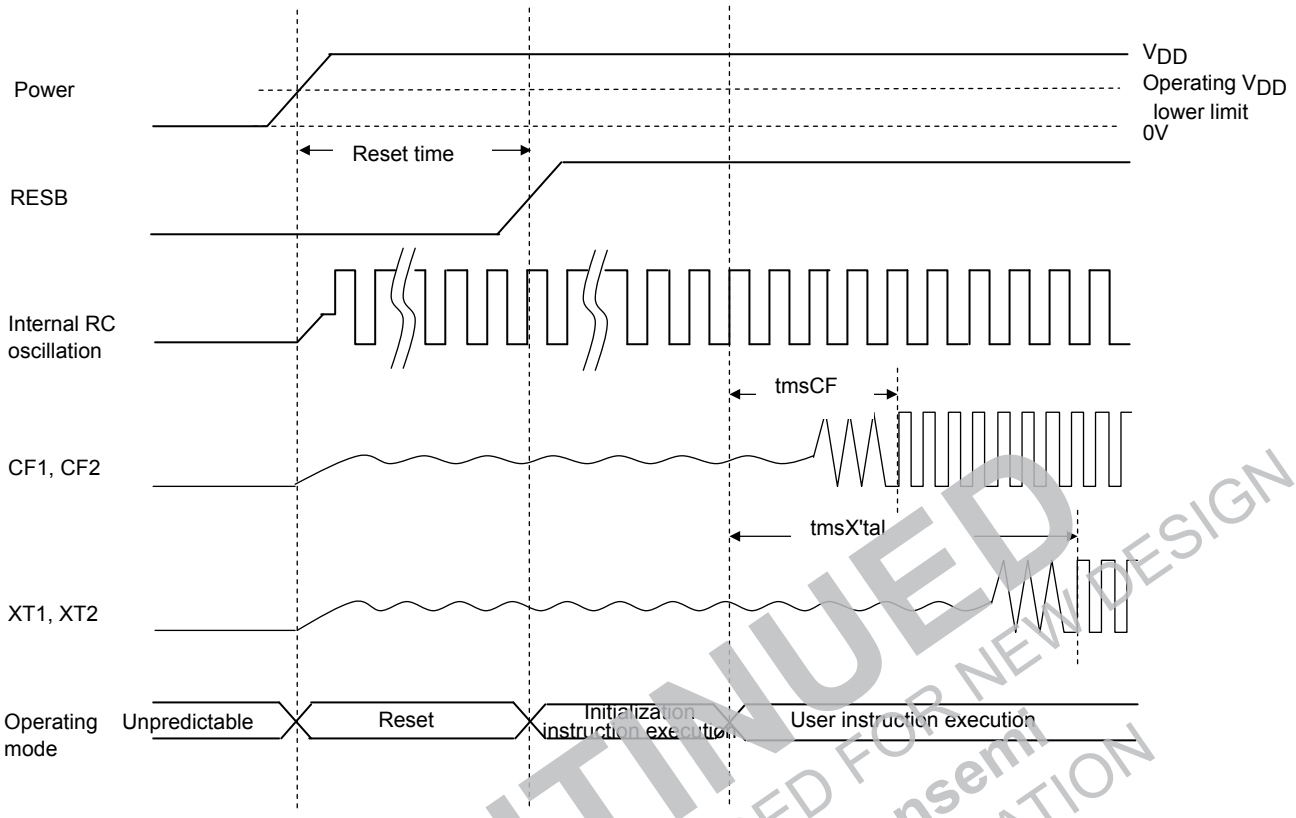
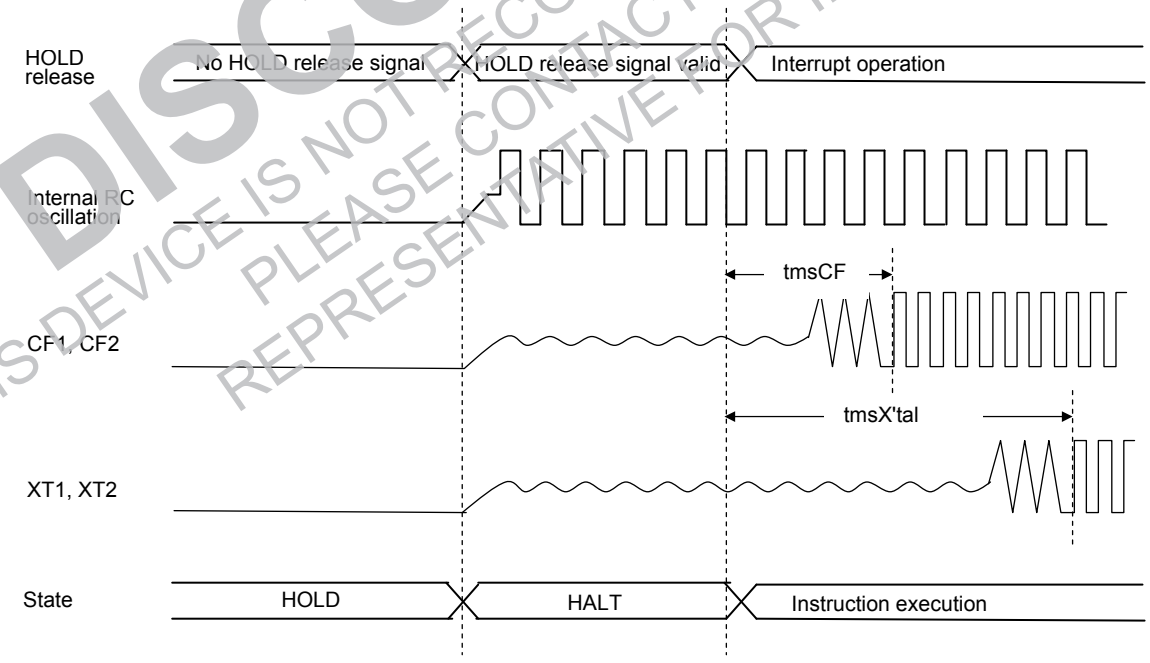


Figure 3. AC Timing Measurement Point

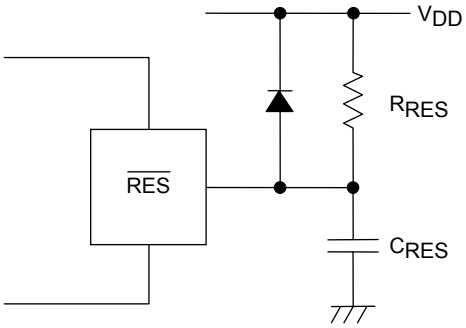


Reset Time and Oscillation Stabilization Time



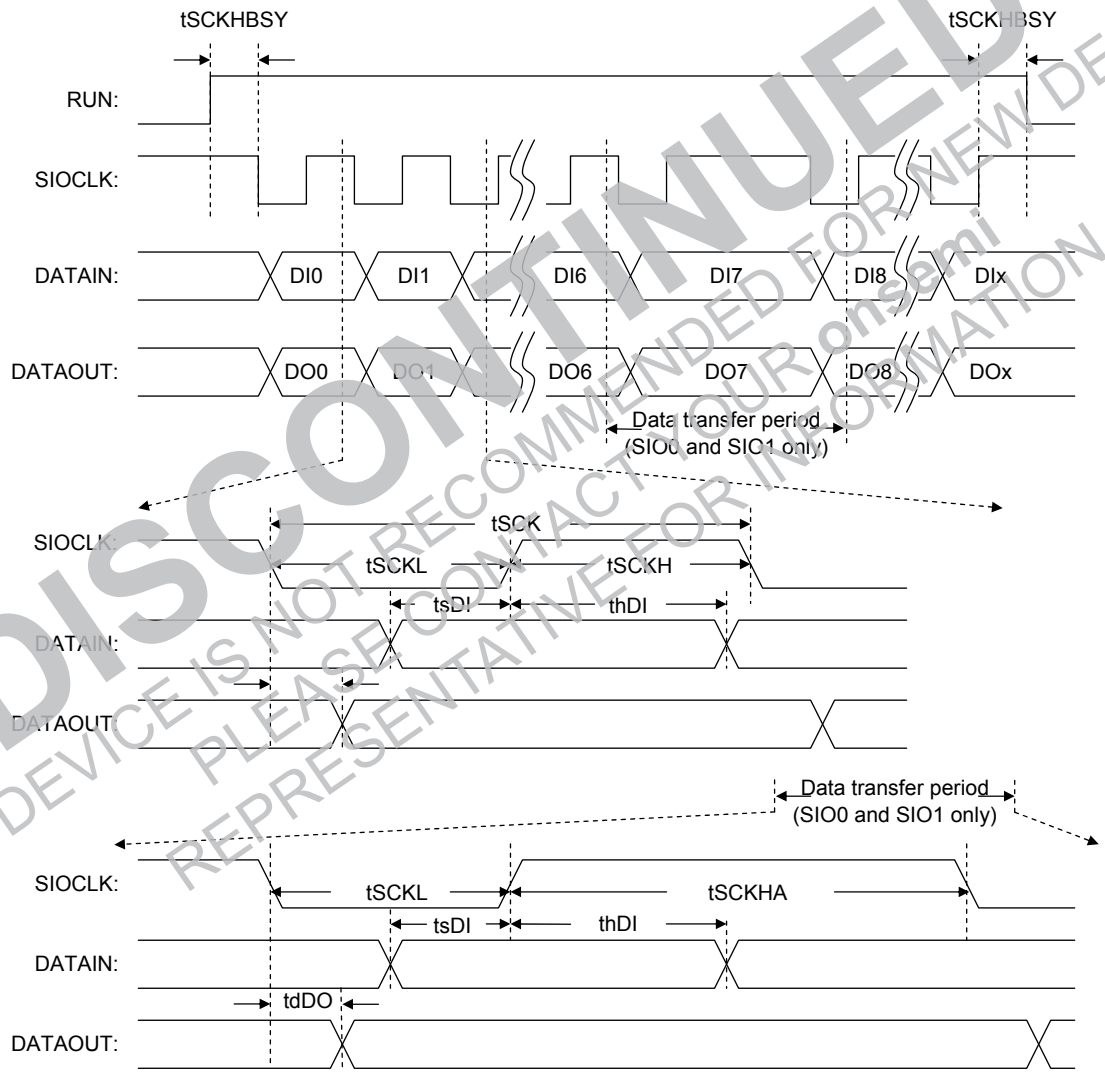
HOLD Release and Oscillation Stabilization Time

Figure 4. Oscillation Stabilization Time Timing Charts



Note :
Reset signal must be present when power supply rises.
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10 μs after the supply voltage gets stabilized.

Figure 5. Reset Circuit



* Remarks: DIx and DOx denote the last bits communicated; x=0 to 32768

Figure 6. Serial I/O Waveforms

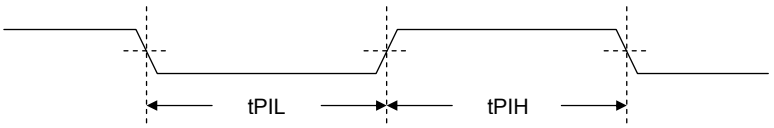
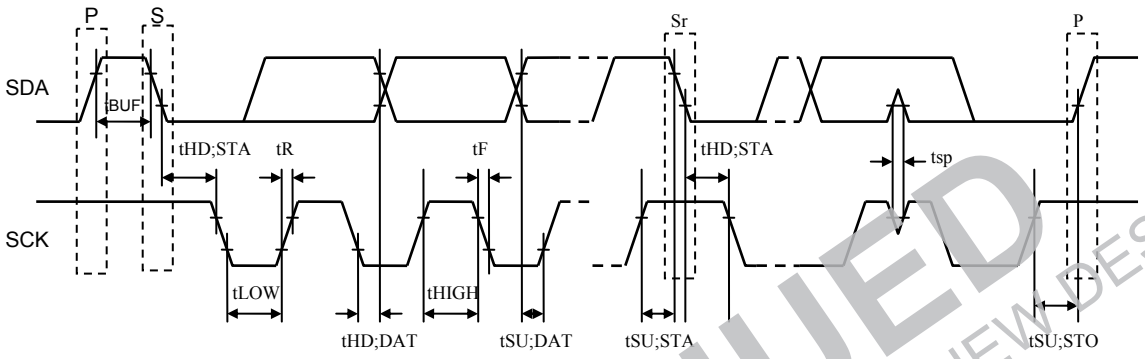


Figure 7. Pulse Input Timing Signal Waveform



S : Start condition
P : Stop condition
Sir : Restart condition

Figure 8. I^2C Timing

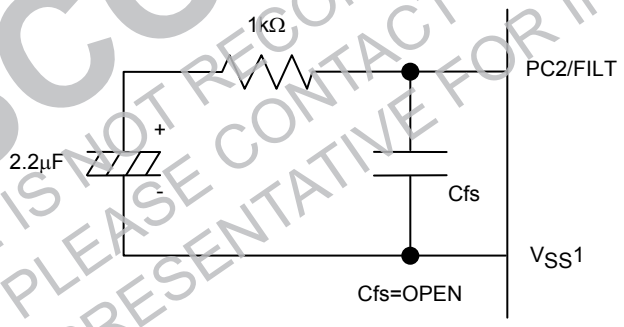


Figure 9. Recommended FILT Circuit

* Take at least 50ms to oscillation to stabilize after PLL is started.

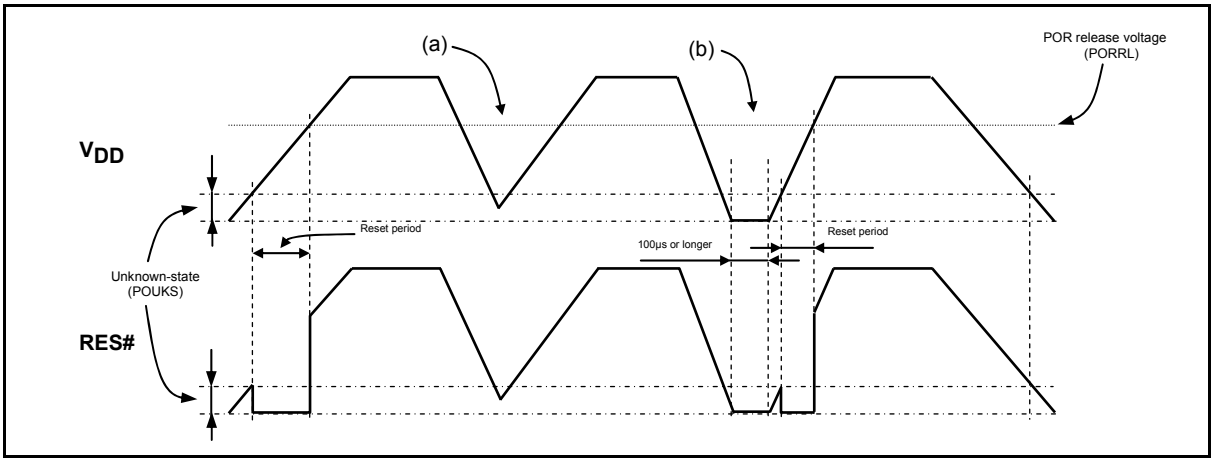


Figure 10. Waveform observed when only POR is used (LVD not used)
(RESET pin : Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

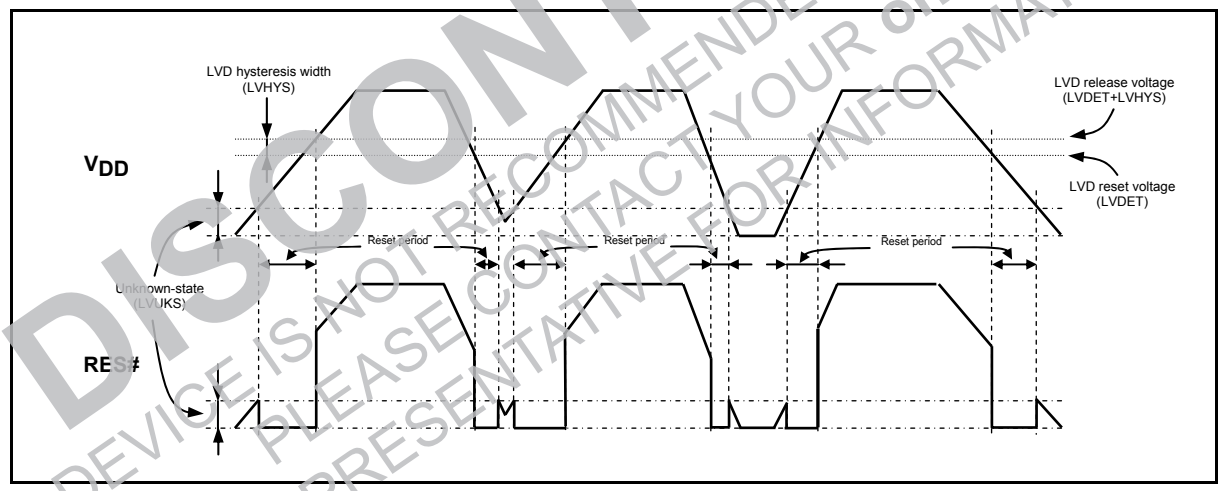


Figure 11. Waveform observed when both POR and LVD functions are used
(RESET pin : Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

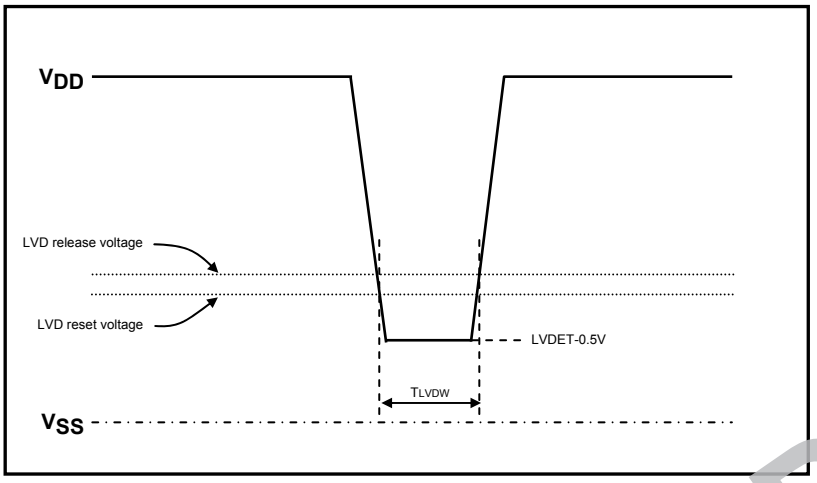


Figure 12. Low voltage detection minimum width
(Example of momentary power loss / Voltage variation waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC88FC3J0AUTJ2H	TQFP 100 14x14 (Pb-Free / Halogen Free)	900 / Tray JEDEC