LC823450 ERRATA

Errata
Silicon Errata for LC823450

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ERRATA

Introduction

This document lists silicon erratas, as well as features of the LC823450 that may be unexpected to the user.

This document refers to the silicon revisions listed in the table below.

Table 1.

Revision	MODEM Register
V0.1.0.0	0x0100

Issues

AudioBuffer May Not Be Cleared Normally

By the problem in the AudioBuffer, a problem such as a value written in not being readable definitely may occur in clear by AudioBuffer Clear Register (ABUFCLR). Because you can evade it by software, please refer to our person in charge.

Affected Revisions: V0.1.0.0

The Implementation of the Register of SysTick is Originally Different

As for NOREF bit, SKEW bit and TENMS bit of SysTick Calibration Value Register, implementation unlike the original intention is done. Specifically, please refer to the application note, ”AND9625/D, System Functions User’s Manual for LC823450 Software Development”.

Affected Revisions: V0.1.0.0

The Data Are Read from DMB Area of LPDSP32 Has Problems

Because internal SRAM controller (Segment0 − Segment8) has a problem, when data are written in internal SRAM by Cortex®−M3/DMAC/USB2.0 Host and the data are read from the DMB of LPDSP32, the data which were written at last cannot be read correctly. It is necessary to perform dummy write once after having written in the last data to begin to read it correctly. Anything of Byte/Half Word/Word is enough for dummy write.

Affected Revisions: V0.1.0.0

exFAT File System Has Problems

- When the function such as findfirst, readdir and fstat is used, the problem that a file/directory stored using the letter except the alphanumeric character is not found in occurs. Because it can be evaded by a patch program, please refer to our person in charge.
- When API to input in FullPath such as open, qopen and mkdir was used, the file/directory that top character string begins in “.” cannot be appointed.

Affected Revisions: V0.1.0.0

USB2.0 Device Driver Has Problems

When Host is reconnected to be defective on USB Device driver with a built-in ROM code with having access to USB, it may not be recognized as an MSC drive by Host. When a USB boot is performed, please be careful. Please usually refer to our person in charge because it can be evaded by a patch program.

Affected Revisions: V0.1.0.0

The Data Are Read from AHB Shadow Area Has Problems

Because internal SRAM controller (Segment0 − Segment8) has a problem, when data are written in internal SRAM of the original address by Cortex−M3/DMAC/USB2.0 Host and the data are read from Shadow area by Cortex−M3/DMAC/USB2.0 Host, the data which were written at last cannot be read correctly. When data written in at Shadow area are begun to read from the original address, it is similar. In addition, it is similar when data are read and written between Shadow area which is located at address 0x0000_0000 when REMAP register was set 2’b01 and Shadow area which is located at address range 0x2000_0000 to 0x2017_FFFF or internal SRAM of the original addresses. It is necessary to perform dummy write once after having written in the last data or is not used Shadow area to begin to read it normally. Anything of Byte/Half Word/Word is enough for dummy write. When data are read and written between original address and Shadow area, the combinatorial table which occurs of the malfunction is as follows.

Table 2.

		Read		
		Shadow Area (REMAP = 2'b01) [0x0000_0000 ～ 0x0001_FFFF]	Original Address [0x0200_0000 ～ 0x0217_FFFF]	Shadow Area [0x2000_0000 ～ 0x2017_FFFF]
Write	Shadow Area (REMAP = 2'b01) [0x0000_0000 ～ 0x0001_FFFF]	Normally	Abnormally	Abnormally
	Original Address [0x0200_0000 ～ 0x0217_FFFF]	Abnormally	Normally	Abnormally
	Shadow Area [0x2000_0000 ～ 0x2017_FFFF]	Abnormally	Abnormally	Normally

Affected Revisions: V0.1.0.0

Writing to the LPDSP32 DMB Area Has Problems

Because internal SRAM controller (Segment0 – Segment8) has a problem, when data are written in internal SRAM of the LPDSP32 DMB area and data are read from Cortex−M3/DMAC/USB2.0 Host or DMA/PM area of LPDSP32, data written in may not be read normally. To evade malfunction, the data which were written in internal SRAM of the LPDSP32 DMB area must not be read from Cortex−M3/DMAC/USB2.0 Host or the LPDSP32 DMA/PM area.

Affected Revisions: V0.1.0.0

Write to the SDRAM area Has Problems

Because SDRAM controller has a problem, it may not be written the data correctly in some cases as shown below.

- When the write access with un−aligned to SDRAM by using Cortex−M3 or USB2.0 Host was executed, it may not be written the data correctly. Specifically, when the write access by Word with un−aligned (not aligned four Bytes unit) or by Half Word with un−aligned (not aligned two Bytes unit) was executed, it may not be written the data correctly. It is necessary to execute the write access with aligned.
- When the write access by Half Word or Byte to SDRAM by using DMIO of LPDSP32, USB2.0 Host or SWD (Cortex−M3) debugger was executed, it may not be written the data correctly. It is necessary to execute the write access by Word with aligned, or to transfer the data by using Cortex−M3 with aligned or DMAC via internal SRAM.

The combinational table of Host and write access which the bug occurs is follow:

Table 3.

		SDRAM Write				
		Word		Half Word		Byte
		Aligned	Un−aligned	Aligned	Un−aligned	Aligned
Host	Cortex−M3 Core0	Normally	Abnormally	Normally	Abnormally	Normally
	Cortex−M3 Core1	Normally	Abnormally	Normally	Abnormally	Normally
	LPDSP32	Normally	− (Note 1)	Abnormally	− (Note 1)	Abnormally
	DMAC	Normally	− (Note 1)	Normally	− (Note 1)	Normally
	USB2.0 Host	Normally	Abnormally	Abnormally	Abnormally	Abnormally
	Cortex−M3 Debugger	Normally	− (Note 2)	Abnormally	− (Note 2)	Abnormally

1. Un−aligned access is inhibited.
2. Un−aligned access is not supported.

Affected Revisions: V0.1.0.0

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