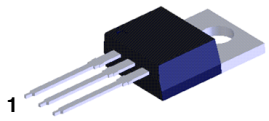
Vertical Deflection Output Power Amplifier

KSA940

PNP Epitaxial Silicon Transistor
Complement to KSC2073



TO−220−3LD
CASE 340AT

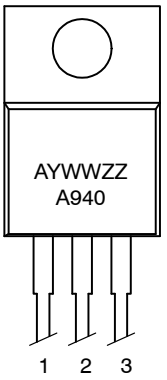
- These are Pb−Free Devices

ABSOLUTE MAXIMUM RATINGS
(T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector−Base Voltage	−150	V
V_{CEO}	Collector−Emitter Voltage	−150	V
V_{EBO}	Emitter−Base Voltage	−5	V
I_C	Collector Current	−1.5	A
I_B	Base Current	−0.5	A
P_C	Collector Dissipation (T_a=25°C)	1.5	W
P_C	Collector Dissipation (T_C=25°C)	25	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



1: Base
2: Collector
3: Emitter

A = Assembly Plant Code
YWW = 3−Digit Date Code (Year and Week)
ZZ = 2−Digits Lot Run Traceability Code
A940 = Specific Device Code

ELECTRICAL CHARACTERISTICS
(T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut−off Current	V_{CB} = − 120 V, I_E = 0	−	−	−10	μA
I_{EBO}	Emitter Cut−off Current	V_{EB} = − 5 V, I_C = 0	−	−	−10	μA
h_{FE}	DC Current Gain	V_{CE} = − 10V, I_C = − 500 mA	40	75	140	
V_{CE}(sat)	Collector−Emitter Saturation Voltage	I_C = − 500 mA, I_B = − 50 mA	−	−	−1.5	V
V_{BE}(on)	Base−Emitter ON Voltage	V_{CE} = − 10 V, I_C = − 500 mA	−0.65	−0.75	−0.85	V
f_T	Current Gain Bandwidth Product	V_{CE} = − 10 V, I_C = − 500 mA	−	4	−	MHz
C_{ob}	Output Capacitance	V_{CB} = − 10 V, I_E = 0, f = 1 mHz	−	55	−	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Package	Shipping
KSA940TU	TO−220−3LD (Pb−Free)	1000 Units / Tube

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TYPICAL PERFORMANCE CHARACTERISTICS

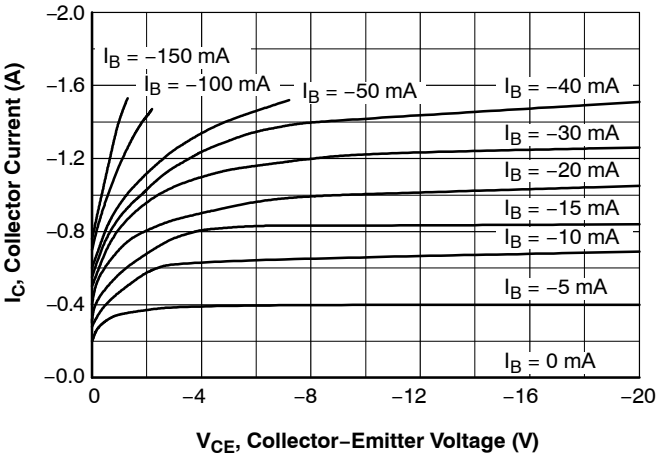

Figure 1. Static Characteristic

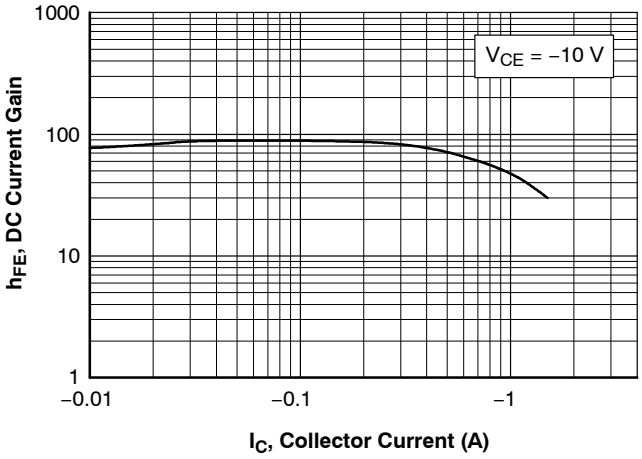

Figure 2. DC Current Gain

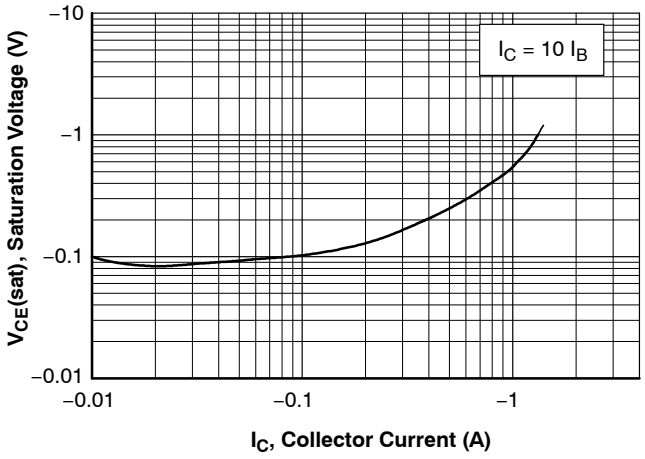

Figure 3. Collector−Emitter Saturation Voltage

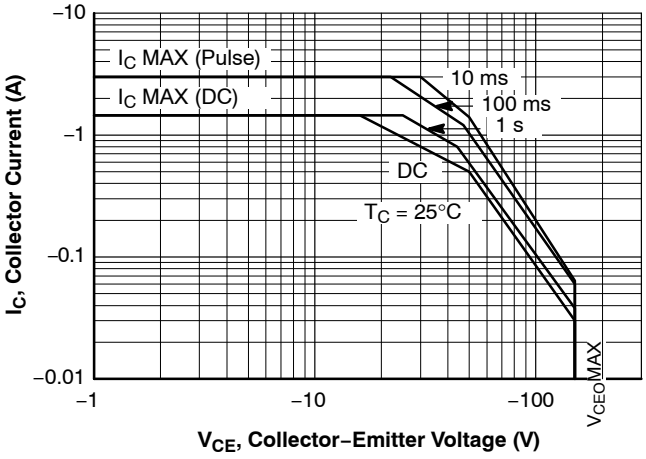

Figure 4. Safe Operating Area

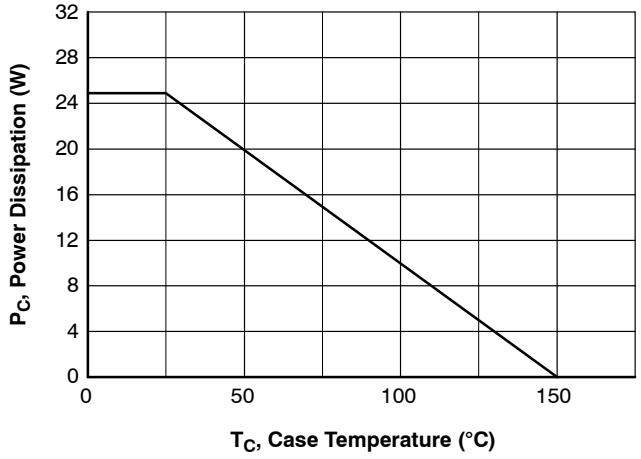

Figure 5. Power Derating

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
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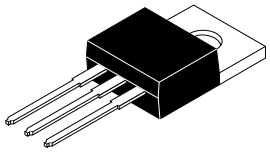
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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