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Dear Customer:

I am pleased to present you with the ON Semiconductor Reliability and Quality Handbook. ON Semiconductor is certified to ISO-9001, IATF16949, AS9100 as well as ISO 14001, OHSAS 18000 and military standards. Our medical manufacturing facility is certified to ISO-13845. We also received distinction by being classified as a ‘Trusted Supplier’. Our Road to Zero Defect initiative recognizes the integrated effectiveness of building both “Reliability” and “Quality” into our services, processes and products. We are committed to developing and maintaining a distinctive, world class Quality system, which transcends all international Quality standards and truly exceeds customer expectations. This handbook is intended to provide basic information on the reliability and quality aspects of the products supplied by ON Semiconductor worldwide. ON Semiconductor maintains a portfolio that includes a broad spectrum of products in a full array of package technologies, including but not limited to, the following products:

- **Power Management Devices**: AC-DC Controllers & Regulators; DC-DC Controllers, Converters, & Regulators; LED Drivers; Motors and Load Drivers; Power Modules; Voltage & Current Management
- **Sensor Devices**: Image Sensors & Processors; Light & Touch Sensors; Thermal Management; Battery-Free Wireless Sensors
- **Analog, Logic and Timing Devices**: Amplifiers & Comparators, Clock Generation; Clock & Data Distribution; Interfaces; Memory; Microcontrollers; Standard Logic
- **Discrete Devices**: Bipolar Transistors; Diodes & Rectifiers; ESD, EMI & Surge Protection Diodes & Filters; IGBTs & FETs; Tunable Components
- **Connectivity, Custom and SoC Devices**: Audio/Video ASSP, Connectivity, ASICs; Custom Foundry Services; Customer Image Sensors; Integrated Passive Devices

ON Semiconductor is headquartered in Phoenix, Arizona (U.S.A.) and has a number of international facilities, which have on-site test, reliability testing and product analysis capabilities. ON Semiconductor has developed a global marketing, sales and field quality network to supply its customers with quality products, information and services.

ON Semiconductor’s Quality System and Business Operating System are synonymous. The company established a Core Business Process Model to ensure that we meet or exceed our customer’s expectations and our business goals. We’ve adopted the approach of taking international standards and some common customer requirements and aligning them within our existing Business Model.

Our Quality Policy states, “We will exceed Customer Expectations with our Superior Products and Services.” In addition, our Quality statement declares, “Every ON Semiconductor employee is personally responsible for ensuring the highest Quality in the products and services delivered to internal and external customers. Continuous improvement in the quality of our processes, products and service is fundamental to the achievement of customer satisfaction.” The policy emphasizes that the responsibility to achieve quality, both in services and products belongs to each and every one of us. I cannot over emphasize this point! ALL of us, every business leader, sales person, project manager, operator, engineer, EVERY ON Semiconductor employee, is personally responsible for the Quality of those products and services that we individually and collectively supply to our Customers.

And finally, because we believe “fulfilling customer requirements is the first step in customer satisfaction,” our Core Business process model begins with the customer and ends with the customer. The strength of our business initiatives and our focus on servicing our customers ensures ON Semiconductor’s success now and in the future.

For additional questions, please contact 1 (800) 282-9855 or email us at quality@onsemi.com.

Brent Wilson
Senior Vice President, Global Quality Assurance and Supply Chain Operations
ON Semiconductor
Section 1 – Introduction

ON Semiconductor (Nasdaq: ON) is driving energy efficient innovations, empowering customers to reduce global energy use. The company is a leading supplier of semiconductor-based solutions, offering a comprehensive portfolio of energy efficient power management, analog, sensors, logic, timing, connectivity, discrete, SoC and custom devices. The company’s products help engineers solve their unique design challenges in automotive, communications, computing, consumer, industrial, medical, aerospace and defense applications. ON Semiconductor operates a responsive, reliable, world-class supply chain and quality program, a robust compliance and ethics program, and a network of manufacturing facilities, sales offices and design centers in key markets throughout North America, Europe and the Asia Pacific regions. For more information, visit www.onsemi.com.

The company’s current portfolio numbers close to 60,000 products which includes full Pb-Free, ROHS compliant device offerings. We shipped more than 55 billion units in 2014, 60 billion units in 2015, 70 billion units in 2016, and over 76 billion units in 2017. These products are put in the hands of our customers through our highly responsive supply chain. With our global logistics network and strong portfolio of power semiconductor devices, ON Semiconductor is a preferred supplier of power solutions to engineers, purchasing professionals, distributors and contract manufacturers in the computer, cell phone, portable devices, automotive and industrial markets.

Headquartered in Phoenix, Arizona, we are a public company and trade on the NASDAQ under the symbol (ON). We employ approximately 34,000 people worldwide and have manufacturing facilities, sales, offices and design centers though out North, America, Asia Pacific and Europe. We strive to continuously meet our customers’ current and anticipated semiconductor component needs so well that, “Customers will come to us first!” We enact this vision by each day fulfilling our mission to: Eliminate any reason for the customer to buy from other suppliers by providing the highest Quality components and services at competitive prices with the most reliable delivery and ease of purchase.

ON Semiconductor has various international certifications. The foundation of our success is customer satisfaction, customer confidence and continuous improvement. The extent of these efforts touches every function and region of our business. Our quality resolve is deeply ingrained in every employee.

This handbook is intended to review and provide information on the reliability and quality aspects of the semiconductor products supplied by ON Semiconductor worldwide.

In today’s semiconductor marketplace, two important elements for the success of a company are its quality and reliability systems. They are interrelated, reliability being the quality extended over the expected life of the product. For any manufacturer to remain in business, its products must meet or exceed the basic quality and reliability standards. As a semiconductor supplier, ON Semiconductor has successfully established reliability and quality standards for products, processes, and services that exceed the basic standards and meet our customers’ needs. For the purpose of this report, the most stringent and demanding definitions of quality and reliability are used.

Quality may be defined as:

• Reduction of variability around a target so that conformance to customer requirements and expectations can be achieved in a cost effective way.

• The probability that a device (equipment, parts) will have performance characteristics within specified limits.

• Fitness for use.

Reliability is defined as:

• Quality in time and environment (temperature, voltage, etc.).

• The probability that a semiconductor device, which initially has satisfactory performance, will continue to perform its intended function for a given time under actual usage environments.
At ON Semiconductor, our reliability and quality assurance program is designed to generate ongoing data for both reliability and quality for the various product families. Both reliability and quality monitors are performed on the different major categories of semiconductor products. These monitors are designed to test the product’s design and material as well as to identify and eliminate potential failure mechanisms to ensure reliable device performance in a real world application. Thus, the primary purpose of the program is to identify trends from the data generated and use that information to continuously improve our products. In addition, this reliability and quality data can be utilized by our customers for failure rate predictions.

This handbook is a compilation of reliability test results and quality data from all semiconductor operations. The data contained are annual summaries of many detailed tests and evaluations performed in ON Semiconductor locations worldwide.

Detailed reliability reports for product line or device types are available upon request and can be obtained through your local ON Semiconductor Sales or Customer advocacy representative, or from the sources indicated in this handbook.
ON Semiconductor is registered to both ISO 9001 and IATF16949. ON Semiconductor’s Quality System and Business Operating System are synonymous. The company established a Core Business Process Model, which shown below ensures we meet or exceed our customer’s expectations and our business goals. We have adopted the approach of taking international standard and common customer requirements and aligning them into our existing Business Model.

Our Quality Policy states, “We will exceed Customer Expectations with our Superior Products and Services.” In addition, our Quality statement declares, “Every ON employee is personally responsible for ensuring the highest Quality in the products and services delivered to internal and external customers. Continuous improvement in the quality of our processes, products and service is fundamental to the achievement of customer satisfaction.” Since we believe that, in other words, “fulfilling customer requirements is the first step in customer satisfaction”, our Core Business process model begins with the customer and ends with the customer.

Customer Business Process Model and Structure

Our core business processes are linked to our global work processes ensuring alignment between our business strategy and practices.

ON Semiconductor Certification Status

Each of our manufacturing sites, support, marketing and design groups have been certified by Det Norske Veritas (DNV). Certificates are available on our website.

Six Sigma®

ON Semiconductor is committed to the Six Sigma philosophy in both our manufacturing and business environments.

Our Six Sigma efforts for the new millennium and beyond will be to:
• Continue our efforts to achieve Six Sigma results - and beyond - in everything we do (products and services)
• Measure in parts per billion (ppb)

Customer Satisfaction

ON Semiconductor is engaged in a very competitive global marketplace. We will not grow if we continue to focus only on our heritage and our past accomplishments. We continually strive to understand our customers’ needs for service and support by focusing on customer service.

A key driver is the feedback we receive on the quality of our products and services. We strive to understand this so well that we will be able to anticipate solutions to product and service needs our customers have yet to recognize. This means listening to their ideas about how we can better serve them from a total system’s perspective - from idea introduction to successful delivery of product or service.

How we gather this feedback? By asking how our external customers perceive ON Semiconductor in terms of quality and by asking them about their expectations of ON Semiconductor via deployment of the Annual Quality Survey. The objectives that will be accomplished through the Annual Quality Survey are:
• Continue strengthening our business operating system by determining our customers’ current business expectations.
• Provide a baseline measurement of our performance against those expectations.
• Provide feedback on our performance against customer expectations on an annual basis (trends).
• Track changing expectations in order to modify our quality system accordingly.
• Provide a basis for a consistent set of customer satisfaction metrics that provides a check of our internal quality measurements.

Therefore, each business must develop customer driven indices - using factors established by the customer - and set aggressive improvement goals.

Our Goals will also change over time as customers raise the bar when we meet their current expectations.
ON Semiconductor Learning and Development

ON Semiconductor has instituted education and training that is directly linked to the strategic company goals identified by the Executive Staff. All corporate driven training delivered is targeted toward those areas. To keep current with business needs, the training focus is reviewed annually in alignment with the corporate strategy. When the focus is determined, supporting training and education events are identified, designed, developed, and/or sourced to meet the need. This is a dynamic process with inputs from the organization, the employees and external market factors.

At the functional level, organizational capability is assessed, matched with current skills of the population, and gaps are filled accordingly. This job/skill match process allows alignment of business goals and job skill requirements.

The Lean Six Sigma Green and Black Belt training and SPC programs are examples of the many training programs developed by ON Semiconductor.

Section 3 – Introduction to Reliability & Quality Methods

For semiconductors, the often critical nature of the equipment in which they are used leaves no room for failure. By their very nature, properly designed semiconductor devices will far outlast the life expectancy of the equipment for which they are intended, and careful processing will ensure that each device meets the specifications to which it is designed.

The result of proper design and careful planning is a quality product.

The reliability and quality methods discussed in this handbook contribute to the attainment of Six Sigma performance in all of our operations.

Reliability Stress Tests

The following are brief descriptions of the tests commonly used in the reliability assessment. Not all of the tests listed are performed on each product. Other tests may be performed when appropriate. The information herein is typical of the testing performed. Variations to the following will be found throughout this document based on the limitations of the specific device being tested.

AUTOCLAVE

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Autoclave is a highly accelerated and destructive test. Alternative test to Unbiased HAST.

Typical Test Conditions: $T_A = 121^\circ C$, $rh = 100\%$, $p = 1$ Atmosphere (15 psig), $t = 24$ to 240 hours.

Common Failure Modes: Parametric shifts, high leakage and/or catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing.

UNBIASED HIGHLY ACCELERATED STRESS TEST

Unbiased Highly Accelerated Stress is the same as HAST (below) with no bias. UHAST accelerates the same failure mechanisms as Autoclave.

Typical Test Conditions: $T_A = 130^\circ C$, $rh = 85\%$ to $95\%$, $p = 2$ Atmospheres, Bias = 80-100% of Data Book maximum rating, $T = 96$ to 240 hrs.

Common Failure Modes: Parametric shifts, high leakage and/or catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing.

HIGHLY ACCELERATED STRESS TEST

Highly Accelerated Stress Test uses a pressurized environment to produce extremely severe temperature, humidity and bias conditions. HAST accelerates the same failure mechanisms as High Humidity High Temperature Bias and Temperature Humidity Bias.

Typical Test Conditions: $T_A = 110$-130$^\circ C$, $rh = 85\%$ to $95\%$, $p = 2$ Atmospheres, Bias = 80% to 100% of Data Book maximum rating, $t = 96$ to 246 hours.

Common Failure Modes: Parametric shifts, high leakage and/or catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing.
HIGH HUMIDITY HIGH TEMPERATURE BIAS/TEMPERATURE HUMIDITY BIAS

This is an environmental test designed to measure the moisture resistance of plastic encapsulated devices. A bias is applied to create an electrolytic cell necessary to accelerate corrosion of the die metallization. With time, this is a catastrophically destructive test. Alternative test to HAST.

**Typical Test Conditions:** \( T_A = 85 \, ^\circ C \text{ to } 95 \, ^\circ C, \, \text{rh} = 85\% \text{ to } 95\%, \) \( \text{Bias} = 80\% \text{ to } 100\% \) of Data Book maximum rating, \( t = 96 \) to 1008 hours.

**Common Failure Modes:** Parametric shifts, high leakage and/or catastrophic failure.

**Common Failure Mechanisms:** Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing.

HIGH TEMPERATURE GATE BIAS

This test is designed to electrically stress the gate oxide under a bias condition at high temperature.

**Typical Test Conditions:** \( T_A = 150 \, ^\circ C, \, \text{Bias} = 100\% \) of Data Book maximum Vgs rating, \( t = 168 \) to 1008 hours.

**Common Failure Modes:** Parametric shifts in gate leakage and gate threshold voltage.

**Common Failure Mechanisms:** Random oxide defects and ionic contamination.

HIGH TEMPERATURE REVERSE BIAS /HIGH TEMPERATURE OPERATION LIFE

The purpose of these tests is to align mobile ions by means of temperature and voltage stress to form a high-current leakage path between two or more junctions.

**Typical Test Conditions:** \( T_A = 85 \, ^\circ C \text{ to } 175 \, ^\circ C, \, \text{Bias} = 80\% \text{ to } 100\% \) of Data Book maximum rating, \( t = 168 \) to 1008 hours.

**Common Failure Modes:** Parametric shifts in leakage and gain.

**Common Failure Mechanisms:** Ionic contamination on the surface or under the metallization of the die.

HIGH TEMPERATURE STORAGE LIFE

High temperature storage life testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures.

**Typical Test Conditions:** \( T_A = 125 \, ^\circ C \text{ to } 200 \, ^\circ C, \, \text{no bias}, \, t = 24 \) to 1008 hours.

**Common Failure Modes:** Parametric shifts in leakage, \( V_f, \) \( V_{CE}s, \) \( R_{DSon} \) and gain.

**Common Failure Mechanisms:** Bulk die and diffusion defects.

INTERMITTENT OPERATING LIFE

The purpose of this test is to accelerate the stresses on all bonds and interfaces between the chip and mounting face of the device that simulates repeated turn on and off of equipment; checking the integrity of both wire and die bonds by means of thermal stressing.

**Typical Test Conditions:** \( T_A = 25 \, ^\circ C, \, P_d = \text{Data Book maximum rating}, \, T_{on} = T_{off} = 2-5 \text{ min (package dependent)}, \, \text{DTJ of } 125 \, ^\circ C \text{ to } 175 \, ^\circ C, \, t = 1000 \) to 15000 cycles.

**Common Failure Modes:** Parametric shifts and catastrophic failure.

**Common Failure Mechanisms:** Foreign material, crack and bulk die defects, metallization, wire and diebond defects.

SOLDERABILITY

The purpose of this test is to measure the ability of device leads/terminals to be soldered after an extended period of storage or shelf life.

**Typical Test Conditions:** J-STD-002

**Common Failure Modes:** Pin holes, dewetting, non-wetting.

**Common Failure Mechanisms:** Poor plating, contaminated leads.

SOLDER HEAT

This test is used to measure the ability of a device to withstand the temperatures as may be seen in wave soldering operations. Electrical testing is the endpoint criterion for this stress.

**Typical Test Conditions:** Solder Temperature = 260°C, \( t = 10 \) seconds.

**Common Failure Modes:** Parameter shifts, mechanical failure.

TEMPERATURE CYCLING (AIR-TO-AIR)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and transitions between temperature extremes. This testing will also expose excessive thermal mismatch between materials.

**Typical Test Conditions:** \( T_A = -65 \, ^\circ C \text{ to } 150 \, ^\circ C, \, \text{cycle} = 100 \) to 1000.

**Common Failure Modes:** Parametric shifts and catastrophic failure.

**Common Failure Mechanisms:** Wire bond, cracked or lifted die and package failure.
Reliability Data Analysis

Reliability is the probability a semiconductor device will perform its specified function for a specified time period under specified environmental conditions. In general, reliability can be thought of as maintaining acceptable quality performance over time and environmental conditions. A key characteristic of reliability is the hazard rate \( h(t) \). The hazard rate roughly represents the rate devices will fail as a function of time. The most widely used probability distribution used for analyzing semiconductor device reliability data is the exponential distribution. The hazard rate function for the exponential distribution 1 (this is usually called the failure rate) is not a function of time and is very simple to estimate. The point estimate of the failure rate is obtained by dividing the number of observed failures by the total number of device-hours from the stress test. Device-hours are defined as the product of the number of devices that are stress tested and the duration of the stress test. This is called the point estimate because it is based on a sample of devices from the population of all devices with similar characteristics, and it does not account for the uncertainty caused by estimating the failure rate from a sample. For modern semiconductor devices, the failure rates are extremely low and the failure rate is presented in units of FIT, where FIT is the number of failures per billion device-hours. These calculations are appropriate when the exact failure times are known. More complicated censoring situations can be analyzed using techniques presented elsewhere (e.g., Meeker and Escobar, “Statistical Methods for Reliability Data,” (1998)).

In order to account for the uncertainty due to calculating the failure rate based on a sample, one must apply confidence limits to the point estimate. The relevant confidence interval for device reliability calculations is the one-sided upper confidence interval of the failure rate. The one-sided upper confidence interval provides an estimate the failure rate that is unlikely to be exceeded by any given point estimate at a given confidence level. The appropriate sampling distribution for the failure rate of the exponential distribution is the chi-square distribution \( \chi^2 \). This means that if one were to calculate the failure rate of many independent samples drawn from the same exponential population, then the distribution of the point estimates of the failure rate would follow a \( \chi^2 \) distribution. The one-sided upper confidence estimate of the exponential failure rate where the life test is time-censored is given by:

\[ \lambda_{1\text{-sided}} = \frac{\chi^2 (\alpha, 2r + 2)}{2nt} \cdot 10^9 \]

where:

- \( \lambda_{1\text{-sided}} \) = one-sided upper confidence level failure rate estimate in FIT
- \( \chi^2 \) = the inverse cumulative distribution function for the chi-square distribution

\( \alpha = (100 - \text{confidence level})/100 \)

- \( r \) = number of failures observed during the stress test
- \( n \) = number of devices in stress test sample
- \( t \) = stress test duration in hours

Values of the inverse cumulative distribution function for the chi-square distribution for the 60% and 90% confidence levels are provided in Table 1.

Due to continuing process improvements and advances in device and package technologies, the failure rate of semiconductor devices is extremely low. To accurately assess the reliability of these devices, reliability engineers routinely use accelerated stress test conditions during reliability testing. These test conditions are carefully chosen to accelerate the failure mechanisms that are expected to occur under normal use conditions without introducing spurious failure mechanisms. Accelerated stress testing is used to provide estimates of device reliability performance under use conditions, and to assist in identifying opportunities for improving the reliability performance of the device. Failure mechanisms found during stress testing are traced to the root cause and eliminated, whenever possible.

The most commonly used stress accelerator is temperature. In most cases, elevated temperature increases the rate at which a given failure mechanism progresses. There are a few failure mechanisms that are accelerated by using lower temperatures. The simplest thermal acceleration model is the Arrhenius equation:

where:

\[ \text{Rate} = A_0 e^{\frac{E_a}{T}} \]

Rate = rate of progress for a given failure mechanism

A0 = pre-exponential factor that is characteristic of the given failure mechanism s-1
Ea = Thermal activation energy of the failure mechanism in eV
k = Boltzman constant, 8.617 \times 10^{-5} \text{ eV/K}
T = device junction temperature in degrees Kelvin

Using the Arrhenius equation, one can relate the failure rate at one stress condition to the failure rate at a different condition. The acceleration factor \( A_f \) is defined in the following manner:

\[
A_f = \frac{\text{Rate (Condition 1)}}{\text{Rate (Condition 2)}}
\]

where:

\( \text{Rate (Condition 1)} \) = rate of progress for a given failure mechanism at Condition 1 (i.e., \( T_1 \))
\( \text{Rate (Condition 2)} \) = rate of progress for a given failure mechanism at Condition 2 (i.e., \( T_2 \))

The thermal acceleration factor becomes:

\[
A_f = e^{\frac{E_a}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right)}
\]

where:

\( T_1 \) and \( T_2 \) = device junction temperatures at stress conditions 1 and 2, respectively.

See Figure 1 for an example of how the acceleration factor is used to transform the stress testing time into the equivalent time at a typical use junction temperature.

**ACTIVATION ENERGY**

ON Semiconductor uses the industry-standard estimates for activation energies that are documented in JEDEC Publication JEP122, “Failure Mechanisms and Models for Silicon Semiconductor Devices.” The following table summarizes the most commonly used activation energies.
<table>
<thead>
<tr>
<th>Device Association</th>
<th>Failure Mechanism</th>
<th>Accelerating Failures</th>
<th>Typical Activation Energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Surface Oxide</td>
<td>Surface Inversion</td>
<td>T, V</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>Mobile Ions</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charge Accumulation</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Surface Charge Spreading</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>Gate Oxide</td>
<td>Dielectric Breakdown</td>
<td>E, T</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>Thin Oxide (&lt; 40 nm)</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thick Oxide (≥ 40 nm)</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>Metallization</td>
<td>Electromigration</td>
<td>J, T</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pure Al</td>
<td>0.48</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AISI (≤ 1.5%)</td>
<td>0.50</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AISI (1.5%)</td>
<td>0.72</td>
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<tr>
<td></td>
<td>AlCu (0.5%)</td>
<td>0.70</td>
<td></td>
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<tr>
<td></td>
<td>AlCuSi (1% Si, 2% Cu)</td>
<td>0.70</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AlCu over TiW (≥ 1%)</td>
<td>0.71</td>
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<tr>
<td>Corrosion</td>
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<td>H, E/V, T, V</td>
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<tr>
<td></td>
<td>General</td>
<td>0.8</td>
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<tr>
<td></td>
<td>With Chlorine</td>
<td>0.7</td>
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</tr>
<tr>
<td></td>
<td>With Phosphorus</td>
<td>0.53</td>
<td></td>
</tr>
<tr>
<td>Assembly Process</td>
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<td>T</td>
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</tr>
<tr>
<td></td>
<td>Intermetallics</td>
<td></td>
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<tr>
<td></td>
<td>Bromine-induced</td>
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<tr>
<td></td>
<td>Halide-induced</td>
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<tr>
<td></td>
<td>Chloride-induced</td>
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<tr>
<td></td>
<td>Wire Bond</td>
<td>T, ΔT</td>
<td>0.75</td>
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<tr>
<td></td>
<td>Die Attach</td>
<td>T, ΔT</td>
<td>0.30</td>
</tr>
</tbody>
</table>

T = Temperature, ΔT = Temperature Cycling, V = Voltage, E = Electric Field, J - Current Density, H = Humidity

### THERMAL RESISTANCE

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the junction temperatures low.

Electrical power dissipated in any semiconductor device is a source of heat. This heat source increases the temperature of the die about some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction depends on the packaging and mounting system’s ability to remove heat generated in the circuit from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

\[
T_J = T_A + P_D (\bar{R}_{JC} + \bar{R}_{CA})
\]

or:

\[
T_J = T_A + P_D (\bar{R}_{JA})
\]

where:
- \(T_J\) = maximum junction temperature
- \(T_A\) = maximum ambient temperature
- \(P_D\) = calculated maximum power dissipation, including effects of external loads when applicable
- \(\bar{R}_{JC}\) = average thermal resistance, junction-to-case
- \(\bar{R}_{CA}\) = average thermal resistance, case-to-ambient
- \(\bar{R}_{JA}\) = average thermal resistance, junction-to-ambient

Only two terms on the right side of equation (1) can be varied by the user, the ambient temperature and the device case-to-ambient thermal resistance, \(\bar{R}_{CA}\). (To some extent, the device power dissipation can also be controlled, but under recommended use the supply voltage and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the \(\bar{R}_{CA}\) thermal resistance term. \(\bar{R}_{CA}\) is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature controlled heat sink, the estimated junction temperature is calculated by:

\[
T_J = T_C + P_D (\bar{R}_{JC})
\]

where \(T_C\) = maximum case temperature and the other parameters are as previously defined.

### AIR FLOW

Air flow over the packages (due to a decrease in \(\bar{R}_{CA}\)) reduces the thermal resistance of the package, therefore, permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature. For thermal resistance values for specific packages, see the product data sheet, or contact your local ON Semiconductor sales office.
ON Semiconductor is committed to delivering superior quality products to our valued customers and providing cost effective solutions. This commitment to continuous improvement in quality and value requires us to periodically make changes to our product portfolio. These changes are handled in accordance with ON Semiconductor’s change management system, described below, which is compliant to all international quality system standards such as ISO 9001, IATF16949, AS-9100, Mil-PRF-38535, J-STD-046, J-STD-048, and mutually agreed Customer Specific Requirements.

Along with our commitment to quality and value, ON Semiconductor manages necessary product changes with a rigorous evaluation and characterization methodology to make them fully “transparent” to our valued customers from an electrical, physical, and thermal performance standpoint.

Change Management Overview

All proposed changes are classified in one of three classes, as determined by the nature and scope of the proposed change. The classification level indicates the level of qualification testing and customer notification required. The classification level is assigned by the corporate Business Change Action Board (BU CAB), which is an independent body chartered to represent the customer’s best interests with representatives from Quality & Reliability, the Business Units, Engineering and Manufacturing. Prior to submittal for Business Change Action Board review, the local manufacturing engineering reviews and approves any potential changes first in the Manufacturing Change Action Board (Mfg CAB). This two-tiered requirement for review and approval is intended to provide thorough analysis of all changes for proper evaluation and risk mitigation.

**Level 1** changes include any minor change to the materials, process method, process equipment or design, which has no effect on the visual appearance, external dimensions and tolerances, or performance of the finished product. Level 1 changes do not require reliability testing or customer notification, but do require product characterization prior to implementation.

**Level 2** changes include any substantial change to the materials, process method, process equipment or design, which has no effect on the external dimensions and tolerances or performance of the finished product. Level 2 changes may have an effect on the visual appearance if the difference is purely cosmetic in nature and does not impact customer usage of the product. Level 2 changes require product characterization and reliability testing but do not require customer notification prior to implementation.

**Level 3** changes include any substantial change to the materials, process method, process equipment or design, which do affect the visual appearance, external dimensions and tolerances, or performance of the finished product (also called ‘major changes’ in standard J-STD-046). Level 3 changes also include the transfer of existing wafer fabrication or assembly processes to a new manufacturing site. Level 3 changes require both product characterization and reliability testing, and are communicated to customers.

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**Diagram:**

- **Classify change level & prepare qualification plan**
- **Manufacturing Change Action Board Review**
- **Carry out qualification plan**
- **Implement change**
- **ON Semiconductor**
- **Customer**
- **Provide Feedback**
- **Request Samples/Data**
- **Provide Initial PCN**
- **Provide Final PCN (PPAP)**
- **Provide Samples**

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ON Semiconductor’s Change Management Policy is to inform customers about Level 3 product and/or process changes in as many as three stages of communication.

**Initial Product/Process Change Notification (IPCN)** This “Initial Notification” is the first, formal notification distributed to customers. The IPCN is optional and gets typically distributed 30 days prior to the publication of the final PCN. The IPCN contains the qualification plan which must be completed prior to implementation, which gives our valued customers the opportunity to request any additional testing they might require in order to approve the change. The content of the qualification plan is dependent on the nature and scope of the change, but in all cases must be in compliance with applicable JEDEC and AEC standards.

**Final Product/Process Change Notification (FPCN)** This ‘Final Notification’ completes the notification process. The FPCN must be distributed at least 90 days prior to the effective date of the change, or can be implemented earlier when approved by the customer. The FPCN must contain successful results of all characterization and reliability testing documented in the qualification plan. Prior to issuance of the FPCN the characterization and reliability data is again reviewed and approved by both the internal Manufacturing and Business Change Action Boards. The 90-day advance notification provides our valued customers with a final opportunity to communicate any additional requirements to accept the change prior to implementation if necessary. The PCN notification process and format is compliant to J-STD-046.

**Product Discontinuance (PD)** is a special type of Notification when the product/process goes to end-of-life. The Product Discontinuance is distributed to customers 6 months for a last purchase (Last Time Buy) and another 6 months for last shipments. The Product Discontinuance process is compliant to J-STD-048.

**Process Change Management Portal** The customer will receive an email notification with hyperlinks to the PCN document and a customized list of the customer’s affected part numbers. Customers should acknowledge receipt of the PCN within 30 days of delivery of the Notification. Acknowledgement is done by opening the hyperlink in the PCN document. Lack of acknowledgement of the Notification within 30 days constitutes acceptance of the change. Published notifications for standard products are accessible by everyone on the ON Semiconductor external website PCN page. Company-specific (customized) notifications can be retrieved from ON Semiconductor’s external website, but require a login.

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**Section 5 – Supplier Quality Process**

ON Semiconductor follows a five step Supplier Development process to improve the quality of goods and services delivered by our suppliers. The five steps of the process are: Planning, Implementation, Measurement, Improvement, and Recognition & Award.

During the Planning phase we establish general expectations of doing business with ON Semiconductor, and make our supplier selection based on their Quality System, Technical Capability, Value Added Services, Cost, Capacity, etc. Suppliers are requested to perform a Quality System self-evaluation to VDA6.3 requirements.

Once a potential supplier has been selected they must pass our qualification process prior to making any production shipments; this is the Implementation step of our Supplier Development Process. In order to pass our qualification requirements suppliers must provide samples and data which demonstrates their product conforms to our specifications as well as their ability to manufacture the product consistently. This process will include a review of First Article Inspection data, Process Control and Measurement System Analysis data, and an on-site audit by ON Semiconductor (for new suppliers). Any significant process changes made by the supplier go through the same qualification process described above, and are managed through our CAB process.
Once a supplier has been qualified we enter into the Measurement stage. The material we use in production is verified in one of three ways prior to use in production, the three methods are: Inspection, Audits combined with measurement of acceptable performance, and/or receipt & review of SPC data. If it is determined that material has been received that is non-conforming to our specified requirements we utilize our automated corrective action tracking system to ensure suppliers respond to the problem using an 8D corrective action. On a quarterly basis we measure our supplier’s performance in the areas of Quality, Cost, Delivery, Service and Technology. This data is shared with our suppliers both by email as well as during Business Review Meetings. We also have an ongoing supplier assessment process (to VDA6.3 requirements) which is prioritized based on their certification status and ongoing performance as measured by our rating system.

In the Improvement stage we establish goals with our suppliers using our Supplier Goal Plan (SGP) Process. This enables us to clearly define priorities for our suppliers, and provides us with a method to follow-up and verifies suppliers are meeting our goals. The SGP is reviewed with suppliers during Business Review meetings.

ON Semiconductor understands the value of recognizing and awarding suppliers for their hard work and dedication. We believe that by recognizing our best suppliers for their superb performance we are setting a standard for all our suppliers to achieve. This is the final step in our Supplier Development Process; Recognition and Award.

Section 6 – Failure Analysis

Overview

Failure analysis is a process which entails vast analytical methods and techniques to solve the reliability and quality issues that may occur in either the manufacturing or application of our products. The process can be a rather complicated endeavor due to the many aspects associated with the ever advancing semiconductor and packaging technologies and the numerous engineering disciplines involved. The failure analyst must be proficient in design, process, assembly, test, and applications, which equates to electrical, physics, chemical, and mechanical engineering.

Failure analysis laboratories are available globally at all ON Semiconductor manufacturing sites. These same analytical tools are proactively utilized for good unit analysis, process characterization, destructive physical analysis, construction analysis, and even competitive benchmarking studies. Tool development for failure analysis is advancing at a similar rate as that of manufacturing. For the labs to stay current with technology, the analyst must be continually developing the associated tools and techniques. As the die features are shrinking and become covered with multiple layers of interconnects, the requirements for failure analysis needs to be anticipated as early as the design cycle. By incorporating these specialized test structures and functional test coverage, problems can more easily be diagnosed. In addition to tools, trained personnel, techniques, and procedures, an adequate database and tracking system should be employed to assist in expeditious problem solving.

At ON Semiconductor, the labs are equipped in a diverse range of instrumentation and engineering expertise to solve problems in all aspects of semiconductor and packaging analysis. The success of failure analysis is not only in a superior instrumentation set, but in its people and their approach to problem solving. While the failure analysis lab may be able to identify a failure mechanism, the road to root cause is just embarked upon. Depending on the manufacturing process complexity, root cause analysis may entail extensive experimentation and designed experiments to not only identify the root cause but to also verify potential corrective action effectiveness. The full process of problem solving entails multiple labs and techniques. These analytical professionals along with the subject matter experts, such as design or manufacturing, work in unison to solve the problem.

Generic Process Steps

The full sequence of the problem solving events is outlined in Section 9, Customer Returns. The following steps outline the basic procedures that a typical field return may be subjected to within the failure analysis lab.

Required Information

The more information the better! There is a minimum set of background information that greatly impacts the overall quality and cycle time of the problem solving process. The minimum set and some questions are as follows:

1. Failure history and failure rate at the customer site, in either this application or other products. Is this a new product or have any changes occurred in this time frame?
2. Length of time in application and the conditions upon failure should be included. Did any other components fail at the same time and if so, how did they fail? Can a schematic be sent? Are there any devices of this same date code still available?
3. What is the failure mode of the application and how can it be related to this device? How do you perceive that the device is failing (short, open, stuck logic levels, etc.)?

4. How was the device handled prior to receipt at ON Semiconductor? Precautions should be taken in the removal and handling (ESD/thermal) of the devices to insure that electrical or physical damage does not occur and testability of the package is maintained.

Receipt of Request
When the product is received in the failure analysis lab, the devices have generally been confirmed as failures through the use of automatic test equipment to achieve rapid failure verification by our customer support group. At this point, the background documentation, electrical results and historical failure data are reviewed to outline the appropriate course of analytical action. An external visual inspection is carried out, documenting the package’s physical condition and markings.

Diagnostic Testing
The devices would most likely be subjected to a benign “pin-to-pin” test which quickly identifies parametric anomalies as compared to known good units. Depending on the failure mode, the device may be subjected to a more extensive bench test with stress conditions applied to match the customer’s application or to stimulate the mechanism.

Non-destructive Testing
Failure analysis in itself is reverse engineering and in this vein, destructive in nature to the returned product. Since the package will be at least partially destroyed to expose the die, non-destructive techniques are carried out first to observe package or assembly related mechanisms. The most common techniques used are acoustic microscopy and radiographic (XRAY) inspections to look for internal assembly or molding anomalies.

Storage Bakes or Stress
Depending on the failure mode, the analyst may subject the device to a series of vacuum or storage bakes to observe parametric or functional shifts. If the original failure mode was not confirmed, stress testing (high temperature bias for instance), may be carried out to observe possible longer-term reliability concerns.

Decapsulation or Package Preparation
The general course of action at this point is to reveal the die surface. In the case of a plastic encapsulated component, this would entail a chemical decapsulation. There are however, many methods utilized for decapsulation or package preparation, dependent on the package, failure mode, and potential failure mechanism.

Internal Inspection
An internal optical inspection would then be carried out to check for any obvious assembly anomalies or wafer fabrication issues. If possible re-testing is recommended at this point to insure that the failure mode has not changed.

Internal Diagnostic Testing
In many cases, the internal inspection will not reveal an obvious failure mechanism. At this point, depending on the technology and level of testability, the lab would utilize one or more of the techniques available to isolate the failure site. This could entail extensive probing or a technique, such as thermography or photoemission, to highlight potential anomalies. The majority of these techniques are attempting to observe the properties of the failure site, as in thermal dissipation or photon emission. From a probing standpoint, the use of navigational tools, a laser cutter or Focused Ion Beam (FIB) may be employed to assist in device and circuit isolation.

Deprocessing
Deprocessing is an iterative process of removing layer of the die, which may entail both wet chemistry and dry plasma etching techniques to reveal the underlying structures. The proper techniques are critical at these steps due to the destructive nature of the process and the potential loss of vital information.

Analysis of Failure Site
Once a potential site has been determined or revealed, further documentation and analysis may be conducted. Further analytical techniques are employed depending on whether the morphology or material composition is required.

Report Conclusion
Upon completion of the analysis, a written report is generated documenting the work. The report should state the relationship of the physical anomaly to the failure mode. It should also include sufficient documentation for root cause analysis by the manufacturing site if warranted.

Summary
The cost of failure analysis is high due to the extensive instrumentation, highly technical staff, continual training and development, and associated analysis expenses (chemicals, fixtures, etc.). To enable the most efficient utilization of these resources, it is essential that the background documentation (see Required Information on the previous page) be complete upon receipt and that an open communication channel between ON Semiconductor and our customers exists. This will insure a timely resolution of the problem on either end.
Section 7 – Reliability Data Summary

ON Semiconductor performs extensive reliability stress testing on devices that span the full breadth of our product portfolio. Reliability data is collected as part of the ON Semiconductor Reliability Audit Program, and as part of the normal product qualification and re-qualification process. This data is periodically updated to include the most recent test results. The data is typically updated on a quarterly basis. The current data can always be located through the reliability data links on the ON Semiconductor website Reliability page.

The reliability data is presented in two parts:
1. Life Test Data that groups the data by business unit and product family or technology. This data provides information that pertains primarily to die design- and wafer fabrication-related failure mechanisms.
2. Package Test Data that groups the data by package case outline and product family or technology. This data provides information that pertains primarily to package design- and assembly process-related failure mechanisms.

The ON Semiconductor package outline reference is also included to make it easier to identify a specific case outline.

Section 8 – External Manufacturing Quality

ON Semiconductor utilizes packaging and testing subcontractor, foundry or external wafer fabrication manufacturer and joint venture partners to support our customers’ increasing requirements for high quality, low cost semiconductors. Our global subcontractor, foundry and joint venture partners perform some or all areas of semiconductor manufacturing. This includes wafer fabrication, wafer probe, assembly, test, as well as product analysis, and reliability testing. When ON Semiconductor selects new manufacturing subcontractors and foundries, this requires an extensive review of the company’s ability to meet our high quality, business and technical requirements. For current manufacturing partners, continuous improvement plans are required which outline aggressive improvement goals. Progress to these goals is periodically reviewed.

The new product introduction and process change control requirements and specifications are the same for internal ON Semiconductor factories as well as our external manufacturing partners. Quality systems vary from subcontractor to subcontractor and foundry to foundry; however,

ON Semiconductor requires each supplier to manufacture our products with the same high standards as our internal factories. Prior to engaging with a subcontractor as a new supplier or when adding a new or expanded manufacturing line, ON Semiconductor performs an extensive assessment. This includes a review of the machine capability and maintenance, process documentation and control, training and certification of personnel, FMEA’s, as well as many other areas. Detailed project management methodology is utilized to drive projects to a timely completion.

ON Semiconductor encourages each subcontractor and foundry to pursue outside certification to drive their quality system improvements.

Additionally, we drive many of our internal factories quality system practices into our external partners. Periodic subcontractor and foundry reviews are held to review progress to key metrics including customer quality and delivery. Joint corrective action plans are agreed upon to drive resolution and continuous improvements.
Section 9 – Customer Returns

ON Semiconductor’s Global Customer Return or Incident process is focused on formal Problem Solving and Responsiveness. We use the 8D Problem Solving Methodology to determine Containment, Root Cause, and Corrective/Preventive Actions.

The Eight Disciplines are:

D1 - Establish the Team - Establish a cross functional team of people with the process/product knowledge to solve the problem.

D2 - Describe the Problem - Specify the customer’s problem by identifying in quantifiable terms the who, what, where, why, how, and how many, for the problem.

D3 - Implement and Verify Containment - Define and Implement containment actions to isolate the effect of the problem from customers until the corrective actions are implemented.

D4 - Define and Verify Root Cause - Identify all potential causes that could explain why the problem occurred and how it escaped our testing. Isolate and verify root cause by testing each potential cause against the problem description.

D5 - Choose and Verify Permanent Corrective Action - Identify all potential corrective actions for the Occur and Escape Root Causes. Verify which actions will correct the root cause.

D6 - Implement Permanent Corrective Action - Provide action plans for implementation of the verified corrective actions. Follow up on any outstanding actions.

D7 - Prevent Recurrence - Implement actions to address the “system” failure. Update control plans, FMEA specifications, process specifications. Fan-Out Corrective Actions to appropriate manufacturing sites, and other Technologies.

D8 - Congratulate the Team - We communicate to the customer throughout the process.

Customer Incident Process Map

Customer Incidents are tracked in our Customer Incident information system. Monthly customer incident metrics are compiled and distributed corporate-wide. Responsiveness metrics are used to drive continuous improvement in the Cycle Time arena. Failure Mechanism paretos are used to drive continuous improvement in the Product and Administrative Quality arenas. These metrics are also reviewed in our monthly Business Unit & Manufacturing Operations Reviews.
Section 10 – New Product Development

ON Semiconductor is using a phase/gate approach (aka Advanced Product Quality Planning - APQP) for New Product Development, as shown in figure below. The major project milestones and phase-gates provide points where the project undergoes a formal review of all deliverables required for that phase. The following design and development phases (gates) are determined for the NPD process:

- Concept (Concept Commit gate),
- Plan (Plan Commit gate),
- Develop (Develop Complete gate),
- Qualify (Qualify Complete gate),
- Launch (Launch Complete gate).

The Sustain and Retire are phases of the Product Life Cycle, but extend beyond, and are not part of NPD.

The Concept Phase is the starting point for new product ideas (proposals), and their associated business opportunity. The primary activity that occurs during the Concept Phase is the analysis of the NPD opportunity from both a technical feasibility and a business viability point of view.

The Plan Phase validates the assumptions made during Concept Phase on scope, schedule and cost. Identified discrepancies with customer expectations must be resolved by the end of this phase. This phase includes the creation of the Project Plan, the Verification and Validation (Qualification) plans, and the Product Technical Specification. For automotive projects, a Design Failure-Mode-Effects-Analysis (DFMEA) is being initiated in accordance to the AIAG standard to identify, document, assess, and manage the project risks. Additionally for automotive, the Production Part Approval Process (PPAP) level is determined.

The Develop Phase encapsulates the execution of the main design and development activities for the new product in accordance with the product requirements and the project plan. This may include silicon design, layout, test, hardware or software design and development, or package development as identified in the Project Plan. Design and development verification and validations are being performed in accordance with planned arrangements to ensure that the design and development outputs meet the design and development input requirements.

During the Qualify phase, the design and development validation gets completed, including Reliability tests (see section 3), product approval, and ensuring product readiness for Manufacturing, Supply Chain, Sales and Marketing. For automotive products, this is the phase where the PPAP is completed.

The purpose of the Launch Phase is to demonstrate that the product can be delivered in high volume with conditions that are acceptable for both ON Semiconductor (cost, manufacturability) and the customer (quality/reliability, volume).

The Product Discontinuance takes place in the Retire Phase of the product life cycle. This is controlled by the Product Discontinuance notice as described in section ‘Customer Process Change Notification’.
Section 11 – ISO 26262 Automotive Functional Safety

A dedicated organization has been defined to enhance the safety culture within the company and to integrate the ISO 26262 requirements in our existing development flow. Refer to diagram below. Those requirements supplement our current Quality Management System that is based on ISO 9001 and IATF16949.

ISO 26262 is an adaptation of IEC 61508 for the automotive industry. The first edition of the standard was released in November 2011. Since then, ISO 26262 has become the state of the art and is now widely used in the development of automotive safety related integrated circuits.

ISO 26262 is focused on the Functional Safety (absence of unreasonable risk) in passenger vehicles and addresses possible hazards caused by the malfunctioning behavior of electrical and/ or electronic (E/E) systems installed in those vehicles. This means that the standard is not only applicable to the system itself, but also to the elements that are composing the system. The elements are characterized by their Automotive Safety Integrated Level (ASIL). ASIL levels range from A to D, with ASIL D being the most stringent.

ISO 26262 includes 10 parts and approximately 750 clauses dealing with each part of the product lifecycle, from project management, to product development, through production, and ending with decommissioning. Not all of the requirements from the standard are applicable to the development of integrated circuits, as some of them only focus on the system level development and on safety analysis (see diagram below).

The main requirements brought by ISO 26262 compared to the regular QMS are defined in Part 5 (Product Development Hardware), Part 8 (Supporting Processes) and Part 9 (ASIL oriented and safety-oriented analysis). They describe the hardware product development flow as well as the tools that are needed to develop safe products. These requirements are, for example, related to the specification of the hardware safety requirements, the definition of the safety mechanisms, and the execution of the safety analysis (e.g. Failure Modes Effects and Diagnostic Analysis (MEDA), Fault Tree Analysis (FTA)).

ON Semiconductor is an active member of the ISO 26262 task force and part of the semiconductor sub-workgroup.
Section 12 – Storage and Preservation

ON Semiconductor adheres in the proper storage and preservation of semiconductors in order to prevent damage or deterioration and ensure on-time delivery of superior quality products to our valued customers. The standard storage and preservation guidelines are tabulated below and followed by all ON Semiconductor manufacturing sites including subcontractors and distribution centers.

The storage durations are monitored in our Supply Chain and Finance information systems. These are tracked on a monthly basis to drive on-time delivery.

Table 3. Storage and Preservation*

<table>
<thead>
<tr>
<th>ON Semiconductor Product</th>
<th>Storage Condition</th>
<th>Storage Life</th>
</tr>
</thead>
<tbody>
<tr>
<td>Finished Wafer, Probe Wafer</td>
<td>Temperature 18-28°C, Humidity 30-65% RH</td>
<td>36 months after final wafer fab finish date</td>
</tr>
<tr>
<td>Die in Tray or Pocket Tape</td>
<td>Temperature 18-28°C, Humidity 30-65% RH</td>
<td>24 months after die singulation/sawing date</td>
</tr>
</tbody>
</table>
| Die in Surf Tape, Wafers in Foil/Tape     | Temperature 18-28°C, N2 storage or in vacuum moisture bag with desiccant and humidity card | 3 months after tape date  
                                          |                                                        | After 3 months quality of products needs to be validated |
| Finished/ Packaged Goods in tray. Tube or sealed in dry bag (MSL2 rated and above) | Temperature 8-30°C, Humidity 30-70% RH                | 24 months after assembly date |
| Finished/packaged Goods in Tray, Tube or sealed in dry bag (MSL1 rated) | Temperature 8-30°C, Humidity 30-70% RH                | 24 months after assembly date |
| Finished/Packaged Ceramics in Tray or Tube | Temperature 8-30°C, Humidity 30-70% RH                | 36 months after assembly date |

* Regular temperature monitor is needed to ensure no sudden changes in temperature that can result to moisture condensation during storage.

Section 13 – ON Semiconductor Corporate Social Responsibility and Sustainability

Corporate Social Responsibility Statement of Commitment

At ON Semiconductor, we are committed to the mission and principals of the Responsible Business Alliance (RBA), upholding the RBA Code of Conduct and following all applicable laws and regulations of those countries where we do business. We work together with our customers, peers, partners and suppliers to promote continual improvement in labor, environment, health and safety, ethics and management system standards within our operations and our supply chain. This includes proactively verifying compliance to the RBA Code of Conduct including the elimination of forced labor, slavery and human trafficking and conflict minerals as per our involvement with the Responsible Minerals Initiative (RMI).

We are proud of our commitment to the RBA along with the many other organizations and initiatives we support in relation to technological advances in sustainable energy, power conservation and corporate social responsibility. This commitment is deeply ingrained in our Core Values, policies, Code of Business Conduct and daily operations and allows us to be transparent and socially responsible toward our employees, suppliers, customers, and communities where we do business worldwide. Please see our Corporate Social Responsibility web page.

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