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November 2013

# FQPF5N40

# N-Channel QFET® MOSFET

**400 V, 3.0 A, 1.6** Ω

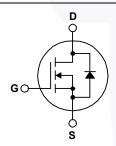
### **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

#### **Features**

- 3.0 A, 400 V,  $R_{DS(on)}$  = 1.6  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 1.5 A
- Low Gate Charge (Typ. 10 nC)
- · Low Crss (Typ. 7 pF)
- · 100% Avalanche Tested





# Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FQPF5N40	Unit
$V_{DSS}$	Drain-Source Voltage	400	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)	3.0	Α
	- Continuous (T <sub>C</sub> = 100°C)	1.9	Α
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	12	Α
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	290	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	3.0	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)	35	W
	- Derate Above 25°C	0.28	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

## **Thermal Characteristics**

Symbol	Parameter FQPF5N4			
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	3.57	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. 62.5		C/VV	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQPF5N40	FQPF5N40	TO-220F	Tube	N/A	N/A	50 units

## **Electrical Characteristics**

T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter Test Conditions		Min.	Тур.	Max.	Uni
Off Ch	avanto vintino					
	aracteristics	\\ -0\\   -250 ·· \	400	1		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		400			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.38		V/°C
DSS Zero Gate Voltage Drain Current	Zoro Coto Voltago Drain Current	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 320 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	aracteristics					•
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		1.27	1.6	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.5 A		2.8		S
C <sub>iss</sub>	ic Characteristics Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		350	460	pF
		v <sub>DS</sub> - 25 v, v <sub>GS</sub> - 0 v,				
Coss	Output Capacitance f = 1 MHz  Reverse Transfer Capacitance			60	80	pF
C <sub>rss</sub>				7	9	pF
Switch	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 200 V, I <sub>D</sub> = 4.5 A,		12	30	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25 \Omega$		60	130	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	116 20 32		20	50	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		30	70	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 320 V, I <sub>D</sub> = 4.5 A,	/	10	13	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		3.0		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		4.5		nC
	Source Diede Cheresteristics of	ad Maximum Datings		1		
ا <sub>S</sub>	Source Diode Characteristics and Maximum Ratings  Maximum Continuous Drain-Source Diode Forward Current				3.0	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				12	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage				1.5	V
		· · · · · · · · · · · · · · · · · ·				

# Q<sub>rr</sub>

 $t_{rr}$ 

Reverse Recovery Time

Reverse Recovery Charge

ns

μС

190

1.0

 $V_{GS} = 0 \text{ V}, I_{S} = 4.5 \text{ A},$ 

 $dI_F / dt = 100 A/\mu s$ 

<sup>1.</sup> Repetitive rating : pulse-width limited by maximum junction temperature.

<sup>2.</sup> L = 56 mH, I<sub>AS</sub> = 3.0 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.

<sup>3.</sup>  $I_{SD} \le$  4.5 A, di/dt  $\le$  200 A/ $\mu$ s,  $V_{DD} \le$  BV $_{DSS}$ , starting  $T_J$  = 25°C.

Essentially independent of operating temperature.

# **Typical Characteristics**

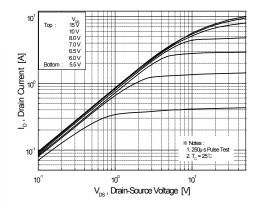


Figure 1. On-Region Characteristics

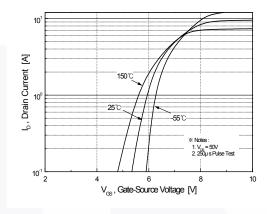


Figure 2. Transfer Characteristics

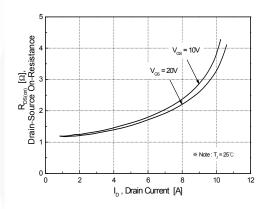


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

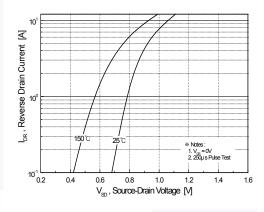


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

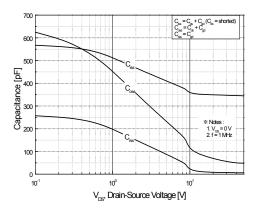


Figure 5. Capacitance Characteristics

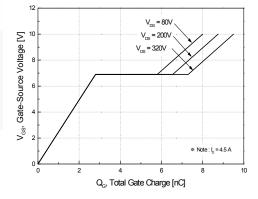


Figure 6. Gate Charge Characteristics

# Typical Characteristics (continued)

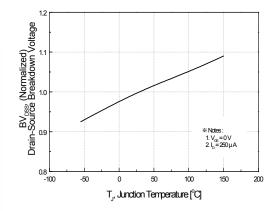
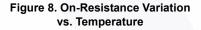
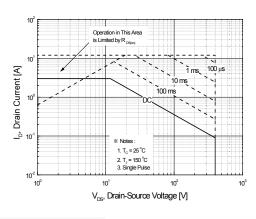


Figure 7. Breakdown Voltage Variation vs. Temperature





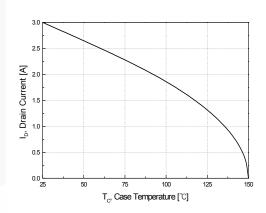


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

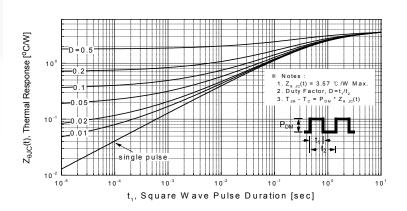


Figure 11. Transient Thermal Response Curve

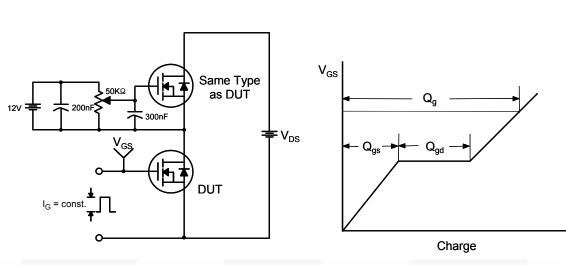


Figure 12. Gate Charge Test Circuit & Waveform

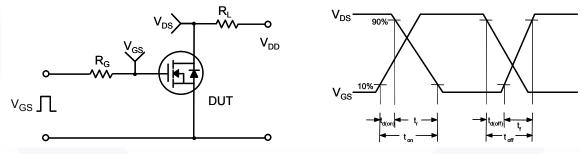


Figure 13. Resistive Switching Test Circuit & Waveforms

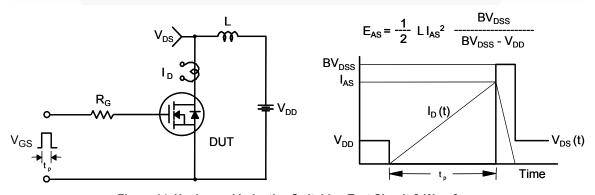
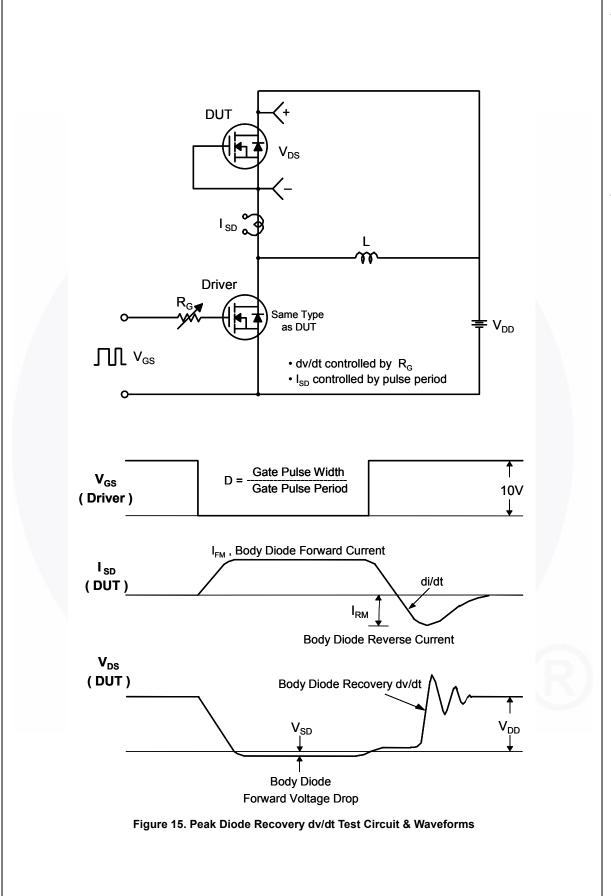


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



## **Mechanical Dimensions**

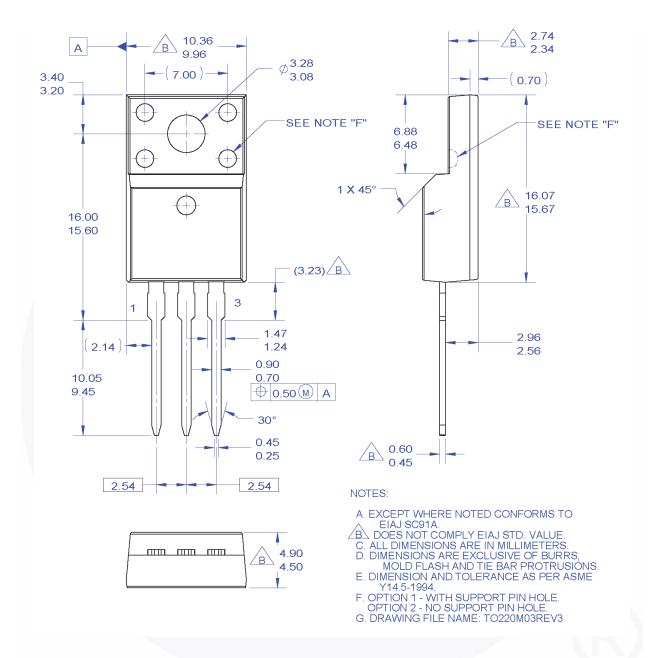


Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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