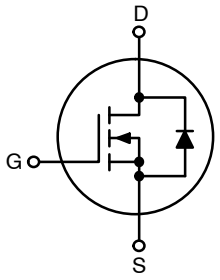
MOSFET – N-Channel, QFET

200 V, 19 A, 170 mΩ

FQP19N20C, FQPF19N20C

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
200 V	170 mΩ @ 10 V	19 A



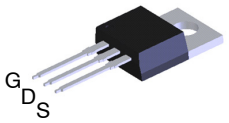
N−Channel MOSFET

Description

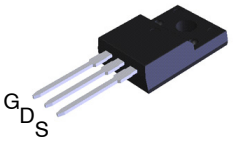
This N−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 19 A, 200 V, $R_{DS(on)}$ = 170 mΩ (Max) @ V_{GS} = 10 V, I_D = 9.5 A
- Low Gate Charge (Typ. 40.5 nC)
- Low C_{rss} (Typ. 85 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

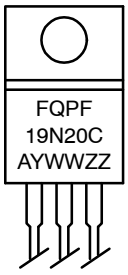


TO−220−3LD
CASE 340AT



TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT

MARKING DIAGRAM



FQP19N20C
FQPF19N20C = Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FQP19N20C	TO−220	1000 Units / Tube
FQPF19N20C	TO−200F	1000 Units / Tube

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FQP19N20C	FQPF19N20C	Unit
V_{DSS}	Drain to Source Voltage		200		V
I_D	Drain Current	– Continuous (T_C = 25°C)	19.0	19.0*	A
		– Continuous (T_C = 100°C)	12.1	12.1*	
I_{DM}	Drain Current	– Pulsed (Note 1)	76.0	76.0*	A
V_{GSS}	Gate to Source Voltage		±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		433		mJ
I_{AR}	Avalanche Current (Note 1)		19.0		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		13.9		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.5		V/ns
P_D	Power Dissipation	(T_C = 25°C)	139	43	W
		–Derate above 25°C	1.11	0.34	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 1.8 mH, I_{AS} = 19.0 V, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 19.0 A, di/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCP190N60	FCPF190N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.9	2.89	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	200	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.24	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 160 V, T_C = 125°C	–	–	100	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 9.5 A	–	0.14	0.17	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 9.5 A	–	10.8	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	830	1080	pF
C_{oss}	Output Capacitance		–	195	255	pF
C_{rss}	Reverse Transfer Capacitance		–	85	110	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 100 V, I_D = 19.0 A, R_G = 25 Ω (Note 4)	–	15	40	ns
t_r	Turn−On Rise Time		–	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		–	135	280	ns
t_f	Turn−Off Fall Time		–	115	240	ns
Q_g	Total Gate Charge	V_{DS} = 160 V, I_D = 19.0 A, V_{GS} = 10 V (Note 4)	–	40.5	53.0	nC
Q_{gs}	Gate−Source Charge		–	6.0	–	nC
Q_{gd}	Gate−Drain Charge		–	22.5	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	19.0	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	76.0	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 19.0 A	–	–	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 19.0 A, dI_F/dt = 100 A/μs	–	208	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.63	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature.

TYPICAL CHARACTERISTICS

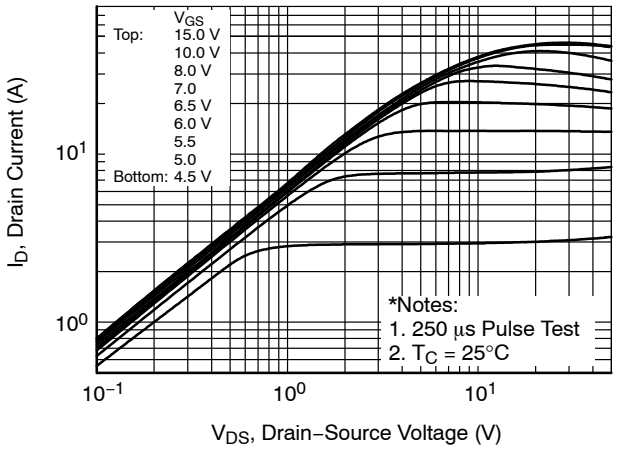


Figure 1. On−Region Characteristics

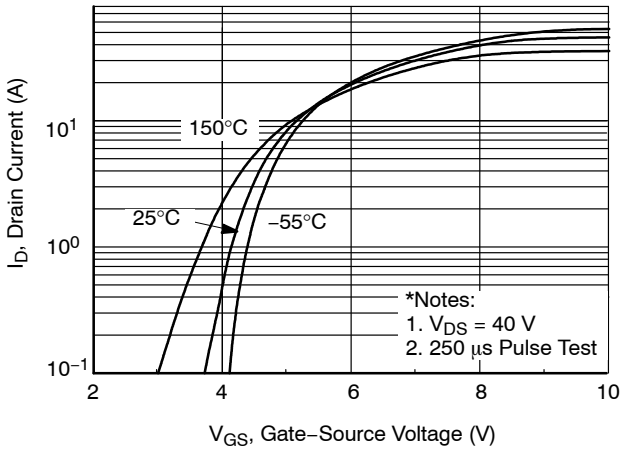


Figure 2. Transfer Characteristics

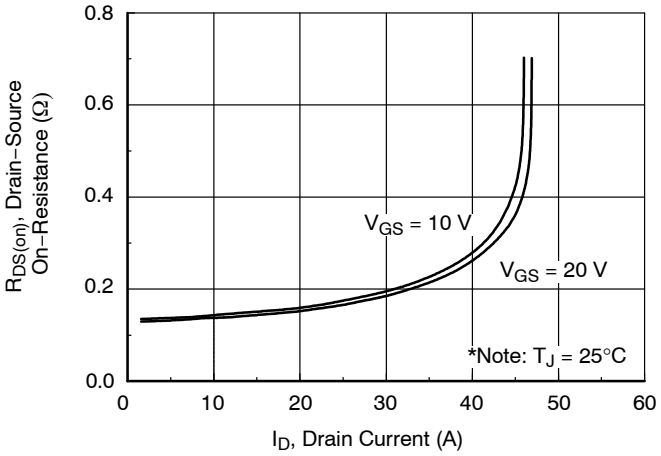


Figure 3. On−Resistance Variation vs Drain Current and Gate Voltage

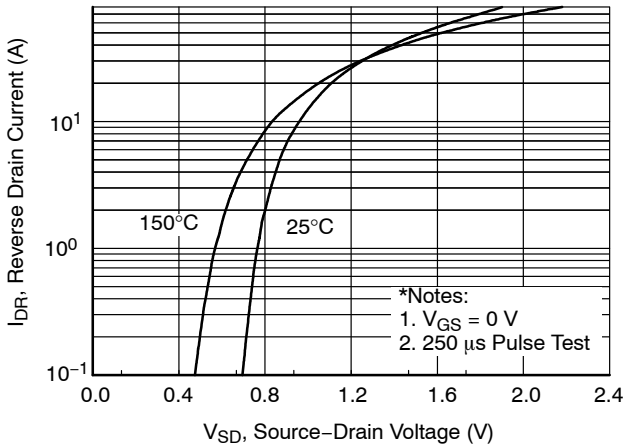


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

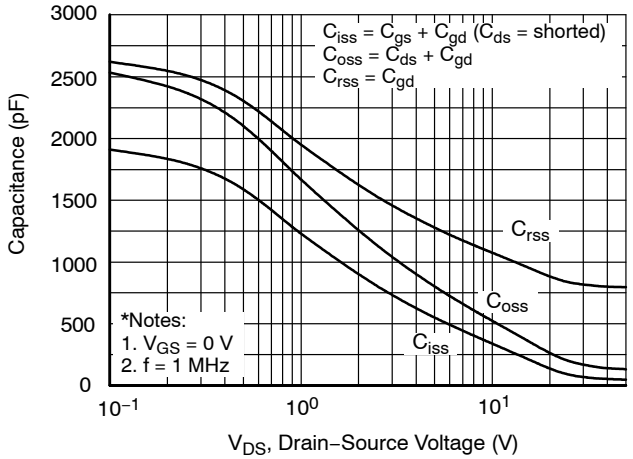


Figure 5. Capacitance Characteristics

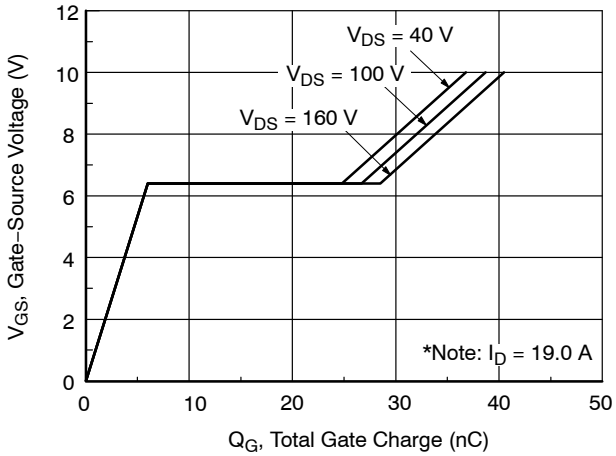


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

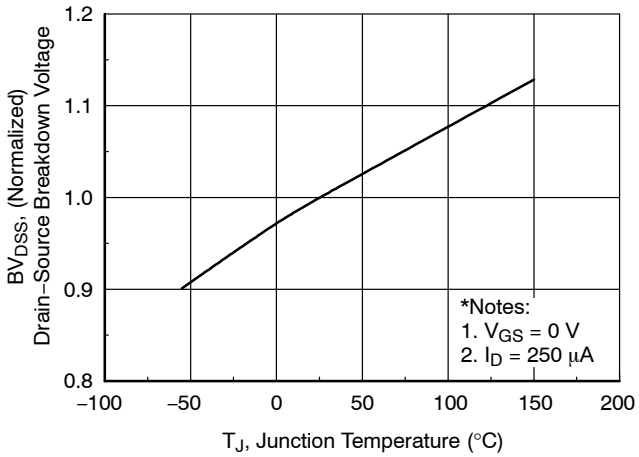


Figure 7. Breakdown Voltage Variation vs Temperature

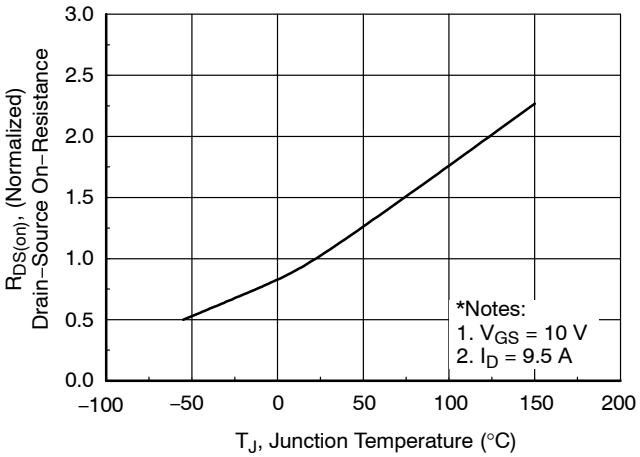


Figure 8. On−Resistance Variation vs Temperature

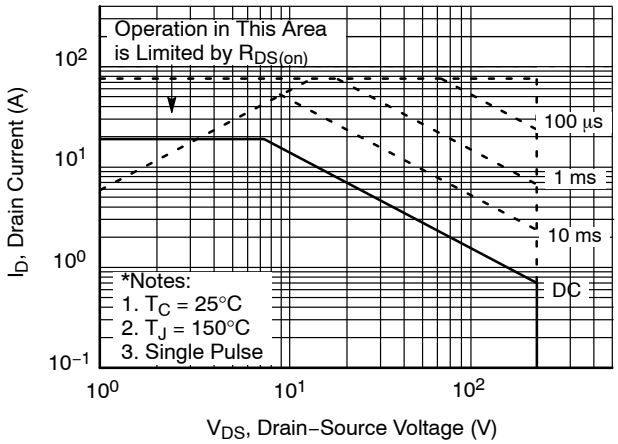


Figure 9.1. Maximum Safe Operating Area for FQP19N20C

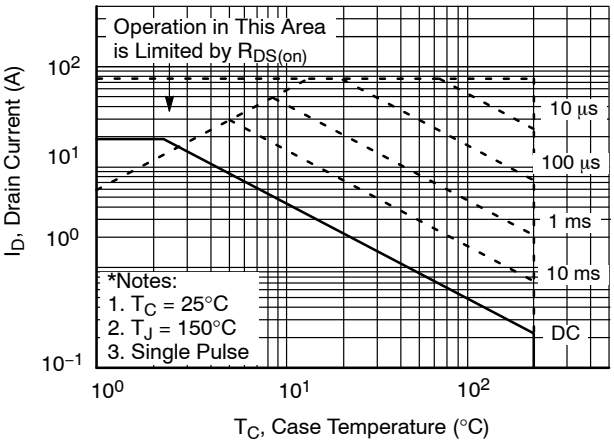


Figure 9.2. Maximum Safe Operating Area for FQPF19N20C

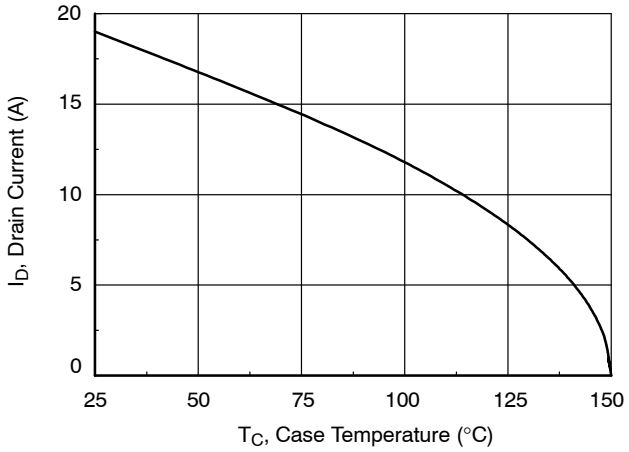


Figure 10. Maximum Drain Current vs Case Temperature

TYPICAL CHARACTERISTICS (continued)

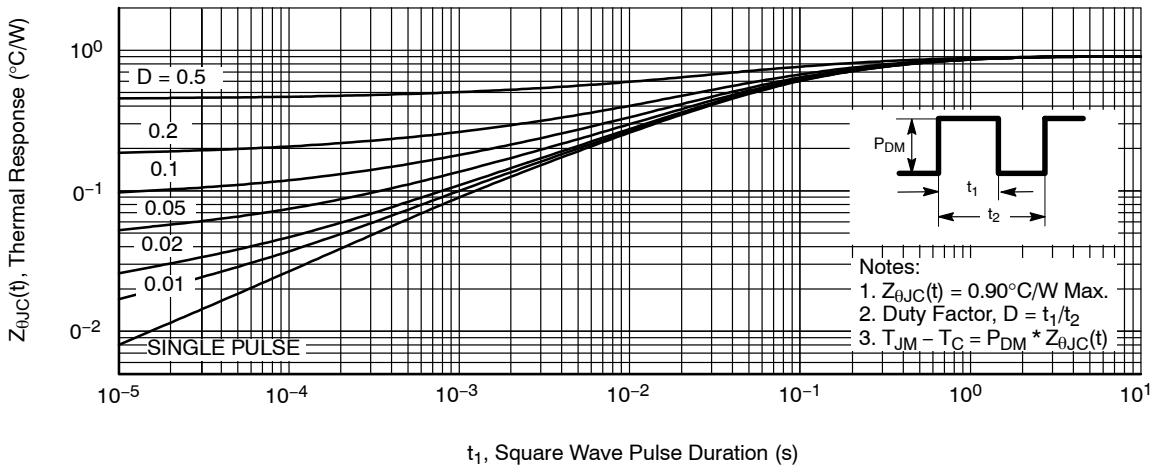


Figure 11.1. Transient Thermal Response Curve for FQP19N20C

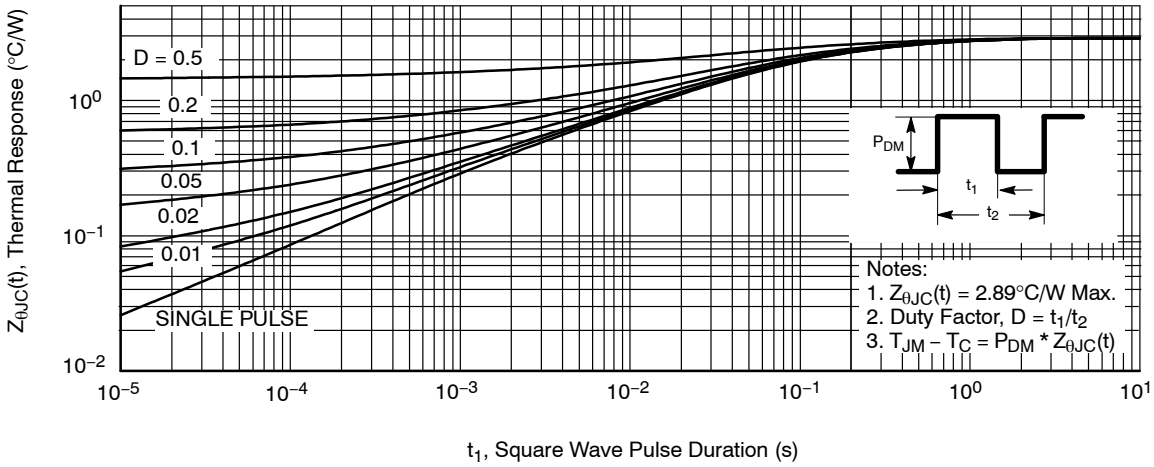


Figure 11.2. Transient Thermal Response Curve for FQPF19N20C

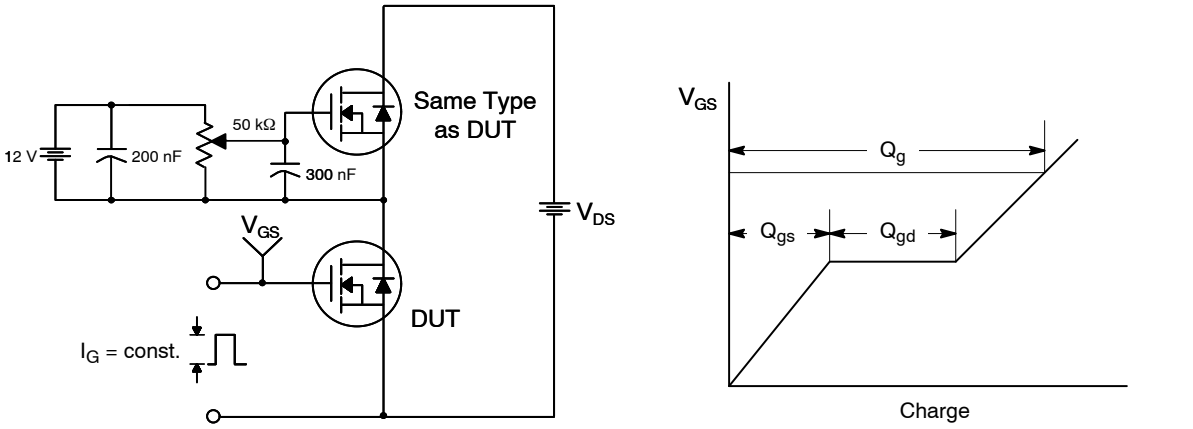


Figure 12. Gate Charge Test Circuit & Waveform

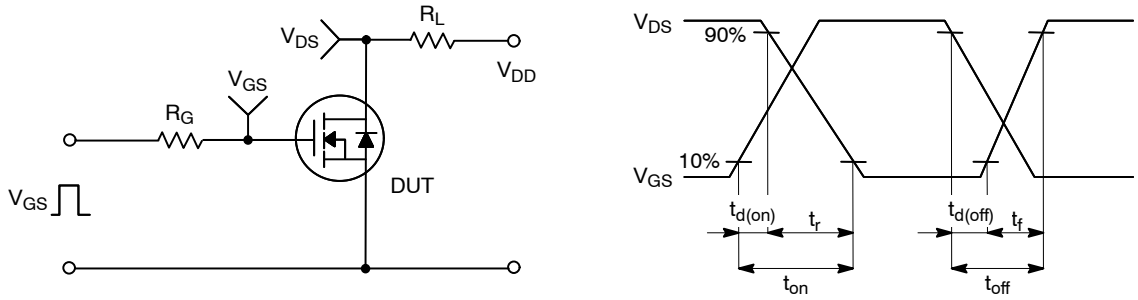


Figure 13. Resistive Switching Test Circuit & Waveforms

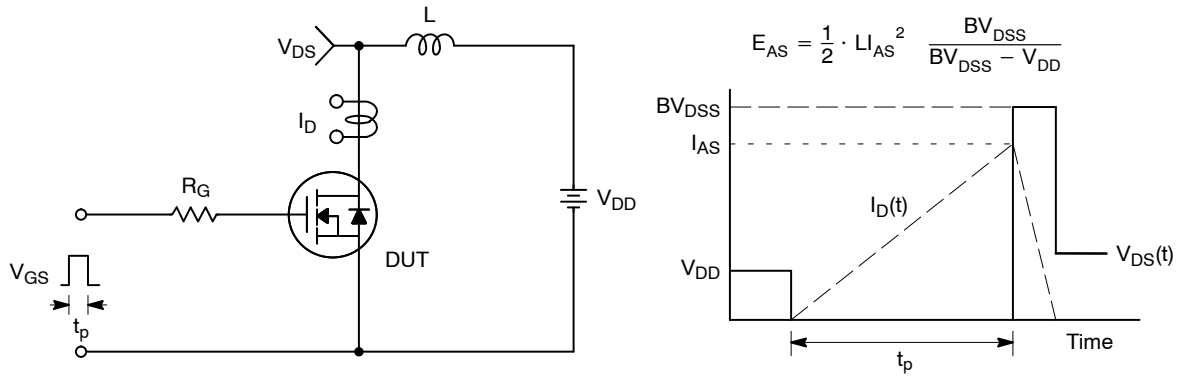


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

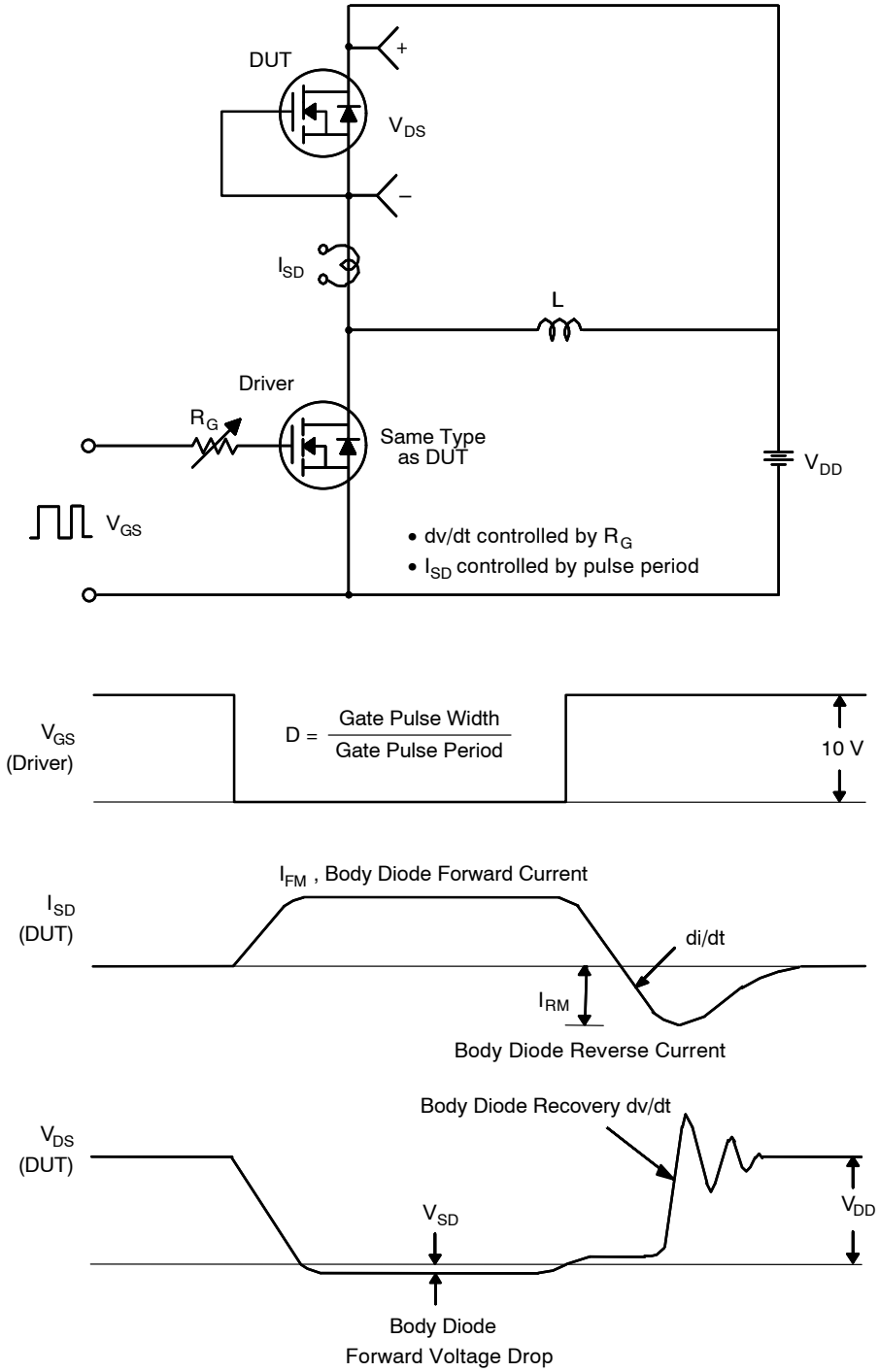
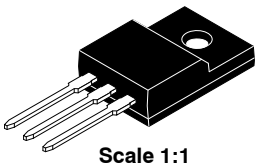


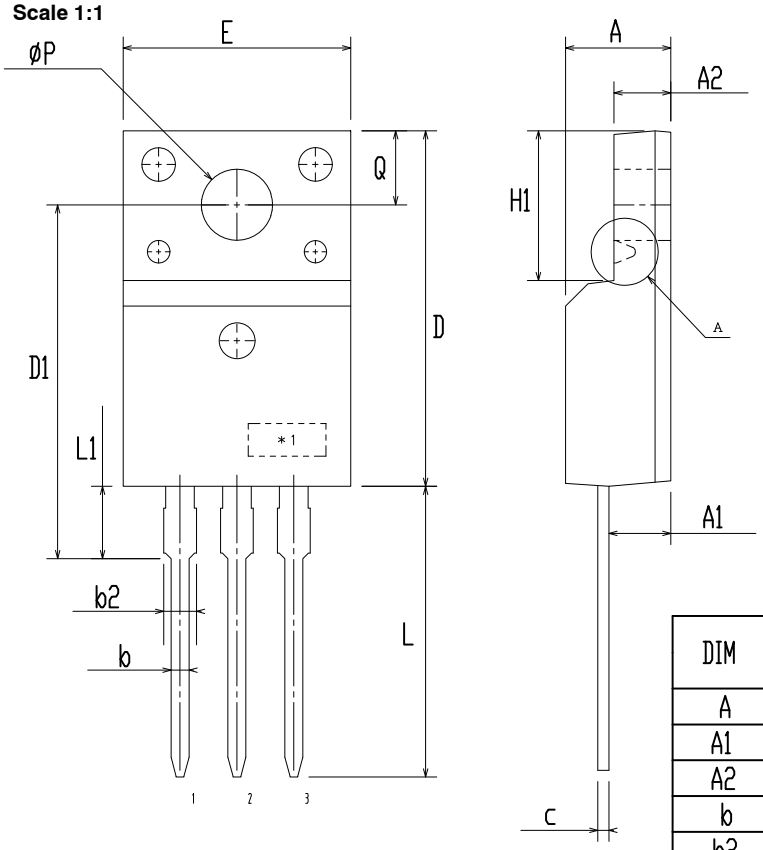
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

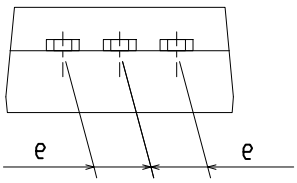
TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

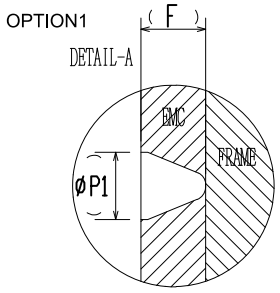
DATE 19 JAN 2021



Scale 1:1







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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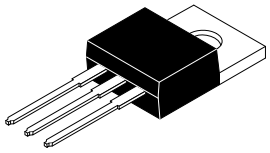
DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD / TO−220F−3SG**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

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