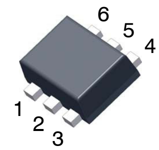
MOSFET – Dual, P-Channel (-1.5 V), Specified, POWERTRENCH®
–20 V, –0.83 A, 0.5 Ω

FDY1002PZ

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
−20 V	0.5 Ω @ −4.5 V	−0.83 A
	0.7 Ω @ −2.5 V	
	1.2 Ω @ −1.8 V	
	1.8 Ω @ −1.5 V	



SOT−563
CASE 419BH

General Description

These P−Channel Logic Level MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for all applications where small size is desireable but especially low cost DC/DC conversion in battery powered systems.

This Dual P−Channel MOSFET has been designed using **onsemi**'s advanced Power Trench process to optimize the $r_{DS(on)}$ @ V_{GS} = −1.5 V.

Features

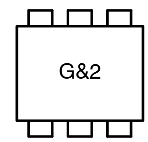
- Max $r_{DS(on)}$ = 0.5 Ω at V_{GS} = –4.5 V, I_D = –0.83 A
- Max $r_{DS(on)}$ = 0.7 Ω at V_{GS} = –2.5 V, I_D = –0.70 A
- Max $r_{DS(on)}$ = 1.2 Ω at V_{GS} = –1.8 V, I_D = –0.43 A
- Max $r_{DS(on)}$ = 1.8 Ω at V_{GS} = –1.5 V, I_D = –0.36 A
- HBM ESD Protection Level = 1400 V (Note 1)
- This Device is Pb−Free and is RoHS Compliant

Application

- Li−Ion Battery Pack

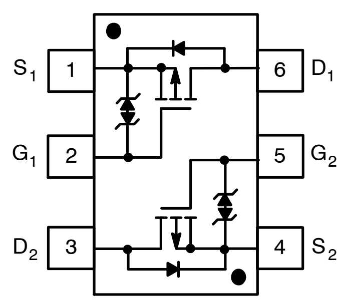
NOTE:
1. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

MARKING DIAGRAM



G = Device Code
&2 = 2−Digit Date Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

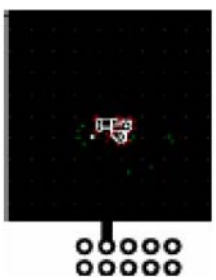
Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		–20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current	– Continuous (Note 2a)	–0.83	A
		– Pulsed	–1.0	
P_D	Power Dissipation	(Note 2a)	0.625	W
		(Note 2b)	0.446	
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

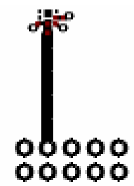
THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	200	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2b)	280	°C/W

2. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 200°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 280°C/W when mounted on a minimum pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250 μA, V_{GS} = 0 V	–20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25°C	–	–11	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250 μA	–0.4	–0.7	–1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25°C	–	3	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On–Resistance	V_{GS} = –4.5 V, I_D = –0.83 A	–	0.28	0.5	Ω
		V_{GS} = –2.5 V, I_D = –0.70 A	–	0.36	0.7	
		V_{GS} = –1.8 V, I_D = –0.43 A	–	0.47	1.2	
		V_{GS} = –1.5 V, I_D = –0.36 A	–	0.62	1.8	
		V_{GS} = –4.5 V, I_D = –0.83 A, T_J = 125°C	–	0.39	0.85	
g_{FS}	Forward Transconductance	V_{DD} = –5 V, I_D = –0.83 A	–	2	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1 MHz	–	100	135	pF
C_{oss}	Output Capacitance		–	23	35	pF
C_{rss}	Reverse Transfer Capacitance		–	18	30	pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –0.83 A V_{GS} = –4.5 V, R_{GEN} = 6 Ω	–	3.5	10	ns
t_r	Rise Time		–	2.9	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	23	37	ns
t_f	Fall Time		–	13	23	ns
Q_g	Total Gate Charge	V_{DD} = –10 V, I_D = –0.83 A V_{GS} = –4.5 V	–	2.2	3.1	nC
Q_{gs}	Gate to Source Charge		–	0.3	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	0.6	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATING						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–0.52	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.52 A (Note 3)	–	–1.0	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –0.83 A, dI_F/dt = 100 A/μs	–	18	31	ns
Q_{rr}	Reverse Recovery Charge		–	3.8	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

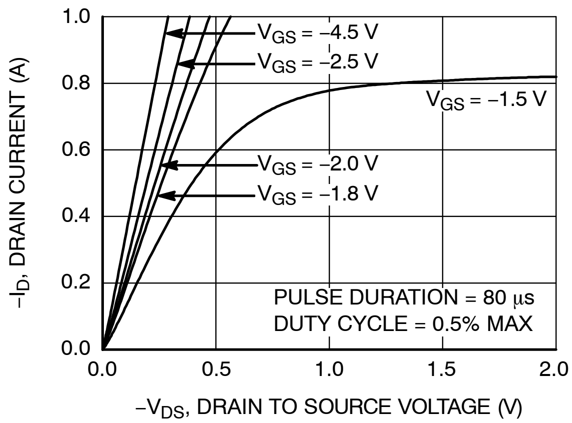


Figure 1. On Region Characteristics

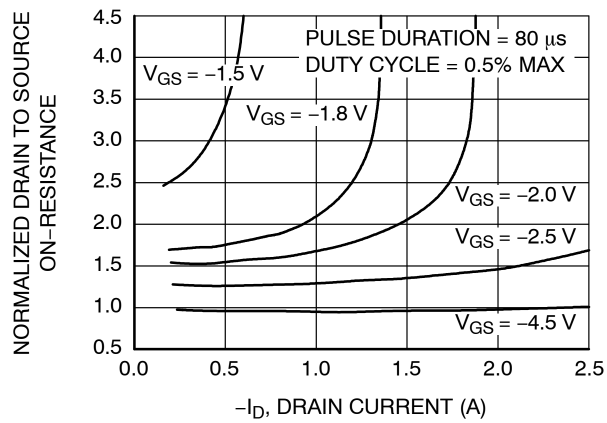


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

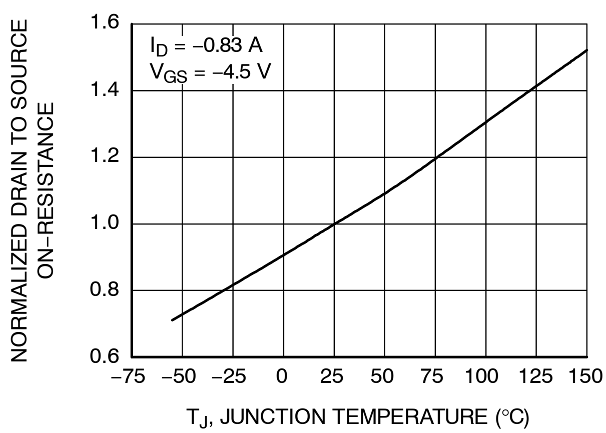


Figure 3. Normalized On Resistance vs. Junction Temperature

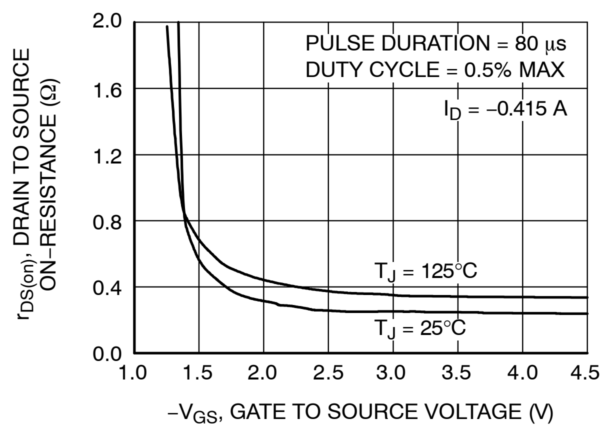


Figure 4. On−Resistance vs. Gate to Source Voltage

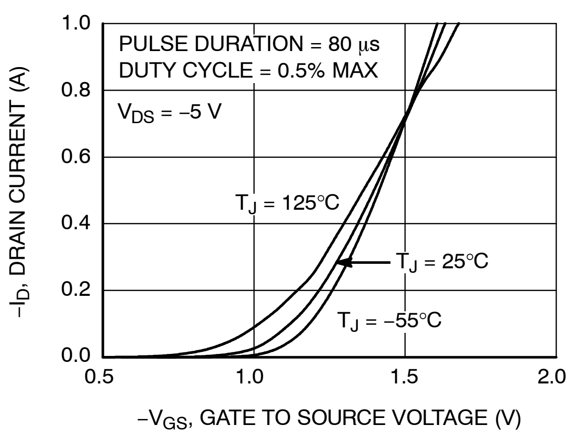


Figure 5. Transfer Characteristics

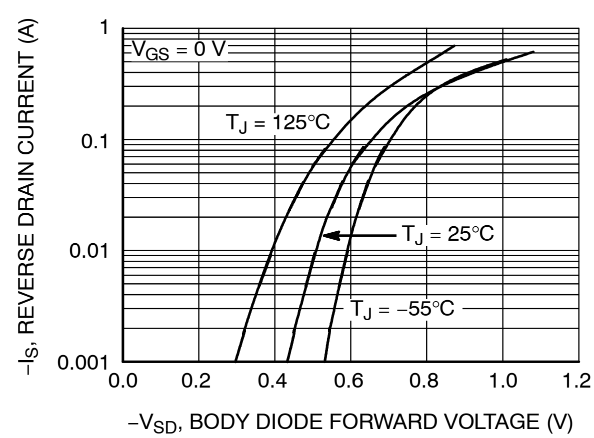


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL ELECTRICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)

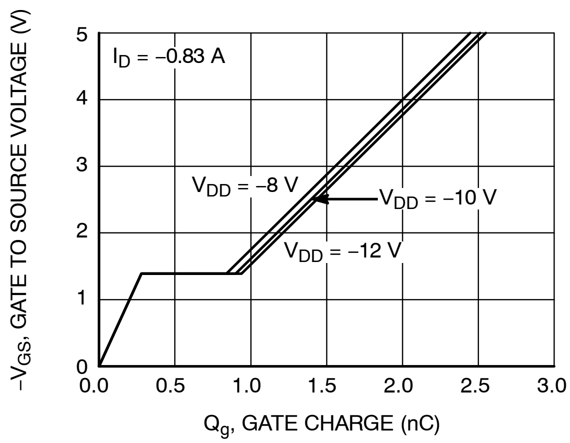


Figure 7. Gate Charge Characteristics

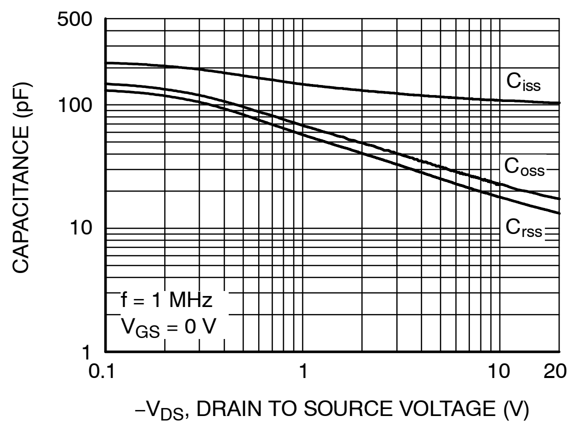


Figure 8. Capacitance vs. Drain to Source Voltage

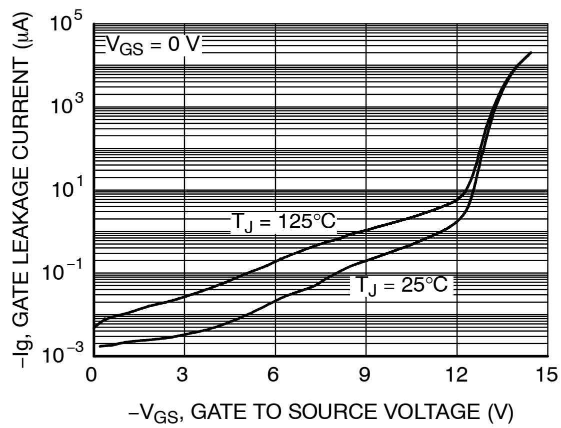


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

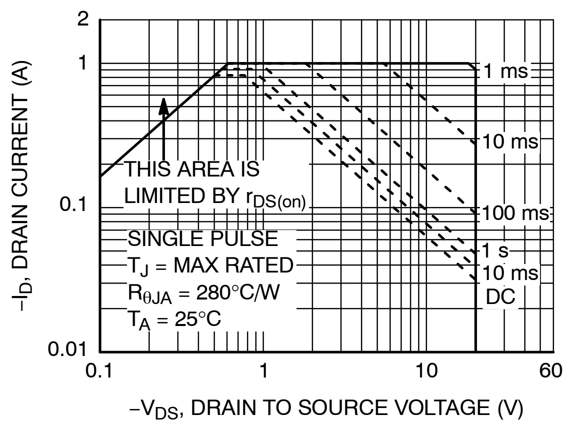


Figure 10. Forward Bias Safe Operating Area

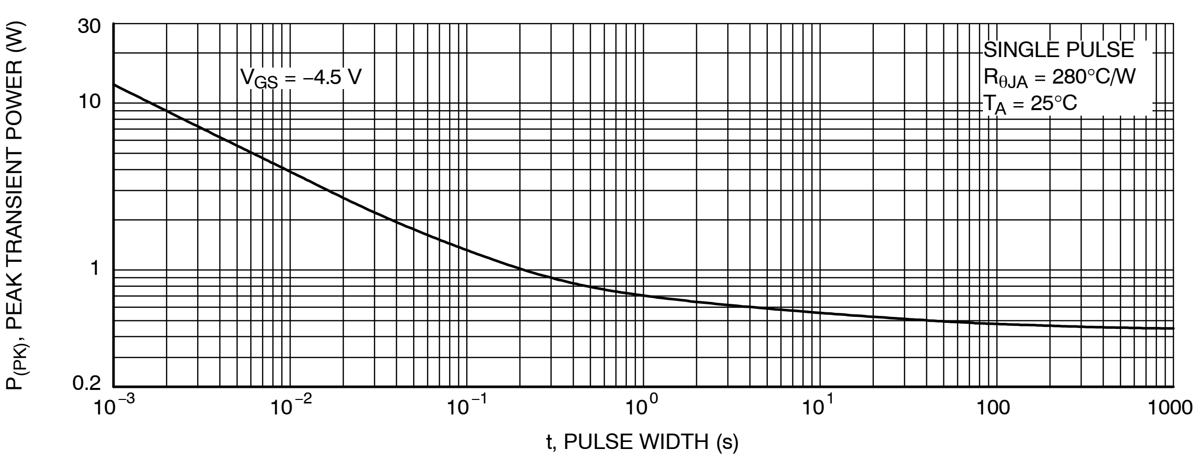


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL ELECTRICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)

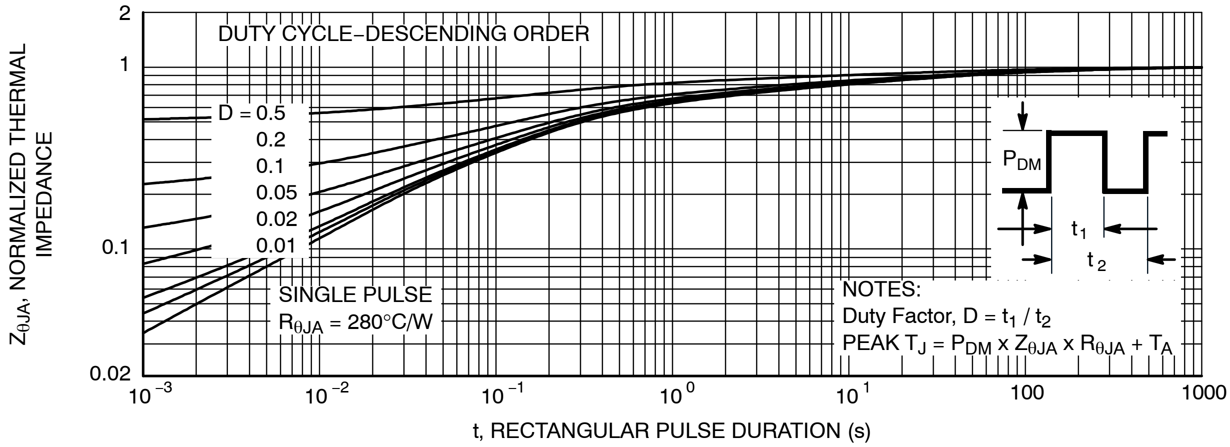


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDY1002PZ	G	SOT−563 (Pb−Free)	7”	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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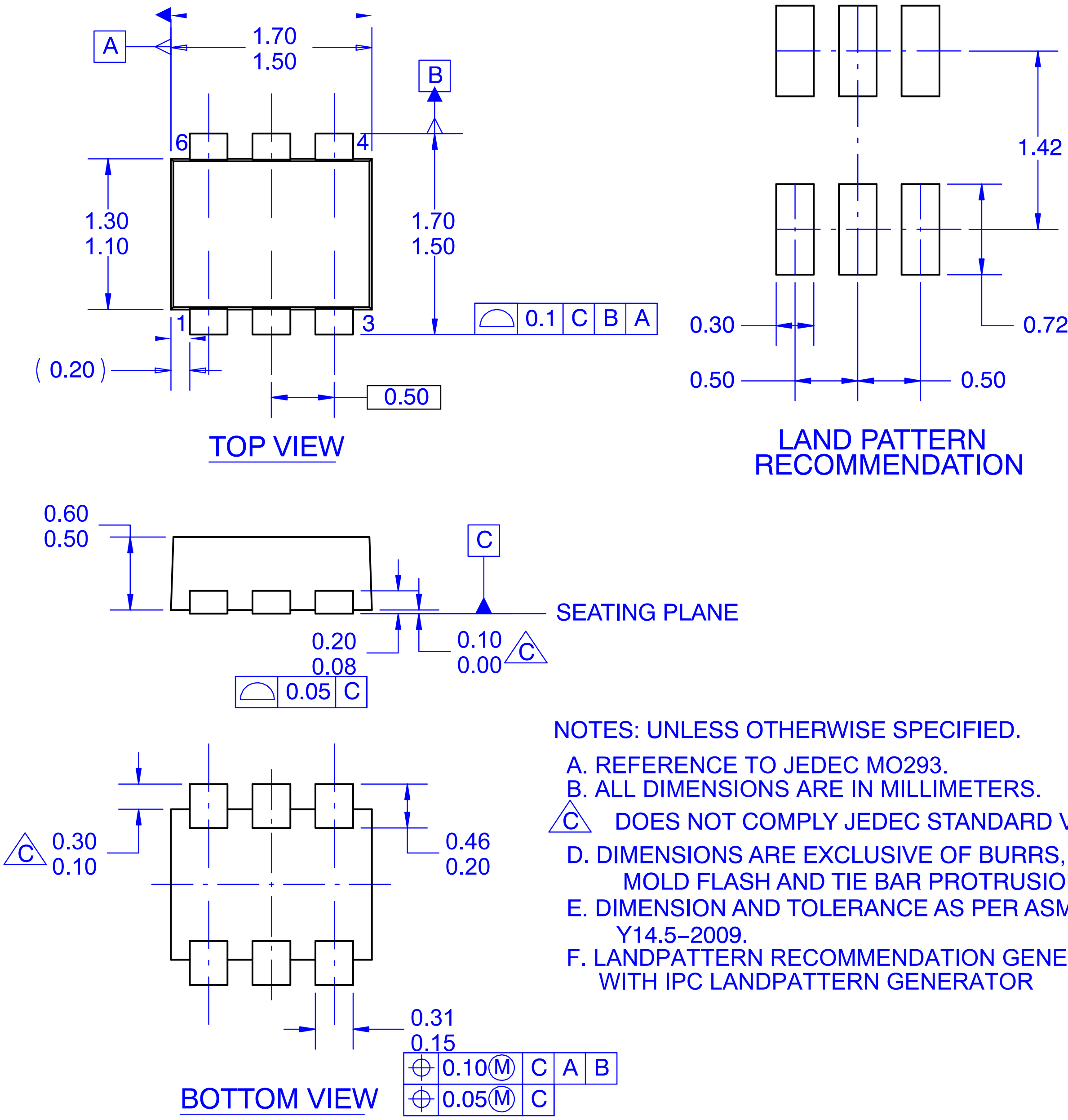
DATE 31 AUG 2016



NOTES: UNLESS OTHERWISE SPECIFIED.

A. REFERENCE TO JEDEC MO293.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT COMPLY JEDEC STANDARD VALUE.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5−2009.
F. LANDPATTERN RECOMMENDATION GENERATED WITH IPC LANDPATTERN GENERATOR

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TECHNICAL PUBLICATIONS:
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onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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