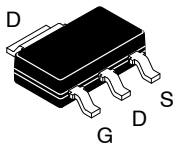
# MOSFET – N-Channel, POWERTRENCH®

## 100 V, 3.2 A, 108 mΩ

# FDT86106LZ

| $V_{DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 100 V | 108 mΩ @ 10 V | 3.2 A |
| | 153 mΩ @ 4.5 V | |




**SOT−223**
**CASE 318H**

### General Description

This N−Channel logic Level MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that has been special tailored to minimize the on−state resistance and yet maintain superior switching performance. G−S zener has been added to enhance ESD voltage level.

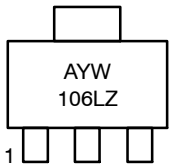
### Features

- Max $r_{DS(on)}$ = 108 mΩ at $V_{GS}$ = 10 V, $I_D$ = 3.2 A
- Max $r_{DS(on)}$ = 153 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 2.7 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- HBM ESD Protection Level > 3 kV Typical (Note 4)
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

### Applications

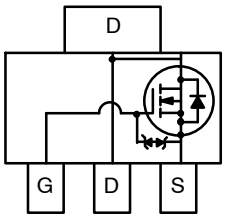
- DC − DC Conversion

### MARKING DIAGRAM




A = Specific Device Code
Y = Date Code
W = Work Week
106LZ = Specific Device Code

### PINOUT




### MOSFET MAXIMUM RATINGS ($T_C$ = 25°C unless otherwise noted)

| Symbol | Parameter | | Ratings | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain−Source Voltage | | 100 | V |
| $V_{GS}$ | Gate−Source Voltage | | ±20 | V |
| $I_D$ | Drain Current | − Continuous $T_A$ = 25°C (Note 1a.) | 3.2 | A |
| | | − Pulsed | 12 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | | 12 | mJ |
| $P_D$ | Power Dissipation | $T_A$ = 25°C (Note 1a.) | 2.2 | W |
| | | $T_A$ = 25°C (Note 1b.) | 1.0 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 12 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a.) | 55 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDT86106LZ | 106LZ | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

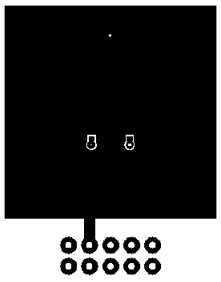
## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 100 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | 71 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±10 | μA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.5 | 2.2 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | –5 | – | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.2 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 2.7 A,<br>$V_{GS}$ = 10 V, $I_D$ = 3.2 A, $T_J$ = 125°C | –<br>–<br>– | 80<br>100<br>140 | 108<br>153<br>189 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 3.2 A | – | 8 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 234 | 315 | pF |
| $C_{oss}$ | Output Capacitance | | – | 46 | 65 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 3.1 | 5 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 3.2 A,<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 3.8 | 10 | ns |
| $t_r$ | Rise Time | | – | 1.3 | 10 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 10 | 20 | ns |
| $t_f$ | Fall Time | | – | 1.5 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 50 V, $I_D$ = 3.2 A | – | 4.3 | 7 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 5 V, $V_{DD}$ = 50 V, $I_D$ = 3.2 A | – | 2.4 | 4 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | $V_{DD}$ = 50 V, $I_D$ = 3.2 A | – | 0.7 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | – | 0.9 | – | nC |
| **DRAIN–SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 3.2 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 1 A (Note 2) | –<br>– | 0.86<br>0.77 | 1.3<br>1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 3.2 A, di/dt = 100 A/s | – | 31 | 49 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 21 | 34 | nC |

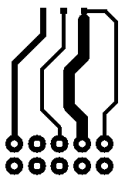
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.



a. 55°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b. 118°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Starting $T_J$ = 25°C, L = 1 mH, $I_{AS}$ = 5 A, $V_{DD}$ = 90 V, $V_{GS}$ = 10 V.
4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

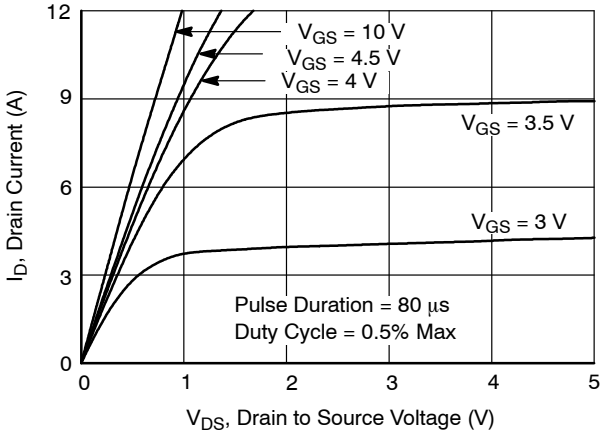



**Figure 1. On−Region Characteristics**

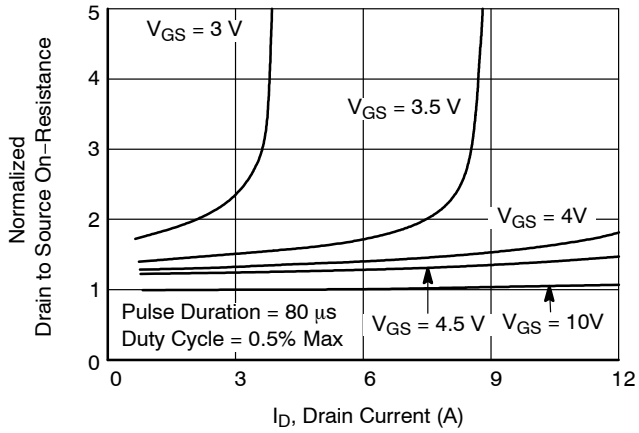



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

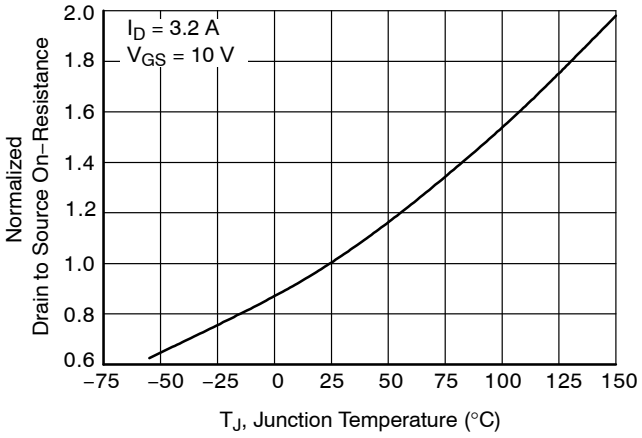



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

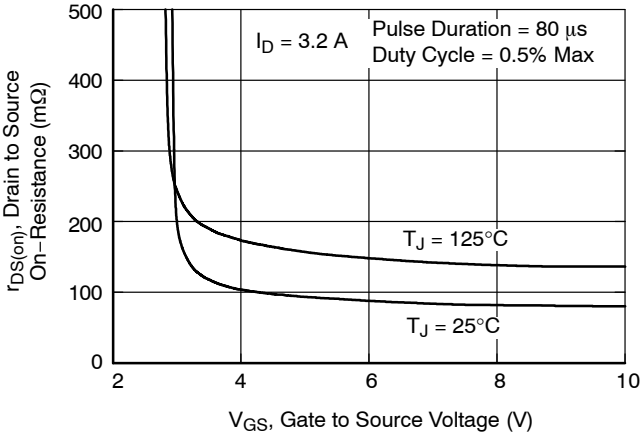



**Figure 4. On−Resistance vs. Gate to Source Voltage**

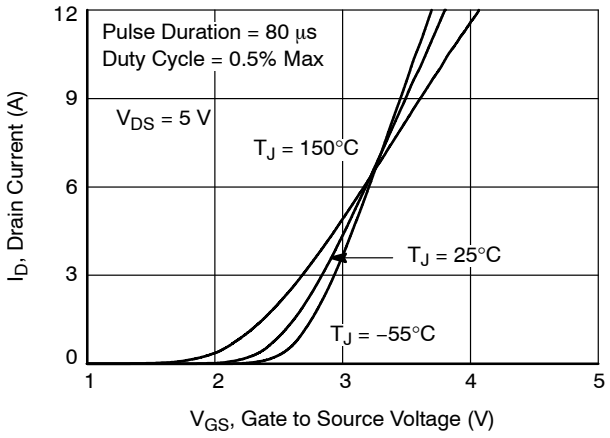



**Figure 5. Transfer Characteristics**

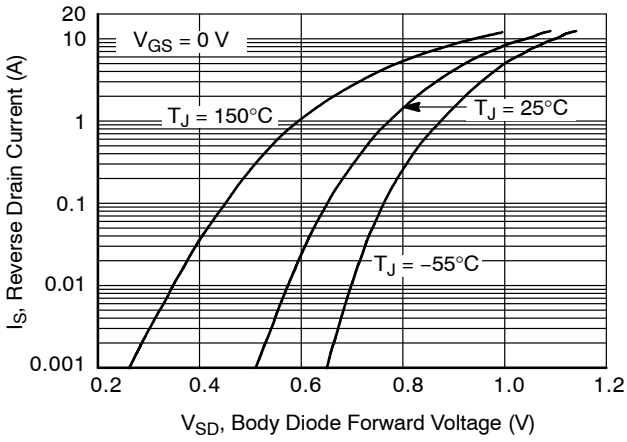



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted) (continued)

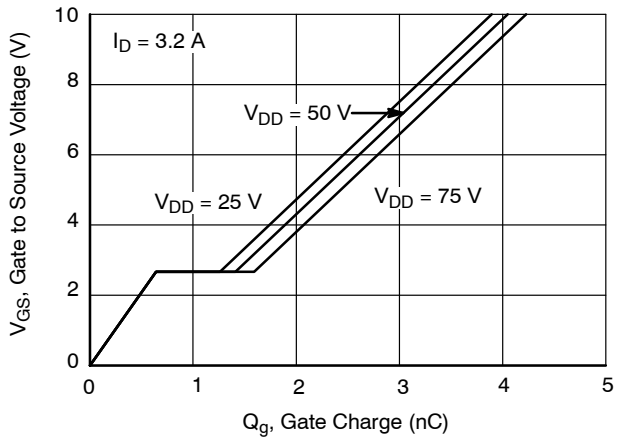



**Figure 7. Gate Charge Characteristics**

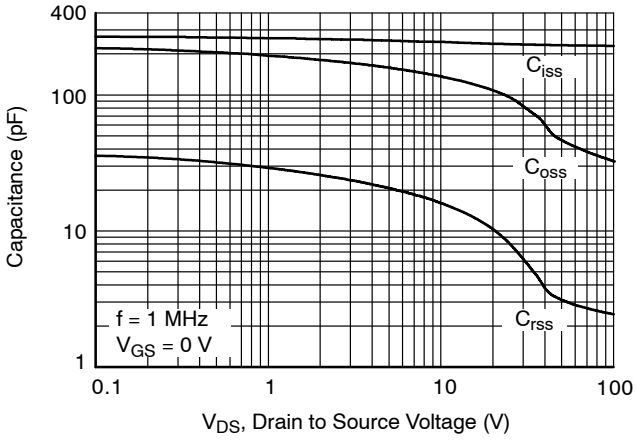



**Figure 8. Capacitance vs. Drain to Source Voltage**

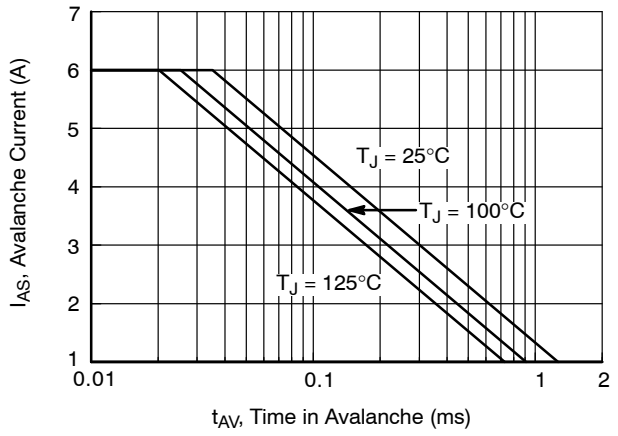



**Figure 9. Unclamped Inductive Switching Capability**

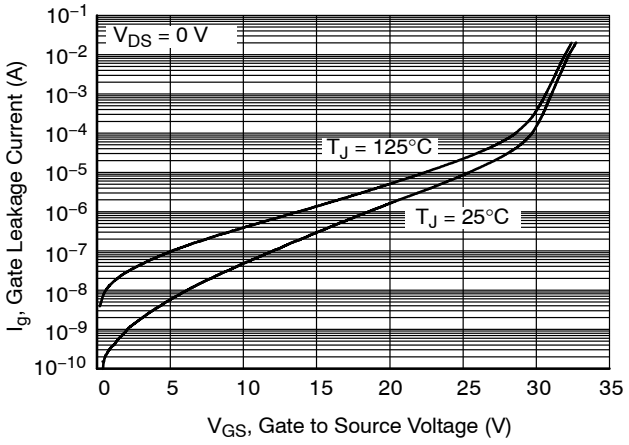



**Figure 10. Gate Leakage Current vs. Gate to Source Voltage**

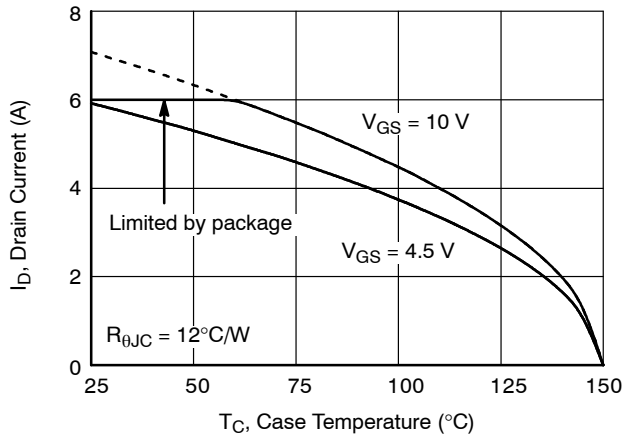



**Figure 11. Maximum Continuous Drain Current vs. Case temperature**

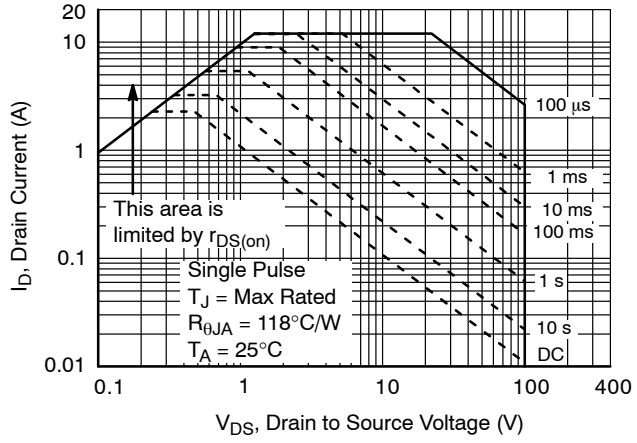



**Figure 12. Forward Bias Safe Operating Area**

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted) (continued)

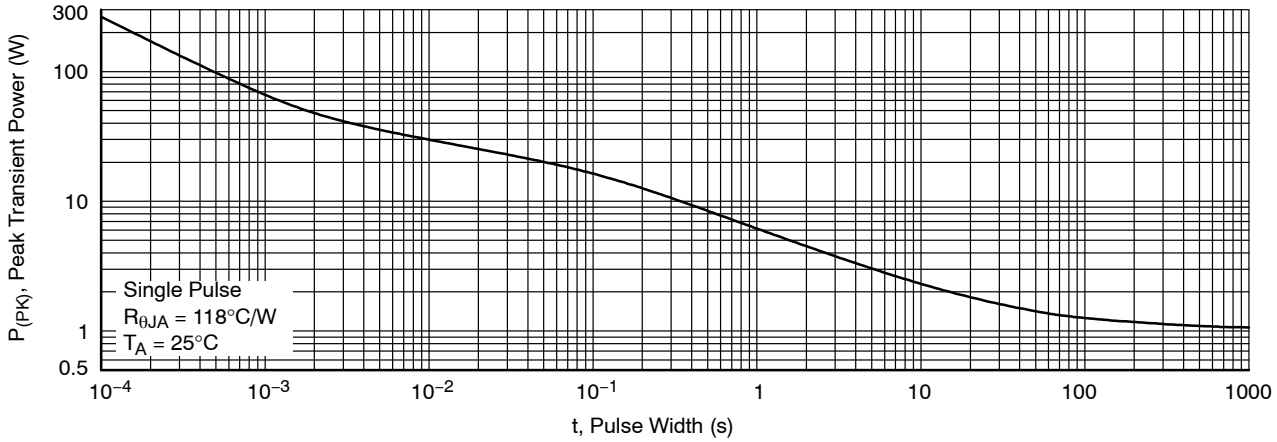



**Figure 13. Single Pulse Maximum Power Dissipation**

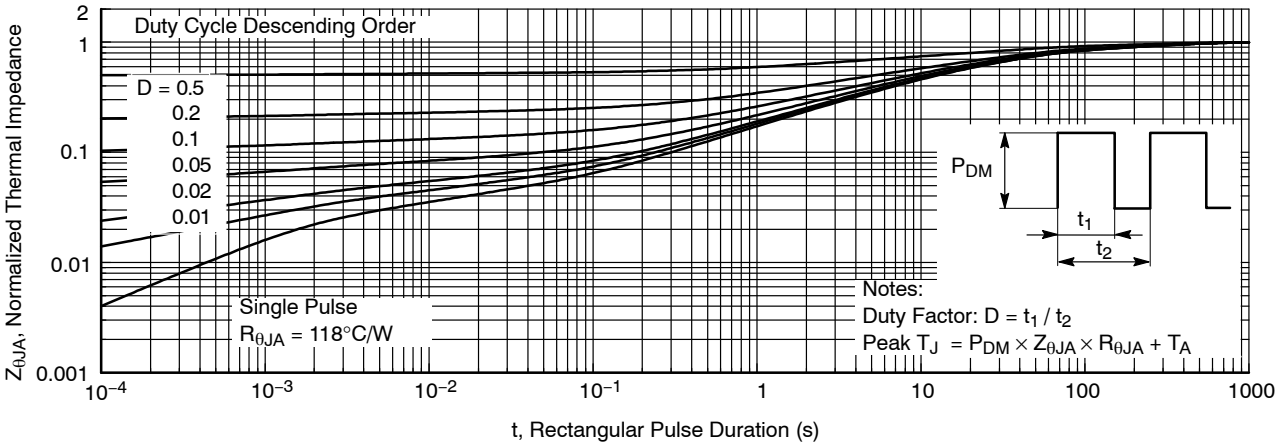
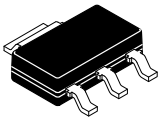


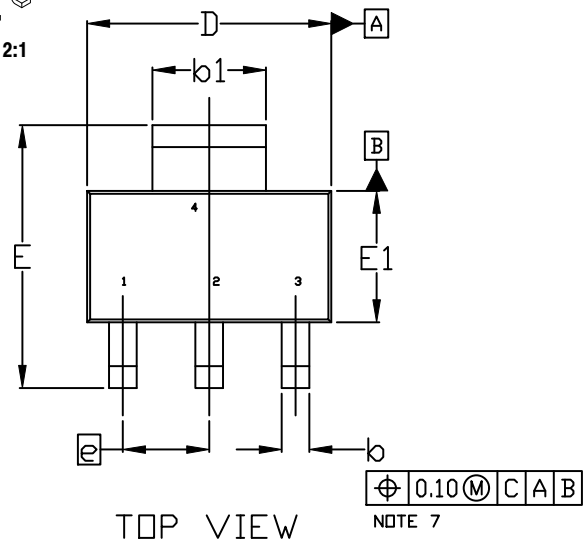

**Figure 14. Junction−to−Ambient Transient Thermal Response Curve**

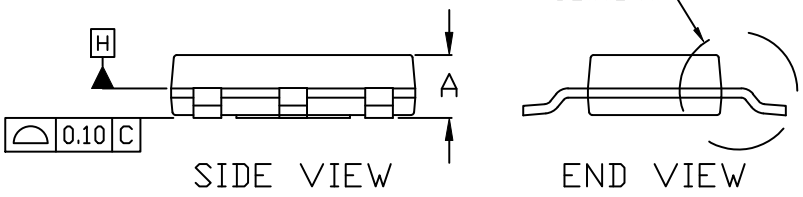


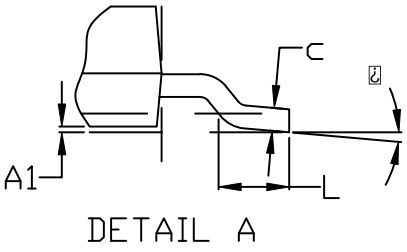
SCALE 2:1

**SOT−223**
CASE 318H
ISSUE B

DATE 13 MAY 2020

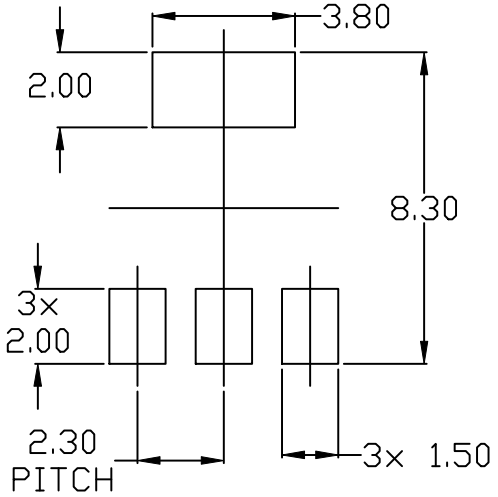



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

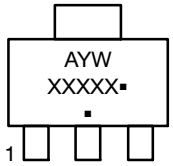
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | --- | --- | 1.80 |
| A1 | 0.02 | 0.06 | 0.11 |
| b | 0.60 | 0.74 | 0.88 |
| b1 | 2.90 | 3.00 | 3.10 |
| c | 0.24 | --- | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 6.70 | 7.00 | 7.30 |
| E1 | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.25 | --- | --- |
| θ | 0° | --- | 10° |




RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOT−223** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales