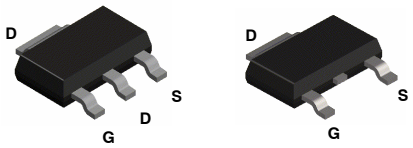
MOSFET – P-Channel 30 V POWERTRENCH®

FDT458P



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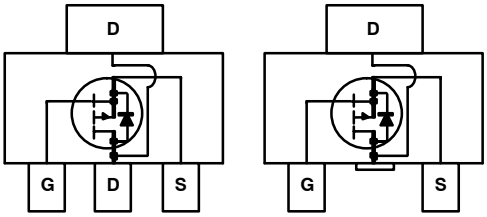


Description

This P−Channel MOSFET has been Designed Specifically to Improve the Overall Efficiency of DC/DC Converters using either Synchronous or Conventional Switching PWM Controllers, and battery chargers.

These MOSFETs Feature Faster Switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

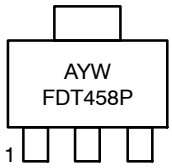
Features

- 3.4 A, −30 V.
  - $R_{DS(on)}$ = 130 mΩ @ V_{GS} = 10 V
  - $R_{DS(on)}$ = 200 mΩ @ V_{GS} = 4.5 V
- Fast switching speed
- Low gate charge (2.5 nC typical)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Battery Chargers
- Motor Drives

MARKING DIAGRAM



FDT4584P	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb Free Package

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−Source Voltage	−30	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current −Continuous (Note 1a)	3.4	A
	−Pulsed	10	
P_D	Maximum Power Dissipation (Note 1a)	3.0	W
	(Note 1b)	1.3	
	(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range.	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDT458P	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	12	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−30	−	−	V
$\frac{\Delta BV_{DSS(th)}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	−23	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −24 V, V_{GS} = 0 V	−	−	1	μA
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 25 V, V_{DS} = 0 V	−	−	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −25 V, V_{DS} = 0 V	−	−	−100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−1	−1.8	−3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	4	−	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −3.4 A	−	105	130	mΩ
		V_{GS} = −4.5 V, I_D = −2.7 A	−	157	200	
		V_{GS} = −10 V, I_D = −3.4 A, T_J = 125°C	−	147	210	
$I_{D(on)}$	On−State Drain Current	V_{GS} = −10 V, V_{DS} = −5 V	−5	−	−	A
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −3.4 A	−	3	−	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = −15 V, V_{GS} = 0 V, f =1.0 MHz	−	205	−	pF
C_{oss}	Output Capacitance		−	55	−	pF
C_{rss}	Reverse Transfer Capacitance		−	26	−	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −15 V, I_D = −1 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	−	4.5	9	ns
t_r	Turn−On Rise Time		−	12.5	23	ns
$t_{d(off)}$	Turn−Off Delay Time		−	11	20	ns
t_f	Turn−Off Fall Time		−	2	4	ns
Q_g	Total Gate Charge	V_{DS} = −15 V, I_D = −3.4 A, V_{GS} = −10 V	−	2.5	3.5	nC
Q_{gs}	Gate−Source Charge		−	0.7	−	nC
Q_{gd}	Gate−Drain Charge		−	1	−	nC

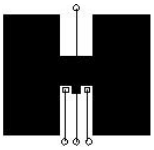
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	−2.5	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −2.5 A (Note 2)	−	−0.8	−1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

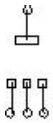
NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a).42 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b).95°C/W when mounted on a.0066 in^2 pad of 2 oz copper.



c).110°C/W when mounted on a minimum pad.

2. Pulse Test : Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS T_J = 25°C UNLESS OTHERWISE NOTED

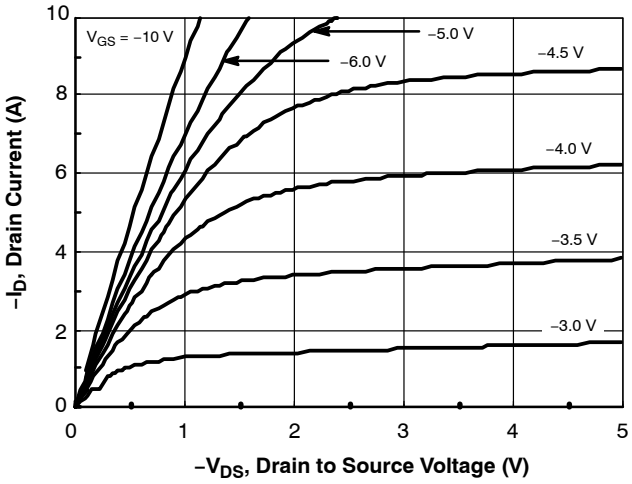


Figure 1. On−Region Characteristics

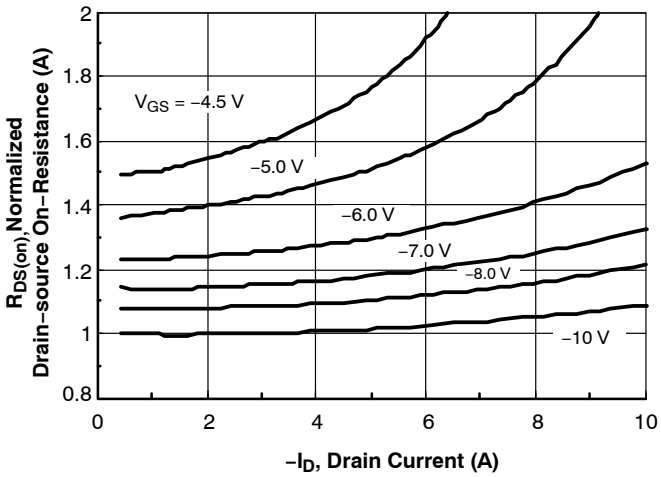


Figure 2. On−Resistance Variation With Drain Current and Gate Voltage

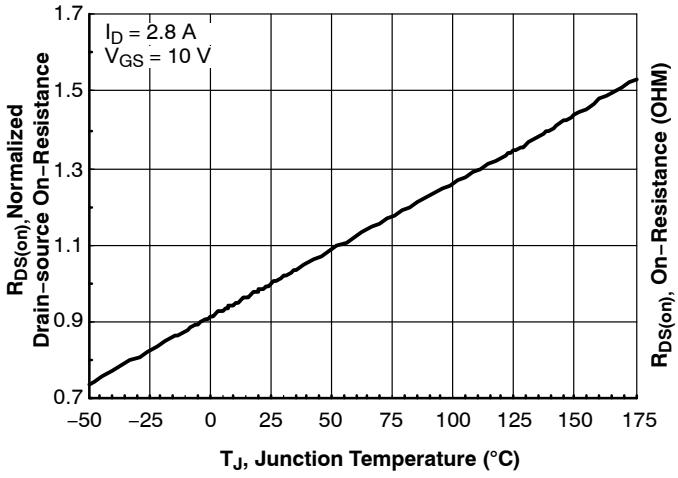


Figure 3. On−Resistance Variation With Temperature

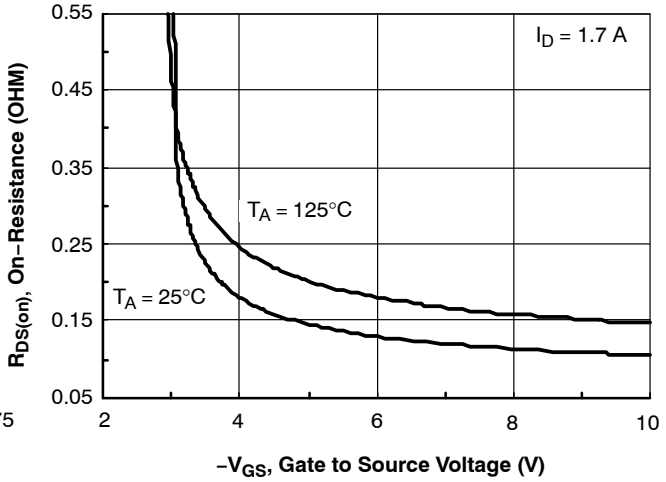


Figure 4. On−Resistance Variation with Gate−to−Source Voltage.

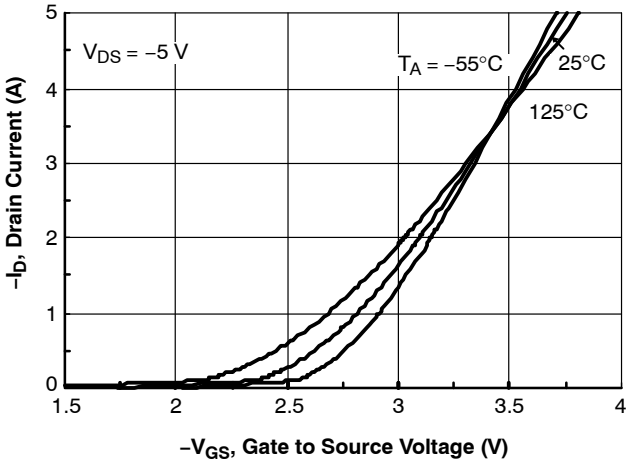


Figure 5. Transfer Characteristics

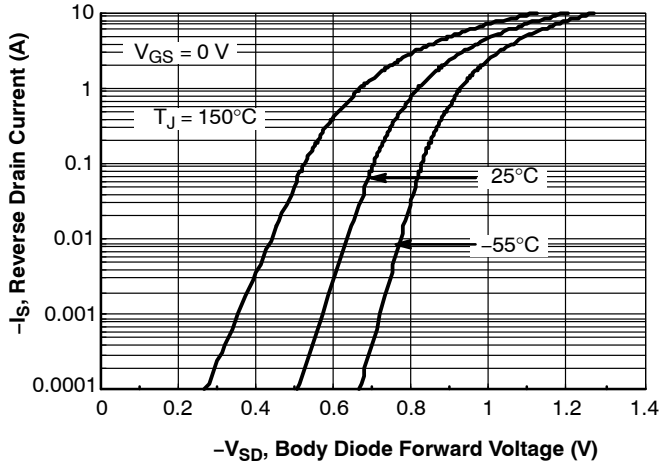


Figure 6. Body Diode Forward Voltage Variation With Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED) T_J = 25°C UNLESS OTHERWISE NOTED

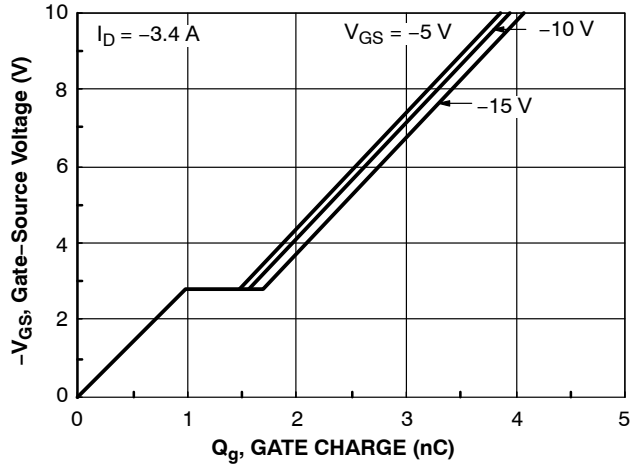


Figure 7. Gate Charge Characteristics

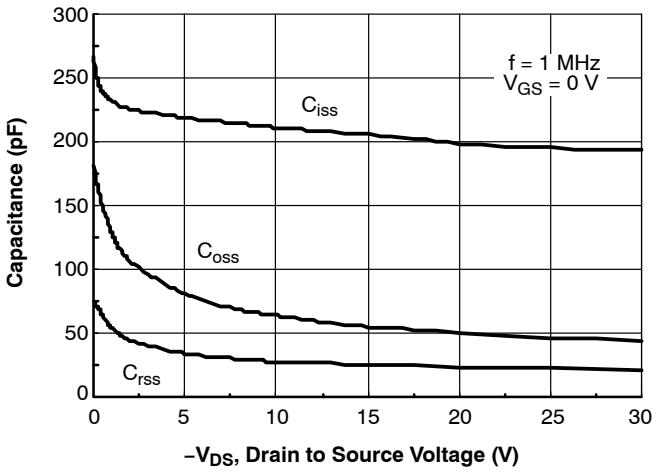


Figure 8. Capacitance Characteristics

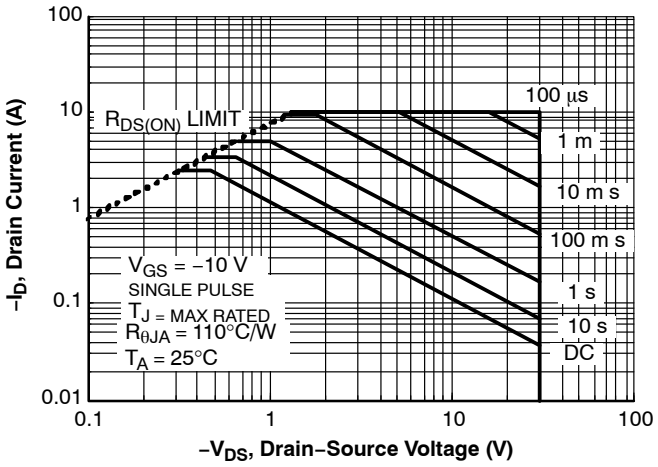


Figure 9. Maximum Safe Operating Area

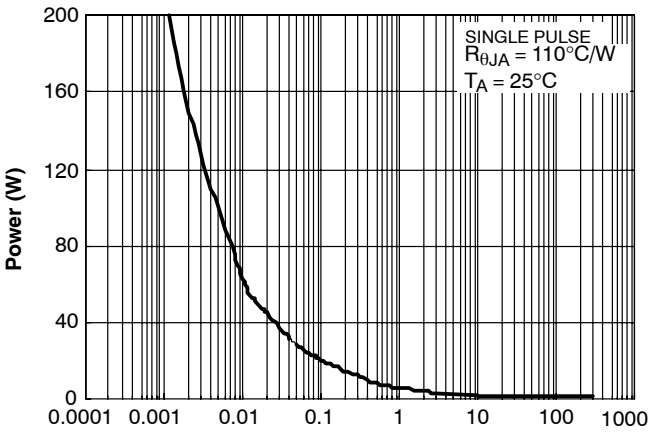


Figure 10. Single Pulse Maximum Power Dissipation.

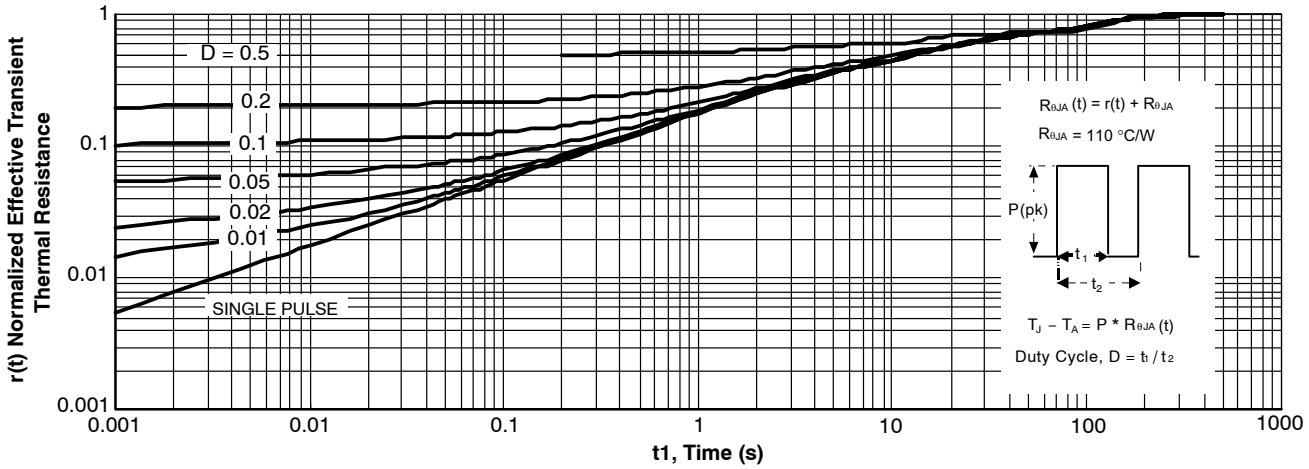


Figure 11. Transient Thermal Response Curve.

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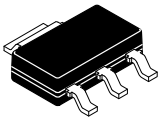
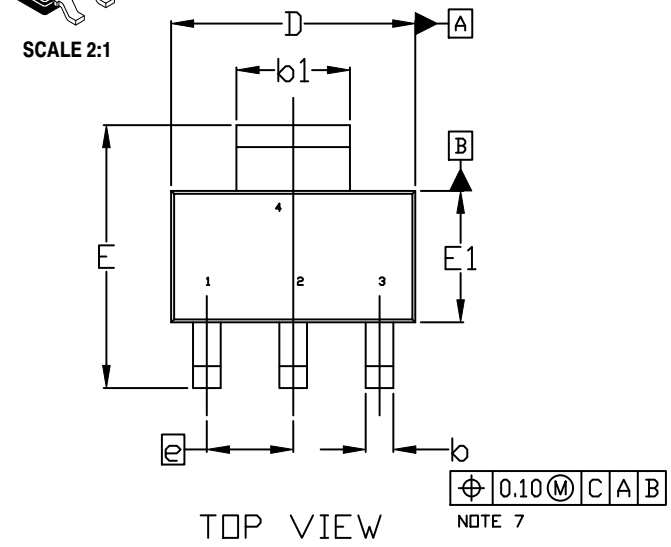
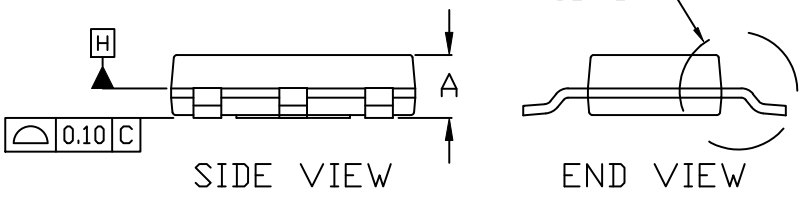
ISSUE B

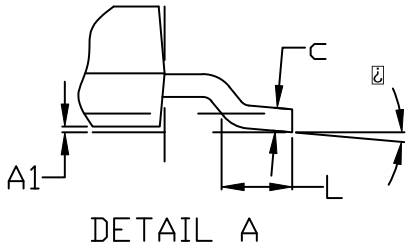
DATE 13 MAY 2020



SCALE 2:1

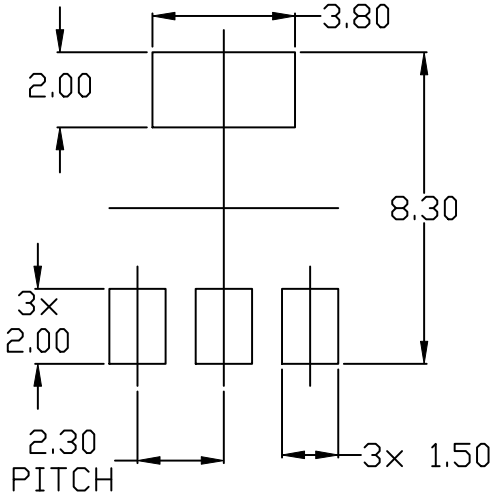






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

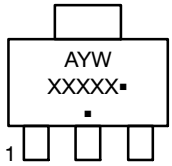
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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