FDS8858CZ
Dual N & P-Channel PowerTrench® MOSFET
N-Channel: 30V, 8.6A, 17.0mΩ P-Channel: -30V, -7.3A, 20.5mΩ

Features
Q1: N-Channel
- Max \( r_{DS(on)} = 17\text{mΩ} \) at \( V_{GS} = 10\text{V}, I_D = 8.6\text{A} \)
- Max \( r_{DS(on)} = 20\text{mΩ} \) at \( V_{GS} = 4.5\text{V}, I_D = 7.3\text{A} \)
Q2: P-Channel
- Max \( r_{DS(on)} = 20.5\text{mΩ} \) at \( V_{GS} = -10\text{V}, I_D = -7.3\text{A} \)
- Max \( r_{DS(on)} = 34.5\text{mΩ} \) at \( V_{GS} = -4.5\text{V}, I_D = -5.6\text{A} \)
- High power and handling capability in a widely used surface mount package
- Fast switching speed

General Description
These dual N and P-Channel enhancement mode power MOSFETs are produced using ON Semiconductor’s advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications
- Inverter
- Synchronous Buck

MOSFET Maximum Ratings \(T_A = 25°C\) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Q1</th>
<th>Q2</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DS})</td>
<td>Drain to Source Voltage</td>
<td>30</td>
<td>-30</td>
<td>V</td>
</tr>
<tr>
<td>(V_{GS})</td>
<td>Gate to Source Voltage</td>
<td>±20</td>
<td>±25</td>
<td>V</td>
</tr>
<tr>
<td>(I_D)</td>
<td>Drain Current</td>
<td>8.6</td>
<td>-7.3</td>
<td>A</td>
</tr>
<tr>
<td>(E_{AS})</td>
<td>Single Pulse Avalanche Energy</td>
<td>50</td>
<td>11</td>
<td>mJ</td>
</tr>
<tr>
<td>(P_D)</td>
<td>Power Dissipation for Dual Operation</td>
<td>2.0</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>Power Dissipation for Single Operation</td>
<td>(Note 1a)</td>
<td>1.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(T_J \leq 25°C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(T_J \leq 25°C)</td>
<td>(Note 1c)</td>
<td>0.9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Dissipation for Single Operation</td>
<td>(T_A = 25°C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_J, T_{STG})</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to +150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Thermal Characteristics
- \(R_{JUC}\) Thermal Resistance, Junction to Case (Note 1) 40 °C/W
- \(R_{JUA}\) Thermal Resistance, Junction to Ambient (Note 1a) 78

Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDS8858CZ</td>
<td>FDS8858CZ</td>
<td>SO-8</td>
<td>13&quot;</td>
<td>12mm</td>
<td>2500 units</td>
</tr>
</tbody>
</table>
### Electrical Characteristics  \( T_J = 25^\circ C \) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Type</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
</table>
| \( \text{V}_{\text{DS}} \) | Drain to Source Breakdown Voltage | \( I_D = 250\mu A, V_{GS} = 0V \)  
  \( I_D = -250\mu A, V_{GS} = 0V \) | Q1  
  Q2 | 30 | -30 | V |
| \( \Delta V_{\text{DS}} / \Delta T_J \) | Breakdown Voltage Temperature Coefficient | \( I_D = 250\mu A, \) referenced to 25°C  
  \( I_D = -250\mu A, \) referenced to 25°C | Q1  
  Q2 | -22 | -22 | mV/°C |
| \( I_{\text{DSS}} \) | Zero Gate Voltage Drain Current | \( V_{GS} = 24V, V_{DS} = 0V \)  
  \( V_{DS} = -24V, V_{GS} = 0V \) | Q1  
  Q2 | 1 | -1 | μA |
| \( I_{\text{GSS}} \) | Gate to Source Leakage Current | \( V_{GS} = \pm 20V, V_{DS} = 0V \)  
  \( V_{GS} = \pm 25V, V_{DS} = 0V \) | Q1  
  Q2 | ±10 | ±10 | μA |

**On Characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Type</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
</table>
| \( V_{GSS(\text{th})} \) | Gate to Source Threshold Voltage | \( V_{GS} = V_{DS}, I_D = 250\mu A \)  
  \( V_{GS} = V_{DS}, I_D = -250\mu A \) | Q1  
  Q2 | 1 | -1 | 1.6 | -3 | V |
| \( \Delta V_{GSS(\text{th})} / \Delta T_J \) | Gate to Source Threshold Voltage Temperature Coefficient | \( I_D = 250\mu A, \) referenced to 25°C  
  \( I_D = -250\mu A, \) referenced to 25°C | Q1  
  Q2 | 5.4 | 6.0 | mV/°C |
| \( r_{DS(on)} \) | Static Drain to Source On Resistance | \( V_{GS} = 10V, I_D = 8.6A \)  
  \( V_{GS} = 4.5V, I_D = 7.3A \)  
  \( V_{GS} = 10V, I_D = 8.6A, T_J = 125^\circ C \) | Q1  
  Q2 | 12.4 | 15.2 | 17.7 | 20.0 | 24.3 | Ω |
| \( g_{FS} \) | Forward Transconductance | \( V_{DS} = 5V, I_D = 8.6A \)  
  \( V_{DS} = -5V, I_D = -7.3A \) | Q1  
  Q2 | 27 | 21 | S |

**Dynamic Characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Q1</th>
<th>Q2</th>
<th>905</th>
<th>1675</th>
<th>1205</th>
<th>2230</th>
<th>pF</th>
</tr>
</thead>
</table>
| \( C_{iss} \) | Input Capacitance | 15V, V_{GS} = 0V, f = 1MHz | Q1  
  Q2 | 180 | 290 | 240 | 390 | pF |
| \( C_{oss} \) | Output Capacitance | V_{DS} = -15V, V_{GS} = 0V, f = 1MHz | Q1  
  Q2 | 110 | 260 | 165 | 390 | pF |
| \( C_{rss} \) | Reverse Transfer Capacitance | | Q1  
  Q2 | 905 | 1675 | 1205 | 2230 | pF |
| \( R_g \) | Gate Resistance | f = 1MHz | Q1  
  Q2 | 4.3 | 4.4 | Ω |

**Switching Characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Q1</th>
<th>Q2</th>
<th>905</th>
<th>1675</th>
<th>1205</th>
<th>2230</th>
<th>pF</th>
</tr>
</thead>
</table>
| \( t_{\text{d(on)}} \) | Turn-On Delay Time | \( V_{DD} = 15V, I_D = 8.6A \)  
  \( V_{GS} = 10V, R_{GEN} = 6\Omega \) | Q1  
  Q2 | 7 | 14 | 18 | ns |
| \( t_r \) | Rise Time | \( V_{DD} = 15V, I_D = 7.3A \)  
  \( V_{GS} = 10V, R_{GEN} = 6\Omega \) | Q1  
  Q2 | 3 | 10 | 20 | ns |
| \( t_{\text{d(off)}} \) | Turn-Off Delay Time | \( V_{DD} = -15V, I_D = 7.3A \)  
  \( V_{GS} = -10V, R_{GEN} = 6\Omega \) | Q1  
  Q2 | 10 | 10 | 10 | 20 | ns |
| \( t_f \) | Fall Time | \( V_{GS} = 10V, V_{DD} = 15V, I_D = 8.6A \) | Q1  
  Q2 | 17 | 33 | 53 | 53 | ns |
| \( Q_{g(TOT)} \) | Total Gate Charge | \( V_{GS} = 10V, V_{DD} = -15V, I_D = -7.3A \) | Q1  
  Q2 | 2.7 | 6.1 | 2.7 | 6.1 | nC |
| \( Q_{gs} \) | Gate to Source Charge | | | | | | | |
| \( Q_{gd} \) | Gate to Drain “Miller” Charge | \( V_{GS} = -10V, V_{DD} = -15V, I_D = -7.3A \) | Q1  
  Q2 | 3.4 | 8.5 | 3.4 | 8.5 | nC |

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Electrical Characteristics  $T_J = 25^\circ C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Type</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SD}$</td>
<td>Source to Drain Diode Forward Voltage</td>
<td>$V_{GS} = 0V, I_S = 8.6A$ (Note 2) $V_{GS} = 0V, I_S = -7.3A$ (Note 2)</td>
<td>Q1</td>
<td>0.8</td>
<td>0.9</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q2</td>
<td></td>
<td></td>
<td>-1.2</td>
<td></td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Reverse Recovery Time</td>
<td>$I_F = 8.6A, di/dt = 100A/s$</td>
<td>Q1</td>
<td>25</td>
<td>28</td>
<td>38</td>
<td>ns</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>Q2</td>
<td></td>
<td></td>
<td>42</td>
<td></td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>Reverse Recovery Charge</td>
<td>$I_F = -7.3A, di/dt = 100A/s$</td>
<td>Q1</td>
<td>19</td>
<td>22</td>
<td>29</td>
<td>nC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q2</td>
<td></td>
<td></td>
<td>33</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. $R_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{JC}$ is guaranteed by design while $R_{CA}$ is determined by the user’s board design.
2. Pulse Test: Pulse Width < 300$\mu$s, Duty cycle < 2.0%.
3. Starting $T_J = 25^\circ C$, N-ch: $L = 1mH, I_{AS} = 10A, V_{DD} = 27V, V_{GS} = 10V$; P-ch: $L = 1mH, I_{AS} = -4.7A, V_{DD} = -27V, V_{GS} = -10V$. 

Scale 1 : 1 on letter size paper
Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ C$ unless otherwise noted

**Figure 1.** On-Region Characteristics

**Figure 2.** Normalized On-Resistance vs Drain Current and Gate Voltage

**Figure 3.** Normalized On-Resistance vs Junction Temperature

**Figure 4.** On-Resistance vs Gate to Source Voltage

**Figure 5.** Transfer Characteristics

**Figure 6.** Source to Drain Diode Forward Voltage vs Source Current

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Typical Characteristics (Q1 N-Channel) \( T_J = 25°C \) unless otherwise noted

**Figure 7.** Gate Charge Characteristics

**Figure 8.** Capacitance vs Drain to Source Voltage

**Figure 9.** Unclamped Inductive Switching Capability

**Figure 10.** Gate Leakage Current vs Gate to Source Voltage

**Figure 11.** Maximum Continuous Drain Current vs Ambient Temperature

**Figure 12.** Forward Bias Safe Operating Area
Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ C$ unless otherwise noted

Figure 13. Single Pulse Maximum Power Dissipation

FOR TEMPERATURES ABOVE 25$^\circ$C DERATE PEAK CURRENT AS FOLLOWS:

$$I = \frac{I_{25^\circ C}}{1 + \frac{T_A - 25}{125}}$$

$T_A = 25^\circ C$

Figure 14. Transient Thermal Response Curve

NOTES:

DUTY FACTOR: $D = \frac{t_1}{t_2}$

$PDM \times Z_{JC} \times R_{\theta JA} + T_A$

NORMALIZED THERMAL IMPEDANCE $Z_{JC}$
Typical Characteristics (Q2 P-Channel)  \( T_J = 25°C \) unless otherwise noted

![Typical Characteristics (Q2 P-Channel)](image)

Figure 15. On-Region Characteristics

![Normalized on-Resistance vs Drain Current and Gate Voltage](image)

Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

![Normalized On-Resistance vs Junction Temperature](image)

Figure 17. Normalized On-Resistance vs Junction Temperature

![On-Resistance vs Gate to Source Voltage](image)

Figure 18. On-Resistance vs Gate to Source Voltage

![Source to Drain Diode Forward Voltage vs Source Current](image)

Figure 20. Source to Drain Diode Forward Voltage vs Source Current

TJ = 25°C unless otherwise noted
** Typical Characteristics (Q2 P-Channel) \( T_J = 25^\circ C \) unless otherwise noted

** Figure 21. Gate Charge Characteristics**

** Figure 22. Capacitance vs Drain to Source Voltage**

** Figure 23. Unclamped Inductive Switching Capability**

** Figure 24. Gate Leakage Current vs Gate to Source Voltage**

** Figure 25. Maximum Continuous Drain Current vs Ambient Temperature**

** Figure 26. Forward Bias Safe Operating Area**
Typical Characteristics (Q2 P-Channel)  $T_J = 25^\circ C$ unless otherwise noted

Figure 27. Single Pulse Maximum Power Dissipation

- $V_{DS} = 10V$
- $R_{JJA} = 135^\circ C/W$
- $P_{PK}$, PEAK TRANSIENT POWER (W)
- $t$, PULSE WIDTH (s)

For temperatures above 25$^\circ$C derate peak current as follows:

\[
I = I_{25} \left[ \frac{150 - T_A}{125} \right]
\]

$T_A = 25^\circ C$

Figure 28. Transient Thermal Response Curve

- $R_{\theta JA} = 135^\circ C/W$
- Duty cycle descending order
- Normalized thermal impedance, $Z_{\theta JA}$
- $D = t_1/t_2$
- Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JA} + T_A$

Notes:
- Duty factor: $D = t_1/t_2$
- $P_{PK}$, PEAK TRANSIENT POWER (W)
- $V_{GS} = 10V$

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