MOSFET – Dual N-Channel, POWERTRENCH®, SyncFET™

FDS6900AS

General Description

The FDS6900AS is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6900AS contains two unique 30 V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the lowside switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using ON Semiconductor’s monolithic SyncFET technology.

Features

- **Q2**: Optimized to Minimize Conduction Losses Includes SyncFET Schottky Body Diode, 8.2 A, 30 V
  - $R_{DS(on)} = 22 \, \text{m}\Omega$ at $V_{GS} = 10 \, \text{V}$
  - $R_{DS(on)} = 28 \, \text{m}\Omega$ at $V_{GS} = 4.5 \, \text{V}$

- **Q1**: Optimized for Low Switching Losses Low Gate Charge (11 nC typical), 6.9 A, 30 V
  - $R_{DS(on)} = 27 \, \text{m}\Omega$ at $V_{GS} = 10 \, \text{V}$
  - $R_{DS(on)} = 34 \, \text{m}\Omega$ at $V_{GS} = 4.5 \, \text{V}$

- 100% $R_G$ (Gate Resistance) Tested
- These Devices are Pb-Free and are RoHS Compliant

Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Q2</th>
<th>Q1</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$</td>
<td>Drain–Source Voltage</td>
<td>30</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GSS}$</td>
<td>Gate–Source Voltage</td>
<td>±20</td>
<td>±20</td>
<td>V</td>
</tr>
</tbody>
</table>
| $I_D$ | Drain Current
  - Continuous (Note 1a)
  - Pulsed | 8.2 | 6.9 | A |
  | 30 | 20 |
| $P_D$ | Power Dissipation for Dual Operation | 2 | | W |
| Power Dissipation for Single Operation
  (Note 1a) | 1.6 | 1 |
  (Note 1b) | | |
  (Note 1c) | | 0.9 |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range | –55 to +150 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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### THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thJA}$</td>
<td>Thermal Resistance, Junction-to-Ambient (Note 1a)</td>
<td>78</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{thJC}$</td>
<td>Thermal Resistance, Junction-to-Case (Note 1)</td>
<td>40</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### Table 1. ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Type</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BV_{DSS}$</td>
<td>Drain to Source Breakdown Voltage</td>
<td>$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$</td>
<td>Q2</td>
<td>30</td>
<td>30</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$ΔBV_{DSS}/ΔT_J$</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>$I_D = 10 \text{ mA}, V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}, V_{GS} = 25 \text{ °C}$</td>
<td>Q2</td>
<td>27</td>
<td>22</td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Zero Gate Voltage Drain Current</td>
<td>$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$</td>
<td>Q2</td>
<td>500</td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>Gate–Body Leakage Current</td>
<td>$V_{GS} = ±20 \text{ V}, V_{DS} = 0 \text{ V}$</td>
<td>Q2</td>
<td>±100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

### OFF CHARACTERISTICS

### ON CHARACTERISTICS (Note 2)

| $V_{GS(th)}$ | Gate to Source Threshold Voltage               | $V_{GS} = V_{DS}, I_D = 1 \text{ mA}$, $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ | Q2    | 1   | 1.9 | 3   | V     |
| $ΔV_{GS(th)}/ΔT_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 10 \text{ mA}, V_{GS} = 25 \text{ °C}$, $I_D = 250 \mu\text{A}, V_{GS} = 25 \text{ °C}$ | Q2    | 1   | −3.2| 3   | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance              | $V_{DS} = 5 \text{ V}, I_D = 8.2 \text{ A}$, $V_{DS} = 10 \text{ V}, I_D = 6.9 \text{ A}, T_J = 125 \text{ °C}$, $V_{DS} = 4.5 \text{ V}, I_D = 7.6 \text{ A}$ | Q2    | 17  | 22  | 3  | mΩ    |
| $R_{D(on)}$ | On–State Drain Current                         | $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$ | Q2    | 30  | 38  | 3  | A     |
| $g_{FS}$   | Forward Transconductance                       | $V_{DS} = 5 \text{ V}, I_D = 8.2 \text{ A}$, $V_{DS} = 5 \text{ V}, I_D = 6.9 \text{ A}$ | Q2    | 25  | 21  |    | S     |

### DYNAMIC CHARACTERISTICS

| $C_{iss}$ | Input Capacitance                             | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | Q2    | 570 | 600 |    | pF    |
| $C_{oss}$ | Output Capacitance                            |                                             | Q2    | 180 | 150 |    | pF    |
| $C_{rss}$ | Reverse Transfer Capacitance                 |                                             | Q2    | 70  | 70  |    | pF    |
| $R_G$     | Gate Resistance                               |                                             | Q2    | 2.8 | 2.2 | 4.9| Ω     |

### SWITCHING CHARACTERISTICS (Note 2)

<p>| $t_{d(on)}$ | Turn–On Delay Time                            | $V_{DD} = 15 \text{ V}, I_D = 1 \text{ A}, V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \text{ Ω}$ | Q2    | 10  | 19  | 3  | ns    |
| $t_r$      | Turn–On Rise Time                             |                                             | Q2    | 5   | 10  | 8  | ns    |
| $t_{d(off)}$ | Turn–Off Delay Time                          |                                             | Q2    | 26  | 42  | 32 | ns    |
| $t_f$      | Turn–Off Fall Time                            |                                             | Q2    | 3   | 6   | 6  | ns    |</p>
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Type</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{d(on)} )</td>
<td>Turn–On Delay Time</td>
<td>( V_{DD} = 15 , \text{V}, , I_D = 1 , \text{A}, , V_{GS} = 4.5 , \text{V}, , R_{GEN} = 6 , \Omega )</td>
<td>Q2</td>
<td>11</td>
<td>20</td>
<td>19</td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Turn–On Rise Time</td>
<td></td>
<td>Q2</td>
<td>15</td>
<td>27</td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{d(off)} )</td>
<td>Turn–Off Delay Time</td>
<td></td>
<td>Q2</td>
<td>16</td>
<td>29</td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Turn–Off Fall Time</td>
<td></td>
<td>Q2</td>
<td>6</td>
<td>12</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>( Q_{g(TOT)} )</td>
<td>Total Gate Charge at ( V_{GS} = 10 , \text{V} )</td>
<td>Q2: ( V_{DS} = 15 , \text{V}, , I_D = 8.2 , \text{A} ) Q1: ( V_{DS} = 15 , \text{V}, , I_D = 6.9 , \text{A} )</td>
<td>Q2</td>
<td>10</td>
<td>15</td>
<td>11</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_g )</td>
<td>Total Gate Charge at ( V_{GS} = 5 , \text{V} )</td>
<td>Q2: ( V_{GS} = 10 , \text{V} ) Q1: ( V_{GS} = 5 , \text{V} )</td>
<td>Q2</td>
<td>5.8</td>
<td>8.2</td>
<td>6.1</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gs} )</td>
<td>Gate–Source Charge</td>
<td></td>
<td>Q2</td>
<td>1.6</td>
<td>1.7</td>
<td>1.6</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gd} )</td>
<td>Gate–Drain Charge</td>
<td></td>
<td>Q2</td>
<td>2.1</td>
<td>2.2</td>
<td>2.1</td>
<td>nC</td>
</tr>
</tbody>
</table>

### DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

| \( I_S \) | Maximum Continuous Drain–Source Diode Forward Current | Q2   | 2.3 | 1.3 | A    |
| \( T_{rr} \) | Reverse Recovery Time \( I_F = 8.2 \, \text{A}, \, d_{IF}/d_t = 300 \, \text{A/µs} \) (Note 3) | Q2   | 15  | ns  |
| \( Q_{rr} \) | Reverse Recovery Charge | Q2   | 6   | nC  |
| \( T_{rr} \) | Reverse Recovery Time \( I_F = 6.9 \, \text{A}, \, d_{IF}/d_t = 100 \, \text{A/µs} \) (Note 3) | Q1   | 19  | ns  |
| \( Q_{rr} \) | Reverse Recovery Charge | Q1   | 10  | nC  |
| \( V_{SD} \) | Drain–Source Diode Forward Voltage | Q2   | 0.6 | 0.7 | 1.2  |
|        | \( V_{GS} = 0 \, \text{V}, \, I_S = 2.3 \, \text{A} \) (Note 2) | Q2   | 0.7 | 1.0 |
|        | \( V_{GS} = 0 \, \text{V}, \, I_S = 5 \, \text{A} \) (Note 2) | Q1   | 0.7 | 1.2 |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

1. \( R_{\text{JA}} \) is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. \( R_{\text{JC}} \) is guaranteed by design while \( R_{\text{CA}} \) is determined by the user’s board design.

2. Pulse Test: Pulse Width < 300 \, \mu s, Duty cycle < 2.0%.

3. See “SyncFET Schottky body diode characteristics” below.
TYPICAL CHARACTERISTICS: Q2

Figure 1. On−Region Characteristics

Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

Figure 3. On−Resistance Variation with Temperature

Figure 4. On−Resistance Variation with Gate−to−Source Voltage

Figure 5. Transfer Characteristics

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature
TYPICAL CHARACTERISTICS: Q2 (Continued)

**Figure 7. Gate Charge Characteristics**

- $V_{GS} = 10V$
- $V_{GS} = 15V$
- $V_{GS} = 20V$

![Gate Charge Characteristics](image)

**Figure 8. Capacitance Characteristics**

- $f = 1MHz$
- $V_{GS} = 0V$

![Capacitance Characteristics](image)

**Figure 9. Maximum Safe Operating Area**

- $V_{DS} = 10V$
- $V_{DS} = 15V$
- $V_{DS} = 20V$

![Maximum Safe Operating Area](image)

**Figure 10. Single Pulse Maximum Power Dissipation**

- $R_{DS(on)} = 150°C/W$
- $T_A = 25°C$

![Single Pulse Maximum Power](image)

**Figure 11. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.
TYPICAL CHARACTERISTICS: Q1

Figure 12. On−Region Characteristics

Figure 13. On−Resistance Variation with Drain Current and Gate Voltage

Figure 14. On−Resistance Variation with Temperature

Figure 15. On−Resistance Variation with Gate−to−Source Voltage

Figure 16. Transfer Characteristics

Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature
TYPICAL CHARACTERISTICS: Q1 (Continued)

Figure 18. Gate Charge Characteristics

Figure 19. Capacitance Characteristics

Figure 20. Maximum Safe Operating Area

Figure 21. Single Pulse Maximum Power Dissipation

Figure 22. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.
SyncFET Schottky Body Diode Characteristics

ON Semiconductor’s SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 23 shows the reverse recovery characteristic of the FDS6900AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

Figure 23. FDS6900AS SyncFET Body Diode Reverse Recovery Characteristics

For comparison purposes, Figure 24 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690).

Figure 24. Non−SyncFET (FDS6690) Body Diode Reverse Recovery Characteristics
TYPICAL CHARACTERISTICS (Continued)

Figure 26. Unclamped Inductive Load Test Circuit

Figure 27. Unclamped Inductive Waveforms

Figure 28. Gate Charge Test Circuit

Figure 29. Gate Charge Waveform

Figure 30. Switching Time Test Circuit

Figure 31. Switching Time Waveform

Pulse Width

Pulse Width

Pulse Width

Pulse Width

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC8
CASE 751EB
ISSUE A
DATE 24 AUG 2017

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DOCUMENT NUMBER: 98AON13735G
DESCRIPTION: SOIC8

SEE DETAIL A

DETAIL A
SCALE: 1:1

0.42±0.09
0.22±0.03
0.175±0.075
1.75 MAX

OPTION A - BEVEL EDGE

OPTION B - NO BEVEL EDGE

GAGE PLANE
(0.43) x 45°

R0.10

R0.10

8° 0°

SEATING PLANE
0.65±0.25
(1.04)

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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