



ON Semiconductor®

## FDP8874

### N-Channel PowerTrench® MOSFET 30V, 114A, 5.3mΩ

#### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(ON)}$  and fast switching speed.

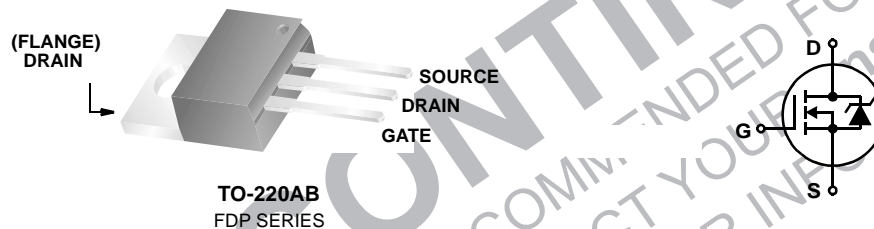
#### Applications

- DC/DC converters



#### Features

- $r_{DS(ON)} = 5.3m\Omega$ ,  $V_{GS} = 10V$ ,  $I_D = 40A$
- $r_{DS(ON)} = 6.6m\Omega$ ,  $V_{GS} = 4.5V$ ,  $I_D = 40A$
- High performance trench technology for extremely low  $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant



#### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 10V$ ) (Note 1)	114	A
	Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 4.5V$ ) (Note 1)	102	A
	Continuous ( $T_{amb} = 25^\circ C$ , $V_{GS} = 10V$ , with $R_{\theta JA} = 62^\circ C/W$ )	16	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	105	mJ
$P_D$	Power dissipation	110	W
	Derate above $25^\circ C$	0.73	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ C$

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220	1.36	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220 ( Note 3)	62	$^\circ C/W$

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8874	FDP8874	TO-220AB	Tube	N/A	50 units

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$T_C = 150^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 40\text{A}$ , $V_{GS} = 10\text{V}$	-	0.0036	0.0053	$\Omega$
		$I_D = 40\text{A}$ , $V_{GS} = 4.5\text{V}$	-	0.0045	0.0066	
		$I_D = 40\text{A}$ , $V_{GS} = 10\text{V}$ , $T_J = 175^\circ\text{C}$	-	0.0062	0.0090	

**Dynamic Characteristics**

$C_{ISS}$	Input Capacitance	$V_{DS} = 15\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	3130	-	pF
$C_{OSS}$	Output Capacitance		-	590	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	345	-	pF
$R_G$	Gate Resistance	$V_{GS} = 0.5\text{V}$ , $f = 1\text{MHz}$	-	1.9	-	$\Omega$
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	56	72	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V	-	30	38	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V	-	3.0	4.0	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 15\text{V}$ $I_D = 40\text{A}$ $I_g = 1.0\text{mA}$	-	9.0	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	6.0	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	11	-	nC

**Switching Characteristics** ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 15\text{V}$ , $I_D = 40\text{A}$ $V_{GS} = 4.5\text{V}$ , $R_{GS} = 4.7\Omega$	-	-	207	ns
$t_{d(ON)}$	Turn-On Delay Time		-	10	-	ns
$t_r$	Rise Time		-	128	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	44	-	ns
$t_f$	Fall Time		-	31	-	ns
$t_{OFF}$	Turn-Off Time		-	-	112	ns

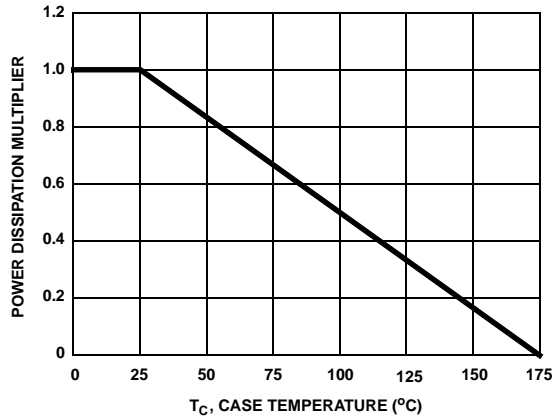
**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 40\text{A}$	-	-	1.25	V
		$I_{SD} = 20\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 40\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	32	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 40\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	18	nC

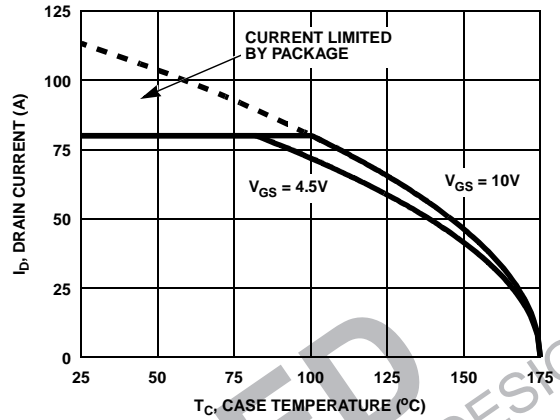
**Notes:**

- 1: Package current limitation is 80A.
- 2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 51\mu\text{H}$ ,  $I_{AS} = 64\text{A}$ ,  $V_{DD} = 27\text{V}$ ,  $V_{GS} = 10\text{V}$ .
- 3: Pulse width = 100s.

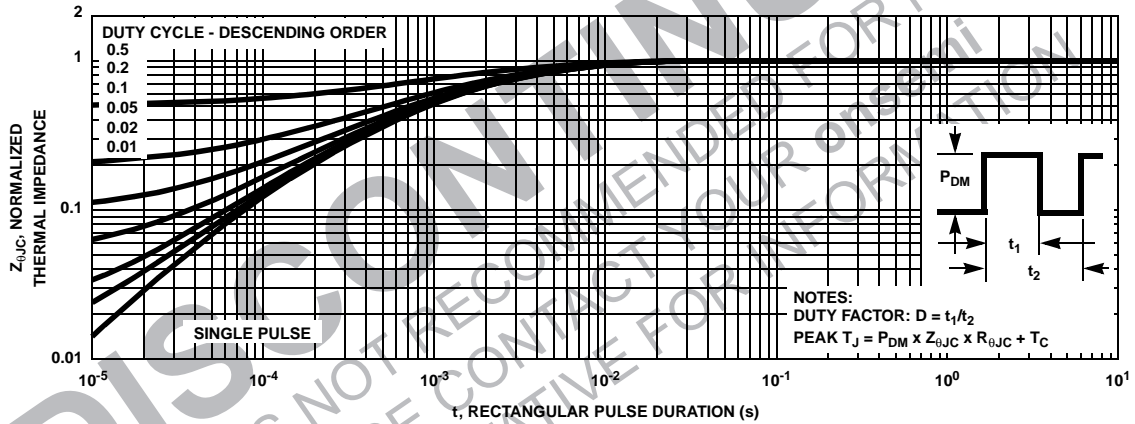
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



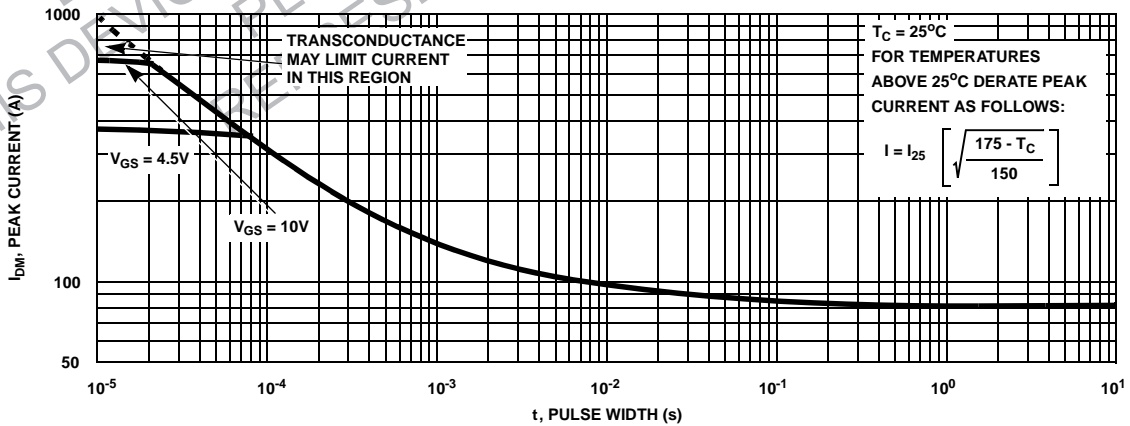
**Figure 1. Normalized Power Dissipation vs Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

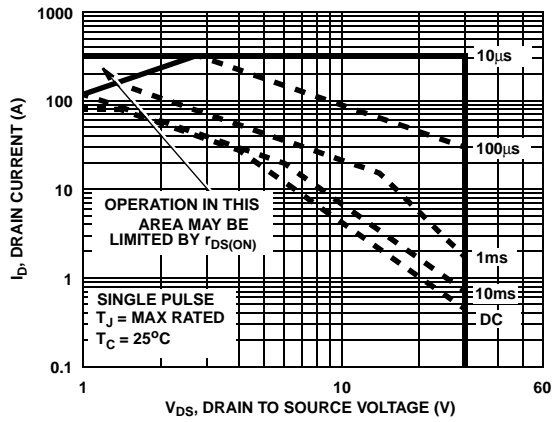


**Figure 3. Normalized Maximum Transient Thermal Impedance**

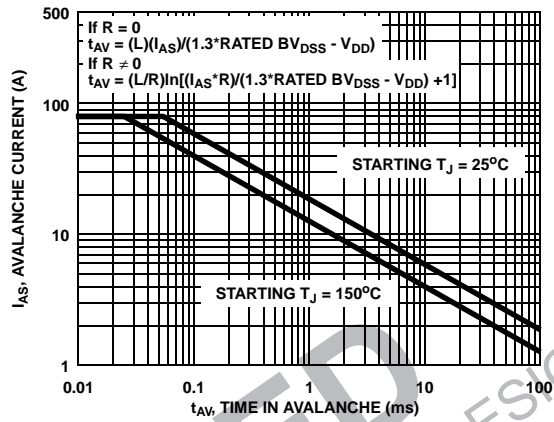


**Figure 4. Peak Current Capability**

**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

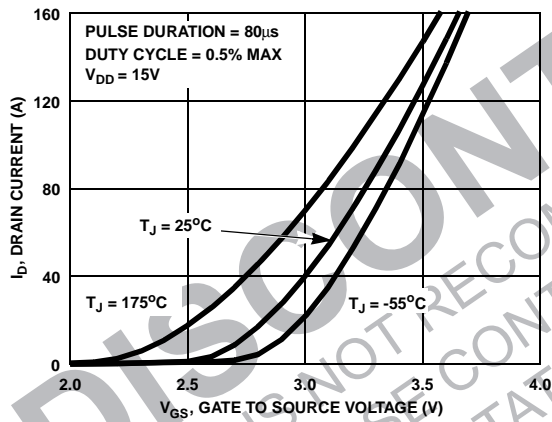


**Figure 5. Forward Bias Safe Operating Area**

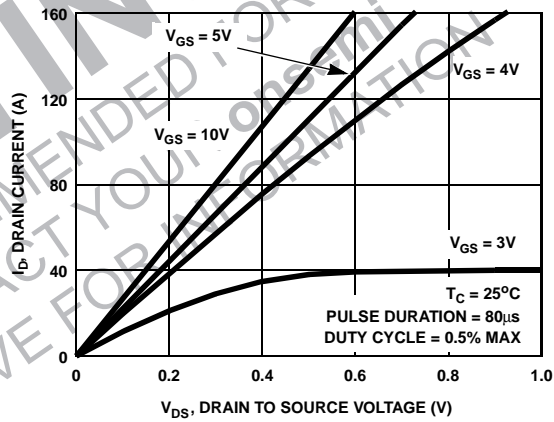


**Figure 6. Unclamped Inductive Switching Capability**

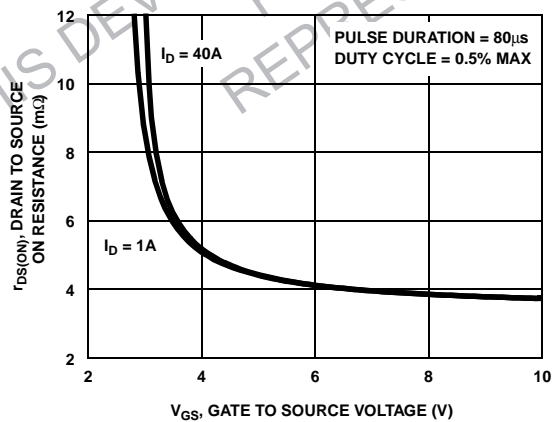
NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515



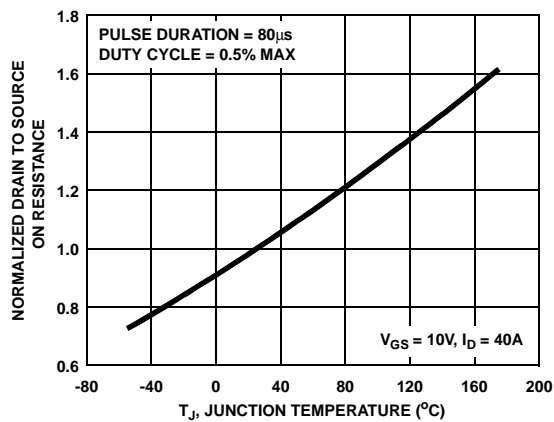
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

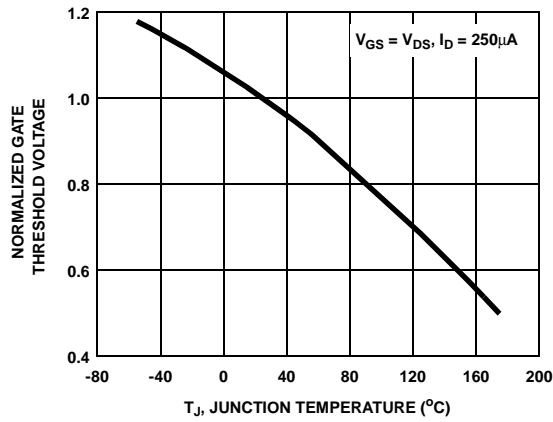


**Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current**

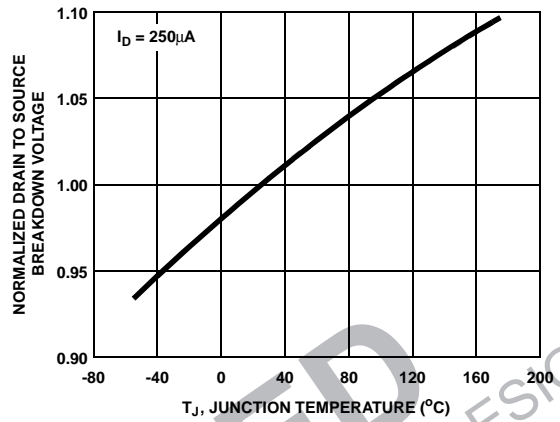


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

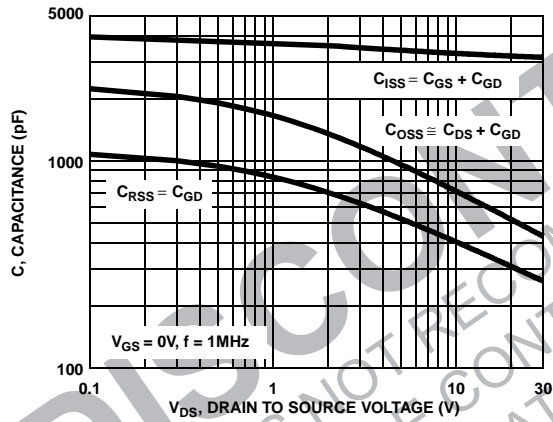
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



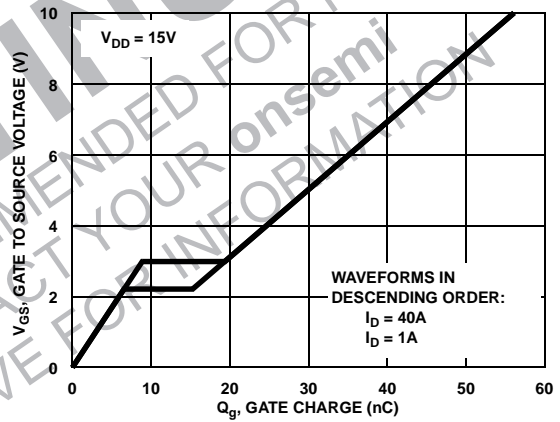
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Current**

Test Circuits and Waveforms

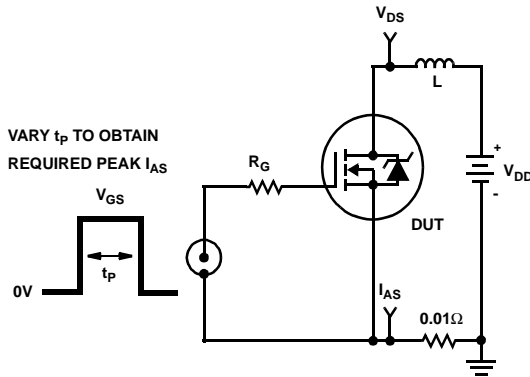


Figure 15. Unclamped Energy Test Circuit

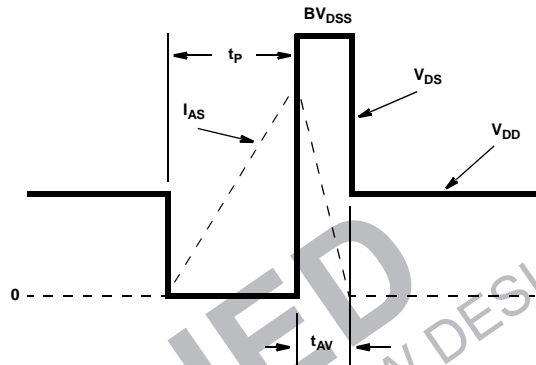


Figure 16. Unclamped Energy Waveforms

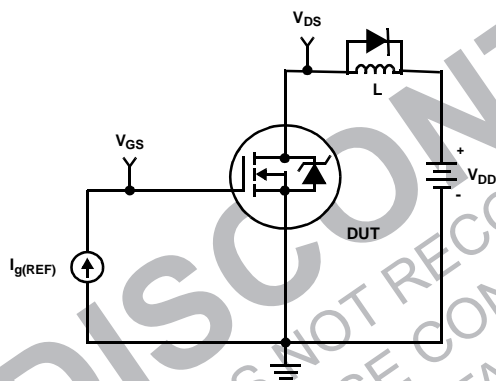


Figure 17. Gate Charge Test Circuit

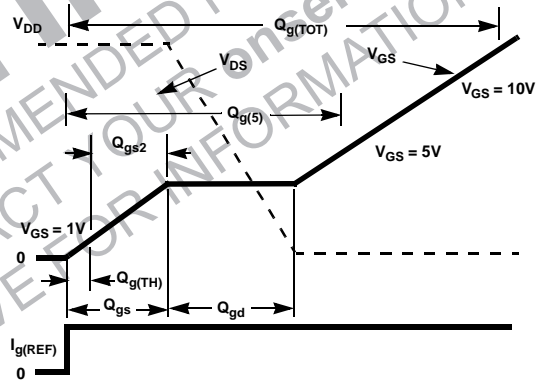


Figure 18. Gate Charge Waveforms

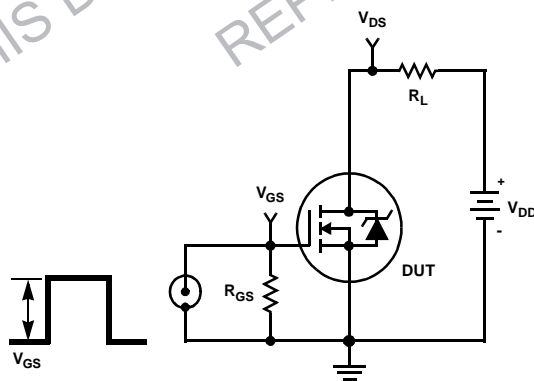


Figure 19. Switching Time Test Circuit

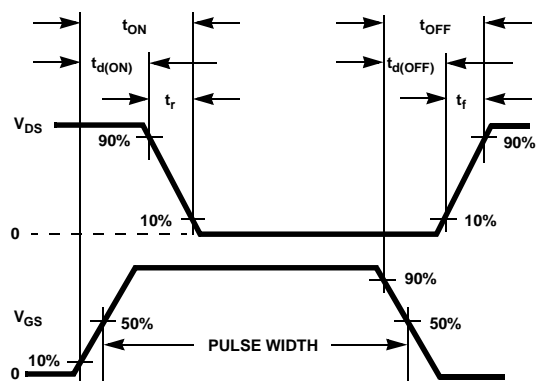


Figure 20. Switching Time Waveforms

**PSPICE Electrical Model**

.SUBCKT FDP8874 2 1 3 ; rev May 2004  
 Ca 12 8 2.3e-9  
 Cb 15 14 2.25e-9  
 Cin 6 8 2.9e-9

Dbody 7 5 DbodyMOD  
 Dbreak 5 11 DbreakMOD  
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 33.3  
 Eds 14 8 5 8 1  
 Egs 13 8 6 8 1  
 Esg 6 10 6 8 1  
 Evthres 6 21 19 8 1  
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 8.5e-9  
 Ldrain 2 5 1.0e-9  
 Lsource 3 7 2.7e-9

RLgate 1 9 85  
 RLdrain 2 5 10  
 RLsource 3 7 27

Mmed 16 6 8 8 MmedMOD  
 Mstro 16 6 8 8 MstroMOD  
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
 Rdrain 50 16 RdrainMOD 1.7e-3  
 Rgate 9 20 1.9  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 Rsource 8 7 RsourceMOD 1.7e-3  
 Rvthres 22 8 RvthresMOD 1  
 Rvtemp 18 19 RvtempMOD 1  
 S1a 6 12 13 8 S1AMOD  
 S1b 13 12 13 8 S1BMOD  
 S2a 6 15 14 13 S2AMOD  
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))/(1e-6\*500),10))}}

.MODEL DbodyMOD D (IS=4.1E-12 IKF=10 N=1.01 RS=2e-3 TRS1=8e-4 TRS2=2e-7  
 + CJO=1.22e-9 M=0.57 TT=3e-12 XTl=3)

.MODEL DbreakMOD D (RS=8e-2 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=1.12e-9 IS=1e-30 N=10 M=0.42)

.MODEL MmedMOD NMOS (VTO=2 KP=9 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.9)

.MODEL MstroMOD NMOS (VTO=2.5 KP=390 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=1.72 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=19 RS=0.1)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-8e-7)

.MODEL RdrainMOD RES (TC1=7e-3 TC2=3.8e-6)

.MODEL RSLCMOD RES (TC1=1e-4 TC2=1e-6)

.MODEL RsourceMOD RES (TC1=1e-4 TC2=2.5e-6)

.MODEL RvthresMOD RES (TC1=-2.4e-3 TC2=-8e-6)

.MODEL RvtempMOD RES (TC1=-1.8e-3 TC2=2e-7)

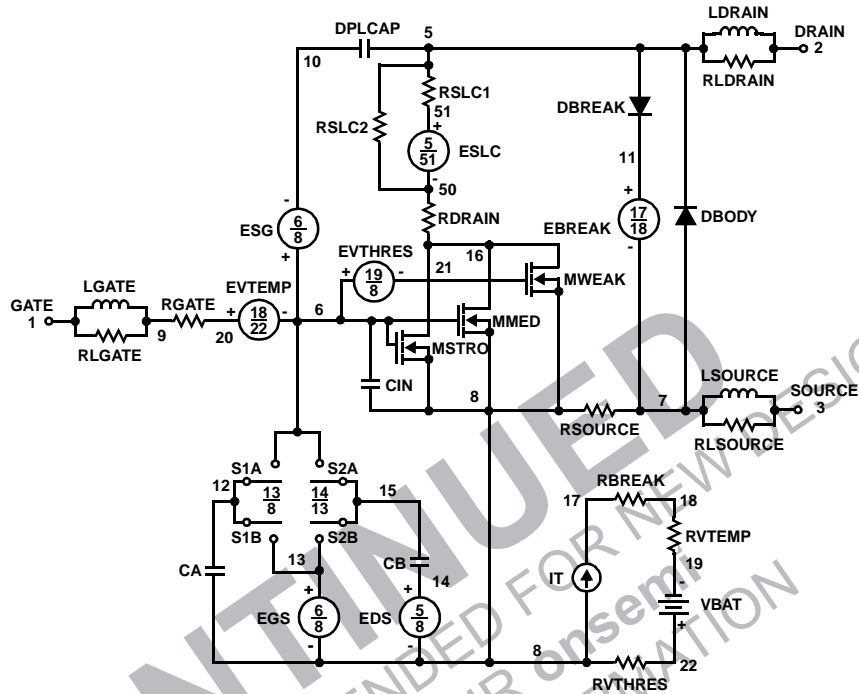
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3)

.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2)

.ENDS



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

### SABER Electrical Model

rev May 2004  
 template FDP8874 n2,n1,n3  
 electrical n2,n1,n3

```

{
  var i iscl
  dp..model dbodymod = (isl=4.1e-12,ikf=10,nl=1.01,rs=2e-3,trs1=8e-4,trs2=2e-7,cjo=1.22e-9,m=0.57,tt=3e-12,xti=3)
  dp..model dbreakmod = (rs=8e-2,trs1=1e-3,trs2=-8.9e-6)
  dp..model dplcapmod = (cjo=1.12e-9,isl=10e-30,nl=10,m=0.42)
  m..model mmedmod = (type=_n,vto=2,kp=9, is=1e-30, tox=1)
  m..model mstrongmod = (type=_n,vto=2.5,kp=390, is=1e-30, tox=1)
  m..model mweakmod = (type=_n,vto=1.72,kp=0.05, is=1e-30, tox=1,rs=0.1)
  sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3)
  sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)
  sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5)
  sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2)
  c.ca n12 n8 = 2.3e-9
  c.cb n15 n14 = 2.25e-9
  c.cin n6 n8 = 2.9e-9
  
```

```

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
  
```

```

spe.ebreak n11 n7 n17 n18 = 33.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
  
```

```
i.it n8 n17 = 1
```

```

l.lgate n1 n9 = 8.5e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2.7e-9
  
```

```

res.rlgate n1 n9 = 85
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 27
  
```

```

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
  
```

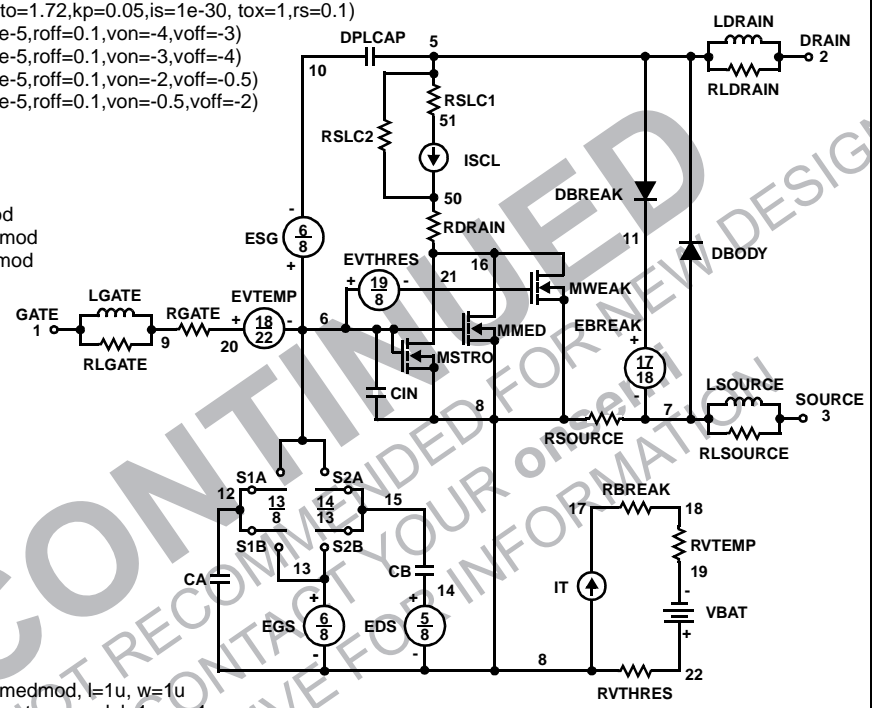
```

res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-8e-7
res.rdrain n50 n16 = 1.7e-3, tc1=7e-3,tc2=3.8e-6
res.rgate n9 n20 = 1.9
res.rslc1 n5 n51 = 1e-6, tc1=1e-4,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.7e-3, tc1=1e-4,tc2=2.5e-6
res.rvthres n22 n8 = 1, tc1=-2.4e-3,tc2=-8e-6
res.rvtemp n18 n19 = 1, tc1=-1.8e-3,tc2=2e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
  
```

```
v.vbat n22 n19 = dc=1
```

```

equations {
  i (n51->n50) +=iscl
  iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51)))))*((abs(v(n5,n51))*1e6/500)** 10)
}
}
  
```





**PSPICE Thermal Model**

REV 23 May 2004

FDP8874T

CTHERM1 TH 6 1.9e-3  
 CTHERM2 6 5 2.8e-3  
 CTHERM3 5 4 3.5e-3  
 CTHERM4 4 3 3.6e-3  
 CTHERM5 3 2 4.0e-3  
 CTHERM6 2 TL 1.6e-2

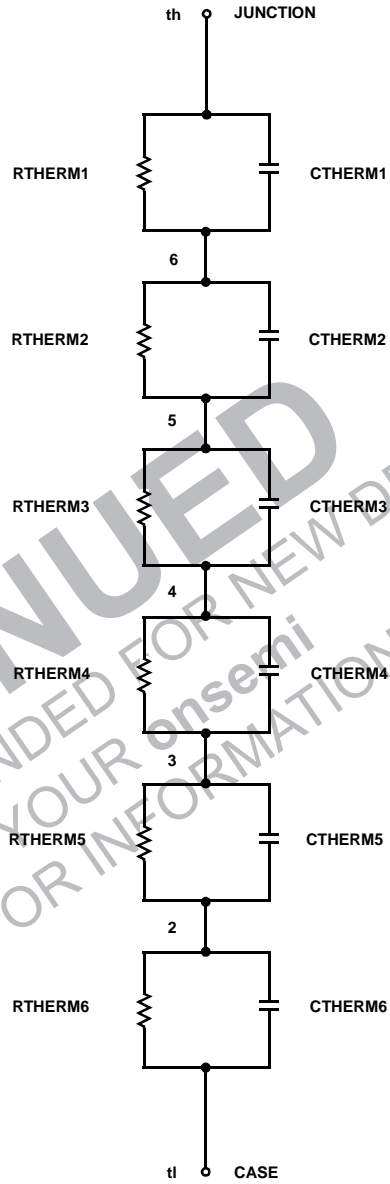
RTHERM1 TH 6 3.8e-2  
 RTHERM2 6 5 5.0e-2  
 RTHERM3 5 4 1.0e-1  
 RTHERM4 4 3 1.8e-1  
 RTHERM5 3 2 3.5e-1  
 RTHERM6 2 TL 3.7e-1

**SABER Thermal Model**

SABER thermal model FDP8874T  
 template thermal\_model th tl  
 thermal\_c th, tl

```
{
ctherm.ctherm1 th 6 =1.9e-3
ctherm.ctherm2 6 5 =2.8e-3
ctherm.ctherm3 5 4 =3.5e-3
ctherm.ctherm4 4 3 =3.6e-3
ctherm.ctherm5 3 2 =4.0e-3
ctherm.ctherm6 2 tl =1.6e-2
```


```
rtherm.rtherm1 th 6 =3.8e-2
rtherm.rtherm2 6 5 =5.0e-2
rtherm.rtherm3 5 4 =1.0e-1
rtherm.rtherm4 4 3 =1.8e-1
rtherm.rtherm5 3 2 =3.5e-1
rtherm.rtherm6 2 tl =3.7e-1
}
```



DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN  
 PLEASE CONTACT YOUR ONSEMI REPRESENTATIVE FOR INFORMATION

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