FDP4D5N10C / FDPF4D5N10C
N-Channel Shielded Gate PowerTrench® MOSFET
100 V, 128 A, 4.5 mΩ

Features
- Max $r_{DS(on)} = 4.5$ mΩ at $V_{GS} = 10$ V, $I_D = 100$ A
- Extremely Low Reverse Recovery Charge, $Q_{rr}$
- 100% UIL Tested
- RoHS Compliant

General Description
This N-Channel MV MOSFET is produced using ON Semiconductor’s advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MOSFET Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain to Source Voltage</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current</td>
<td>128</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Continuous, $T_J = 25°C$</td>
<td>(Note 3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Continuous, $T_J = 100°C$</td>
<td>(Note 3)</td>
<td></td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single Pulse Avalanche Energy</td>
<td>486</td>
<td>mJ</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation</td>
<td>150</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>$T_C = 25°C$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Dissipation</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = 25°C$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_J, T_{STG}$</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
</tbody>
</table>

* Drain current limited by maximum junction temperature. Package limitation current is 120A.

Thermal Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>FDP4D5N10C</th>
<th>FDPF4D5N10C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUC}$</td>
<td>Thermal Resistance, Junction to Case</td>
<td>1.0</td>
<td>4.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JUA}$</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>62.5</td>
<td>62.5</td>
<td></td>
</tr>
</tbody>
</table>

Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Packing Mode</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDP4D5N10C</td>
<td>FDP4D5N10C</td>
<td>TO-220</td>
<td>Tube</td>
<td>50 units</td>
</tr>
<tr>
<td>FDPF4D5N10C</td>
<td>FDPF4D5N10C</td>
<td>TO-220F</td>
<td>Tube</td>
<td>50 units</td>
</tr>
</tbody>
</table>
### Electrical Characteristics

Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units
--- | --- | --- | --- | --- | --- | ---
$BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D = 250 \mu A, V_{GS} = 0 \, V$ | 100 | | | V
$\Delta BV_{DSS}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu A$, referenced to 25 °C | 53 | | | mV/°C
$I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS} = 80 \, V, V_{GS} = 0 \, V$ | 1 | | | µA
$I_{GSS}$ | Gate to Source Leakage Current | $V_{GS} = \pm 20 \, V, V_{DS} = 0 \, V$ | ±100 | | | nA

### Off Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
</table>
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 310 \mu A$ | 2.0 | 3.2 | 4.0 | V
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10 \, V, I_D = 100 \, A$ | 4.0 | 4.5 | | mΩ
| $g_{FS}$ | Forward Transconductance | $V_{DS} = 5 \, V, I_D = 100 \, A$ | 134 | | | S

### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
</table>
| $C_{iss}$ | Input Capacitance | $V_{DS} = 50 \, V, V_{GS} = 0 \, V$, $f = 1 \, MHz$ | 3615 | 5065 | | pF
| $C_{oss}$ | Output Capacitance | | 2330 | 3265 | | pF
| $C_{rss}$ | Reverse Transfer Capacitance | | 18 | 35 | | pF
| $R_{g}$ | Gate Resistance | | 0.1 | 1.1 | 2.2 | Ω

### Switching Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
</table>
| $td(on)$ | Turn-On Delay Time | $V_{DD} = 50 \, V, I_P = 100 \, A$, $V_{GS} = 10 \, V, R_{GEN} = 6 \, \Omega$ | 29 | 47 | | ns
| $tr$ | Rise Time | $V_{DD} = 50 \, V, I_P = 100 \, A$, $V_{GS} = 10 \, V$ | 49 | 79 | | ns
| $td(off)$ | Turn-Off Delay Time | $V_{GS} = 0 \, V, I_D = 100 \, A$ | 41 | 66 | | ns
| $tf$ | Fall Time | | 13 | 24 | | ns
| $Q_{g}$ | Total Gate Charge | $V_{DD} = 0 \, V$ to $10 \, V$ | 48 | 68 | | nC
| $Q_{gs}$ | Gate to Source Gate Charge | $V_{DD} = 50 \, V, I_D = 100 \, A$ | 19 | | | nC
| $Q_{gd}$ | Gate to Drain "Miller" Charge | | 9 | | | nC
| $Q_{oss}$ | Output Charge | $V_{DD} = 50 \, V, V_{GS} = 0 \, V$ | 150 | | | nC

### Drain-Source Diode Characteristic

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
</table>
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 128 | A
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 512 | A
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0 \, V, I_S = 100 \, A$ | 1.0 | 1.3 | | V
| $I_{tr}$ | Reverse Recovery Time | $V_{GS} = 0 \, V, V_{DD} = 50 \, V$ | 82 | 132 | | ns
| $Q_{tr}$ | Reverse Recovery Charge | $I_T = 100 \, A$, $dI_T/dt = 100 \, A/\mu s$ | 106 | 170 | | nC
| $I_{tr}$ | Reverse Recovery Time | $V_{GS} = 0 \, V, V_{DD} = 50 \, V$ | 71 | 114 | | ns
| $Q_{tr}$ | Reverse Recovery Charge | $I_T = 100 \, A$, $dI_T/dt = 300 \, A/\mu s$ | 258 | 413 | | nC

**Notes:**

1. Pulsed Id please refer to Figure "Forward Bias Safe Operating Area" for more details.
2. $E_{AS}$ of 486 mJ is based on starting $T_J = 25 \, ^\circ C$, $L = 3 \, mH$, $I_{AS} = 18 \, A$, $V_{DD} = 100 \, V$, $V_{GS} = 10 \, V$. 100% test at $L = 0.1 \, mH$, $I_{AS} = 58 \, A$.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
**Typical Characteristics** $T_J = 25\, ^\circ\text{C}$ unless otherwise noted.

**Figure 1.** On Region Characteristics

**Figure 2.** Normalized On-Resistance vs. Drain Current and Gate Voltage

**Figure 3.** Normalized On Resistance vs. Junction Temperature

**Figure 4.** On-Resistance vs. Gate to Source Voltage

**Figure 5.** Transfer Characteristics

**Figure 6.** Source to Drain Diode Forward Voltage vs. Source Current
Typical Characteristics $T_J = 25\, ^\circ C$ unless otherwise noted.

- **Figure 7.** Gate Charge Characteristics
- **Figure 8.** Capacitance vs. Drain to Source Voltage
- **Figure 9.** Unclamped Inductive Switching Capability
- **Figure 10.** Maximum Continuous Drain Current vs. Case Temperature
- **Figure 11.** Forward Bias Safe Operating Area for FDP4D5N10C
- **Figure 12.** Forward Bias Safe Operating Area for FDP4D5N10C
Typical Characteristics \( T_J = 25 \, ^\circ C \) unless otherwise noted.

Figure 13. Single Pulse Maximum Power Dissipation for FDP4D5N10C

Figure 14. Single Pulse Maximum Power Dissipation for FDPF4D5N10C

Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP4D5N10C

Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF4D5N10C
Dimensional Outline and Pad Layout

TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)
Dimensional Outline and Pad Layout

TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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