FDMC8878

N-Channel POWERTRENCH® MOSFET

30 V, 16.5 A, 14 mΩ

This N−Channel MOSFET is a rugged gate version of ON Semiconductor's advanced PowerTrench process. It has been optimized for power management applications.

Features

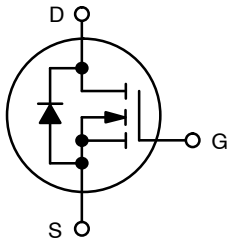
- $R_{DS(on)}$ = 14 mΩ (Max.) @ V_{GS} = 10 V, I_D = 9.6 A
- $R_{DS(on)}$ = 17 mΩ (Max.) @ V_{GS} = 4.5 V, I_D = 8.7 A
- Low Profile − 0.8 mm Max in MLP 3.3 x 3.3
- These Devices are Pb−Free and are RoHS Compliant

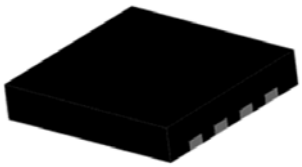
Application

- DC − DC Conversion

ON Semiconductor®

www.onsemi.com





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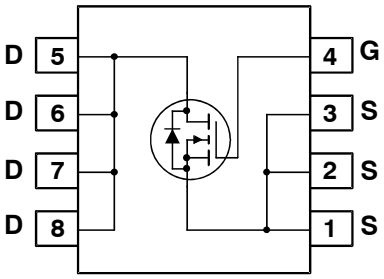


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DS}	30	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C (Package limited)	I_D	16.5	A
	T_C = 25°C (Silicon limited)		38	
	T_A = 25°C (Figure 1)		9.6	
Drain Current	Pulsed	I_D	60	A
Power Dissipation	T_C = 25°C	P_D	31	W
	T_A = 25°C (Figure 1)		2.1	
Operating and Storage Junction Temperature Range		T_J, T_{STG}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	4	°C/W
Thermal Resistance, Junction−to−Ambient (Figure 1)	$R_{\theta JA}$	60	

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 1 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

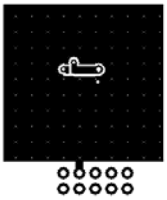
Part Number	Top Mark	Package	Reel Size	Tape Width	Quantity
FDMC8878	FDMC8878	MLP 3.3 x 3.3	13″	12 mm	3000 units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	20	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C	–	–	100	
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = V_{DS}	1	1.7	3	V
$\Delta BV_{DSS}/\Delta T_J$	Gate−to−Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	−5.7	–	mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 9.6 A	–	9.6	14.0	mΩ
		V_{GS} = 4.5 V, I_D = 8.7 A	–	12.1	17.0	
		V_{GS} = 10 V, I_D = 9.6 A, T_J = 125°C	–	13.5	20.0	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 9.6 A	–	35	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	1000	1230	pF
C_{oss}	Output Capacitance		–	183	255	pF
C_{rss}	Reverse Transfer Capacitance		–	118	180	pF
R_g	Reverse Transfer Capacitance	f = 1 MHz	–	1.1	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 9.6 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	8	16	ns
t_r	Rise Time		–	4	10	
$t_{d(off)}$	Turn−Off Delay Time		–	20	36	
t_f	Fall Time		–	3	10	
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 10 V, V_{DD} = 15 V, I_D = 9.6 A	–	18	26	nC
Q_{gs}	Gate−to−Source Gate Charge		–	2.8	–	
Q_{gd}	Gate−to−Drain “Miller” Charge		–	3.9	–	
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 9.6 A (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9.6 A, di/dt = 100 A/μs	–	23	35	ns
Q_{rr}	Reverse Recovery Charge		–	14	21	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

Figure 1.

b. 135°C/W when mounted on a minimum pad of 2 oz copper

Figure 2.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

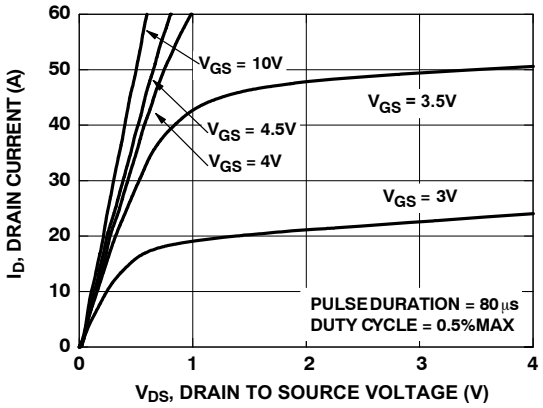


Figure 3. Gate Charge Characteristics

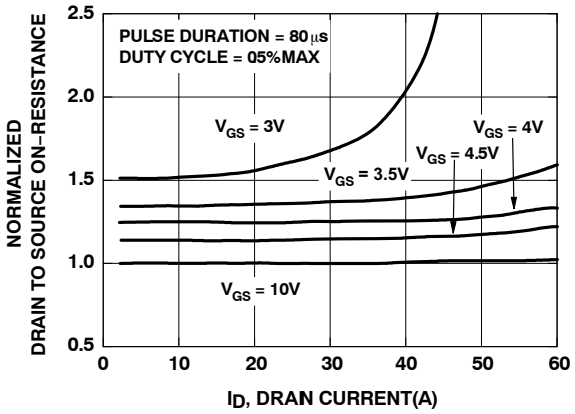


Figure 4. Capacitance vs. Drain to Source Voltage

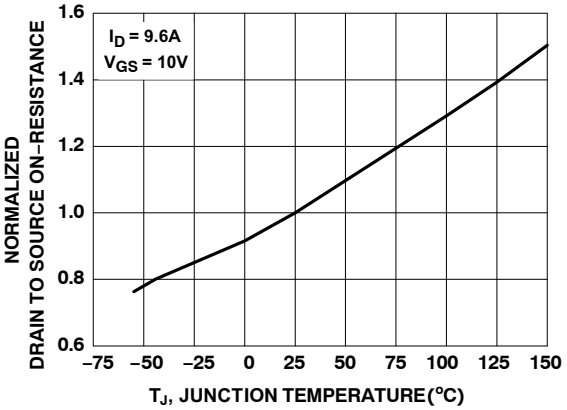


Figure 5. Unclamped Inductive Switching Capability

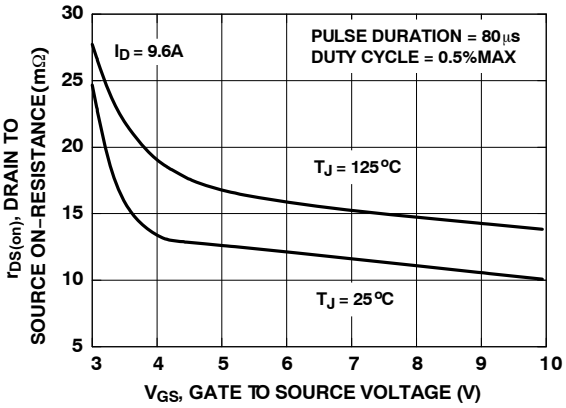


Figure 6. Maximum Continuous Drain Current vs. Ambient Temperature

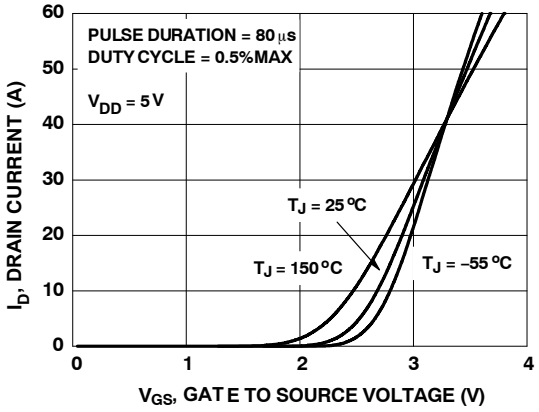


Figure 7. Forward Bias Safe Operating Area

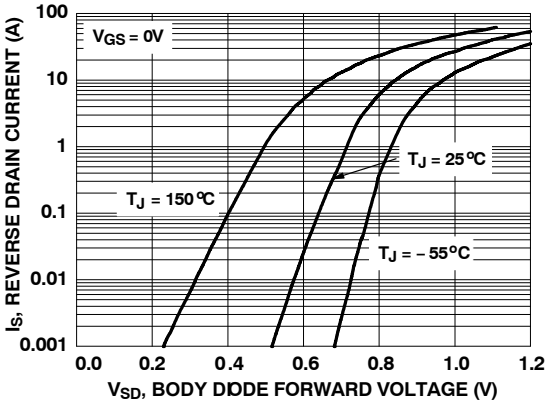


Figure 8. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

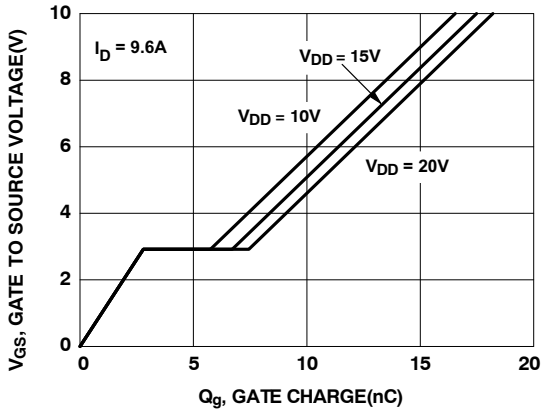


Figure 9. On−Region Characteristics

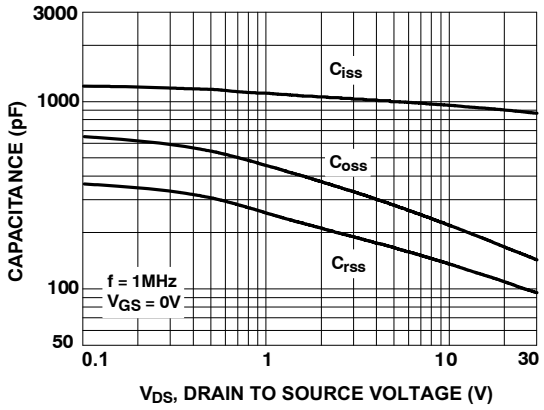


Figure 10. Transfer Characteristics

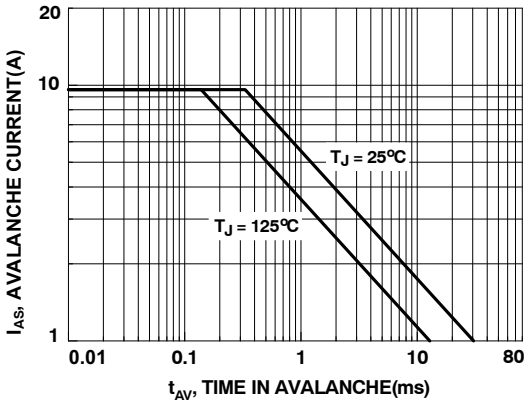


Figure 11. On−Resistance Variation vs. Drain Current and Gate Voltage

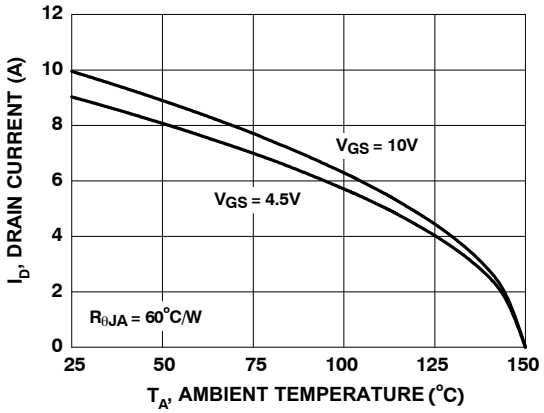


Figure 12. Body Diode Forward Voltage Variation vs. Source Current and Temperature

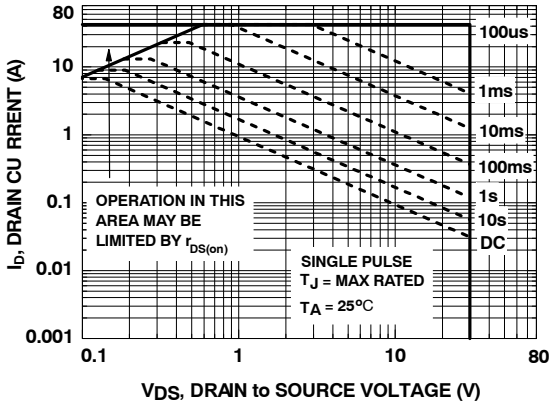


Figure 13. Capacitance Characteristics

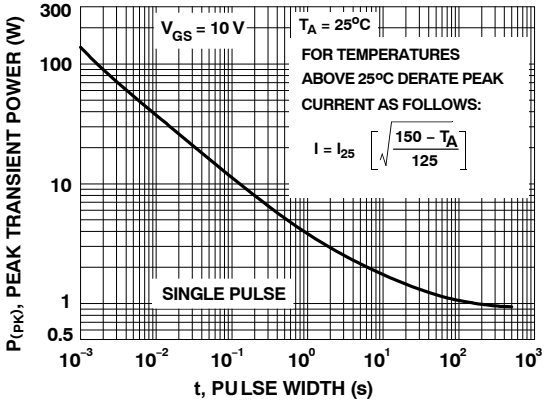


Figure 14. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

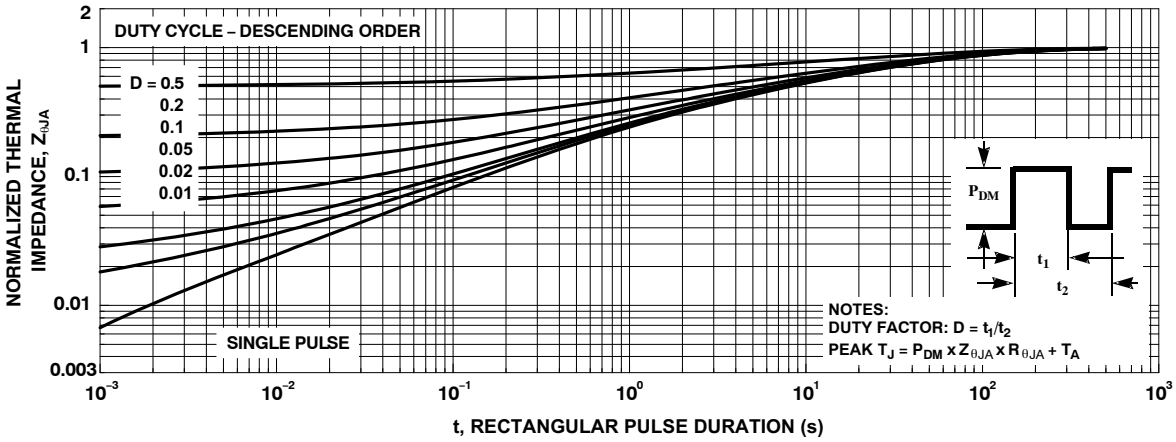


Figure 15. Transient Thermal Response Curve

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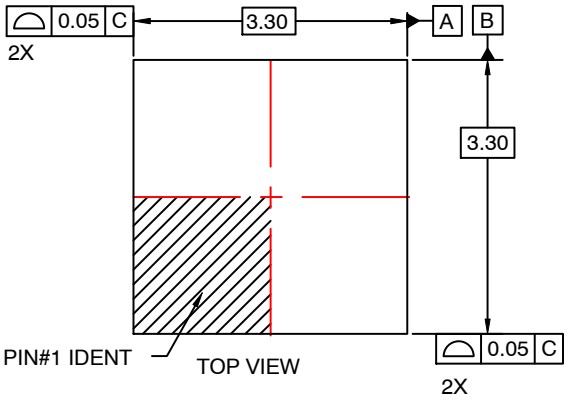
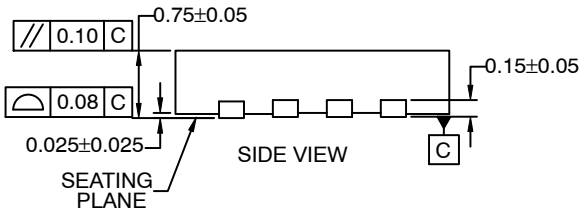
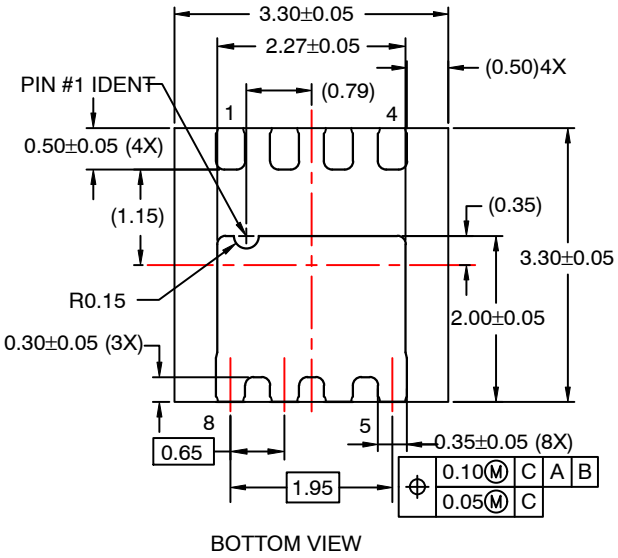
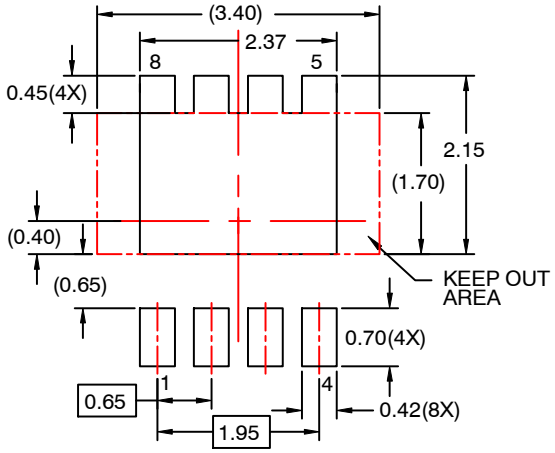






BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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