

MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 22 mΩ and 10 mΩ

FDMC7200S

General Description

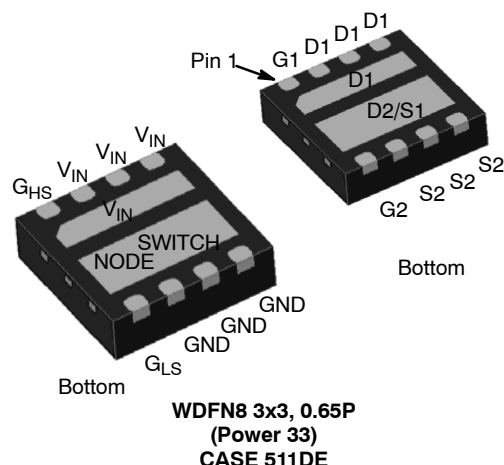
This device includes two specialized N-Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Features

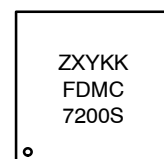
- Q1: N-Channel
 - ◆ Max $R_{DS(on)}$ = 22 m Ω at V_{GS} = 10 V, I_D = 6 A
 - ◆ Max $R_{DS(on)}$ = 34 m Ω at V_{GS} = 4.5 V, I_D = 5 A
- Q2: N-Channel
 - ◆ Max $R_{DS(on)}$ = 10 m Ω at V_{GS} = 10 V, I_D = 8.5 A
 - ◆ Max $R_{DS(on)}$ = 13.5 m Ω at V_{GS} = 4.5 V, I_D = 7.2 A
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load

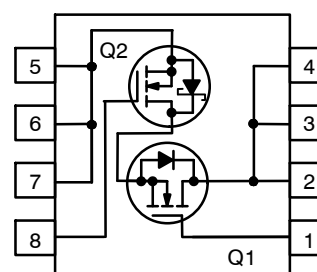


MARKING DIAGRAM



Z = Assembly Plant Code
 XY = Date Code
 KK = Lot Run Traceability Code
 EDMC7200S = Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping [†]
FDMC7200S	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Q1	Q2	Unit
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	± 20	V
I_D	Drain Current – Continuous (Package Limited) $T_C = 25^\circ\text{C}$	18	13	A
	– Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	23	46	
	– Continuous $T_A = 25^\circ\text{C}$	7 (Note 1a)	13 (Note 1b)	
	– Pulsed	40	27	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	12	32	mJ
P_D	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	1.9 (Note 1a)	2.5 (Note 1b)	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	0.7 (Note 1c)	1.0 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 (Note 1a)	50 (Note 1b)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 (Note 1c)	125 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	4.2	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$ $I_D = 1\ \text{mA}, V_{GS} = 0\ \text{V}$	Q1 Q2	30 30	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C $I_D = 1\ \text{mA}$, referenced to 25°C	Q1 Q2	– –	14 13	– –	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$	Q1 Q2	– –	– –	1 500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$	Q1 Q2	– –	– –	100 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$ $V_{GS} = V_{DS}, I_D = 1\ \text{mA}$	Q1 Q2	1.0 1.0	2.3 2.0	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C $I_D = 1\ \text{mA}$, referenced to 25°C	Q1 Q2	– –	–5 –6	– –	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 6\ \text{A}$ $V_{GS} = 4.5\ \text{V}, I_D = 5\ \text{A}$ $V_{GS} = 10\ \text{V}, I_D = 6\ \text{A}, T_J = 125^\circ\text{C}$	Q1	– – –	17 25 23	22 34 30	m Ω
		$V_{GS} = 10\ \text{V}, I_D = 8.5\ \text{A}$ $V_{GS} = 4.5\ \text{V}, I_D = 7.2\ \text{A}$ $V_{GS} = 10\ \text{V}, I_D = 8.5\ \text{A}, T_J = 125^\circ\text{C}$	Q2	– – –	7.8 10.3 11.4	10.0 13.5 13.1	
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 6\ \text{A}$	Q1	–	29	–	S
		$V_{DD} = 5\ \text{V}, I_D = 8.5\ \text{A}$	Q2	–	43	–	

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Q1	–	495	660	pF
			Q2	–	1080	1436	
C _{oss}	Output Capacitance		Q1	–	145	195	pF
			Q2	–	373	495	
C _{rss}	Reverse Transfer Capacitance		Q1	–	20	30	pF
			Q2	–	35	52	
R _g	Gate Resistance	f = 1 MHz	Q1	0.2	1.4	4.2	Ω
			Q2	0.2	1.2	3.6	

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω Q2 V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	Q1	–	11	20	ns
			Q2	–	7.6	15	
t _r	Rise Time		Q1	–	3.1	10	ns
			Q2	–	1.8	10	
t _{d(off)}	Turn-Off Delay Time		Q1	–	35	56	ns
			Q2	–	21	34	
t _f	Fall Time		Q1	–	1.3	10	ns
			Q2	–	8.5	17	
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V Q1 V _{DD} = 15 V, I _D = 6 A Q2 V _{DD} = 15 V, I _D = 8.5 A	Q1	–	7.3	10	nC
			Q2	–	15.7	22	
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 4.5 V Q1 V _{DD} = 15 V, I _D = 6 A Q2 V _{DD} = 15 V, I _D = 8.5 A	Q1	–	3.1	4.3	nC
			Q2	–	7.2	10	
Q _{gs}	Gate to Source Charge	Q1 V _{DD} = 15 V, I _D = 6 A	Q1	–	1.8	–	nC
			Q2	–	3	–	
Q _{gd}	Gate to Drain "Miller" Charge	Q2 V _{DD} = 15 V, I _D = 8.5 A	Q1	–	1	–	nC
			Q2	–	1.9	–	

DRAIN-SOURCE CHARACTERISTICS

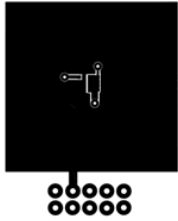
V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 6 A (Note 2) V _{GS} = 0 V, I _S = 8.5 A (Note 2) V _{GS} = 0 V, I _S = 1.3 A (Note 2)	Q1	–	0.8	1.2	V
			Q2	–	0.8	1.2	
			Q2	–	0.6	0.8	
t _{rr}	Reverse Recovery Time	Q1 I _F = 6 A, di/dt = 100 A/μs	Q1	–	13	24	ns
			Q2	–	20	32	
Q _{rr}	Reverse Recovery Charge	Q2 I _F = 8.5 A, di/dt = 300 A/μs	Q1	–	2.3	10	nC
			Q2	–	15	24	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDMC7200S

NOTES:

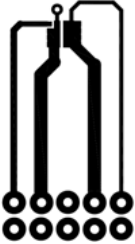
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



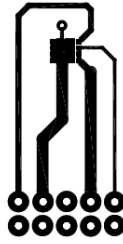
a. 65°C/W when mounted on a 1 in² pad of 2 oz copper



b. 50°C/W when mounted on a 1 in² pad of 2 oz copper



c. 180°C/W when mounted on a minimum pad of 2 oz copper



d. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
3. Starting Q1: T = 25°C, L = 1 mH, I = 5 A, Vgs = 10 V, Vdd = 27V, 100% test at L = 3 mH, I = 4 A; Q2: T = 25C, L = 1 mH, I = 8 A, Vgs = 10 V, Vdd = 27 V, 100% test at L = 3 mH, I = 3.2 A.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted)

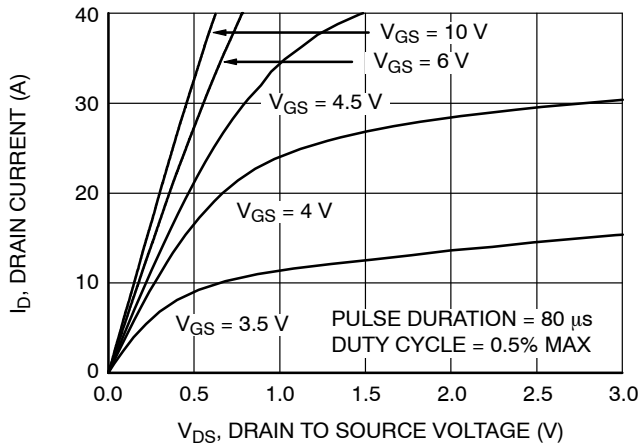


Figure 1. On Region Characteristics

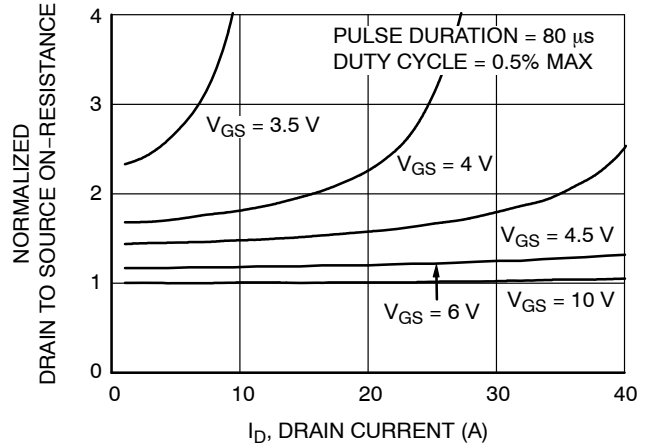


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

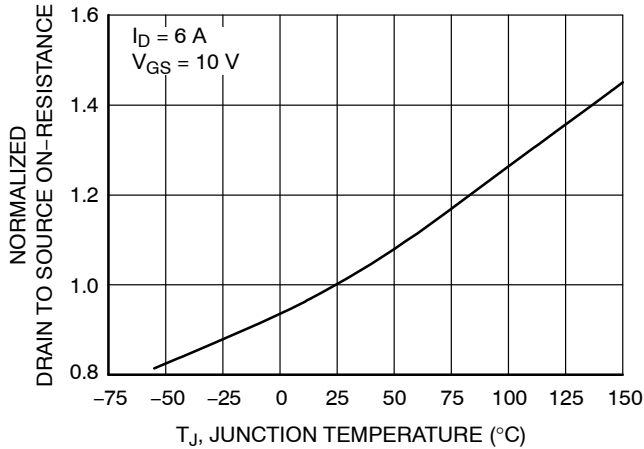


Figure 3. Normalized On Resistance vs. Junction Temperature

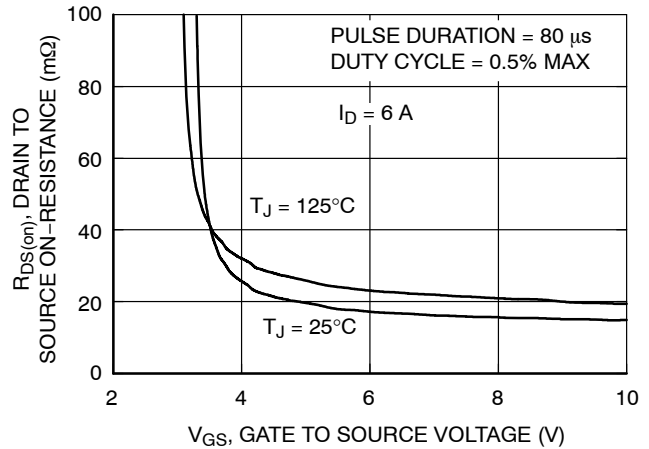


Figure 4. On-Resistance vs. Gate to Source Voltage

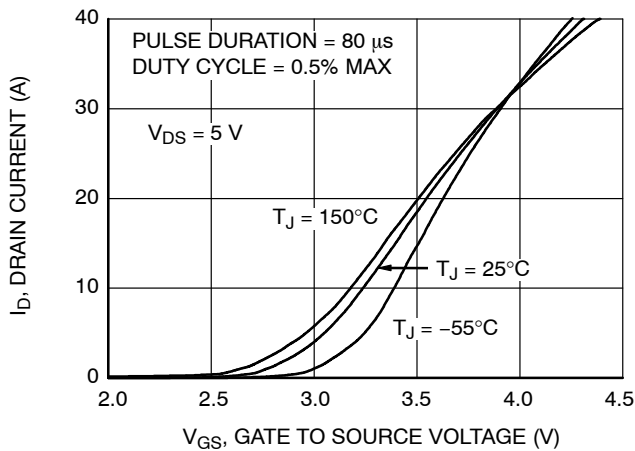


Figure 5. Transfer Characteristics

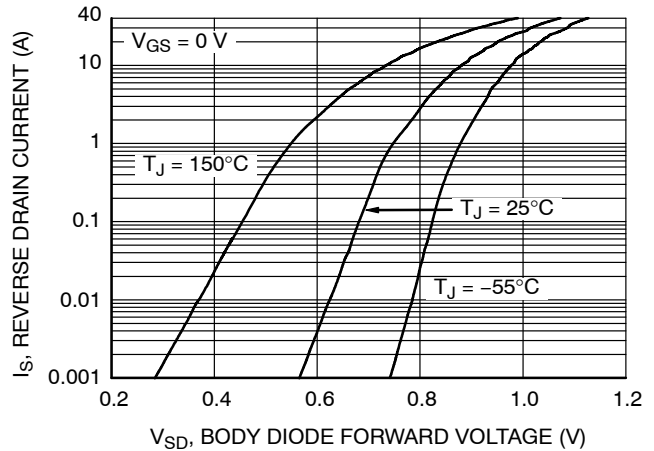


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

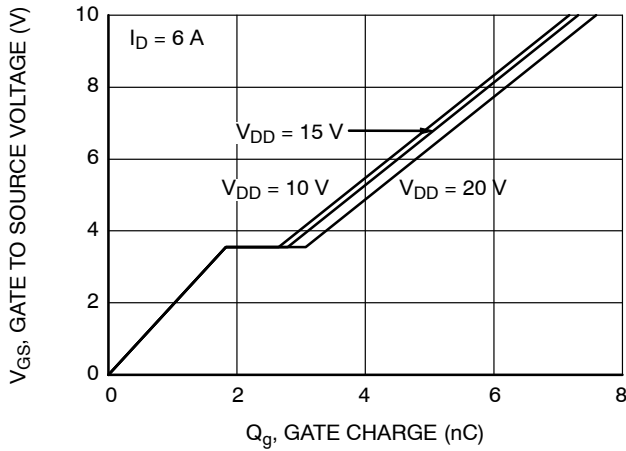


Figure 7. Gate Charge Characteristics

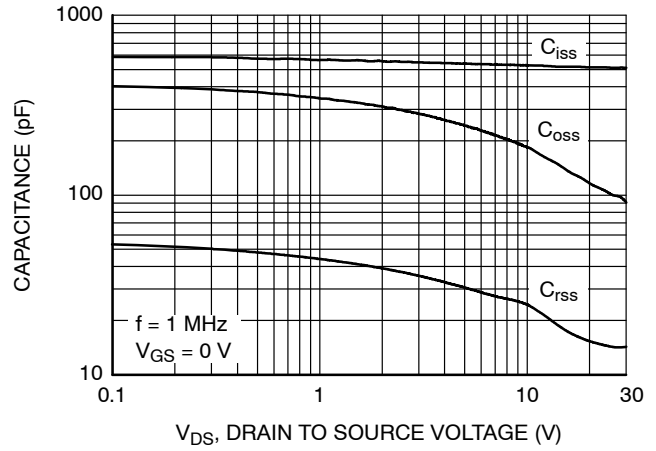


Figure 8. Capacitance vs. Drain to Source Voltage

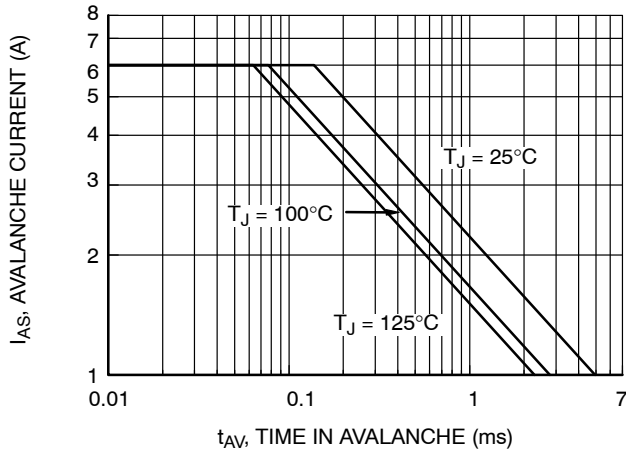


Figure 9. Unclamped Inductive Switching Capability

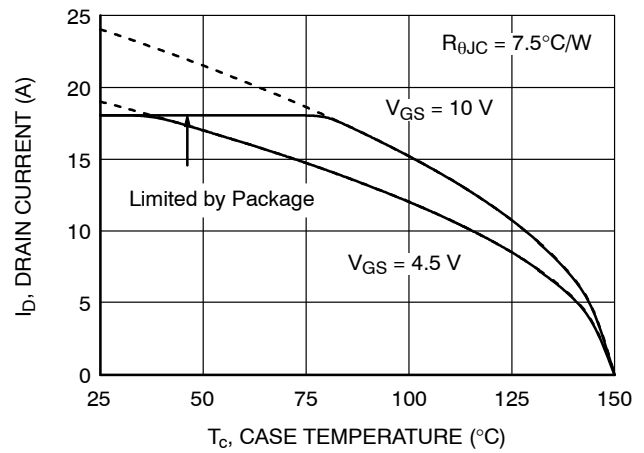


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

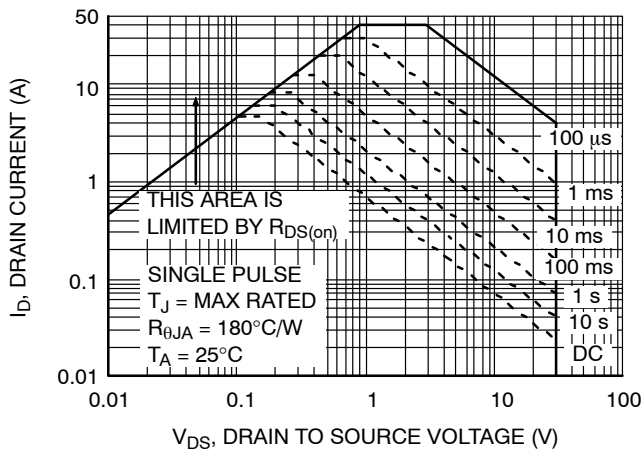


Figure 11. Forward Bias Safe Operating Area

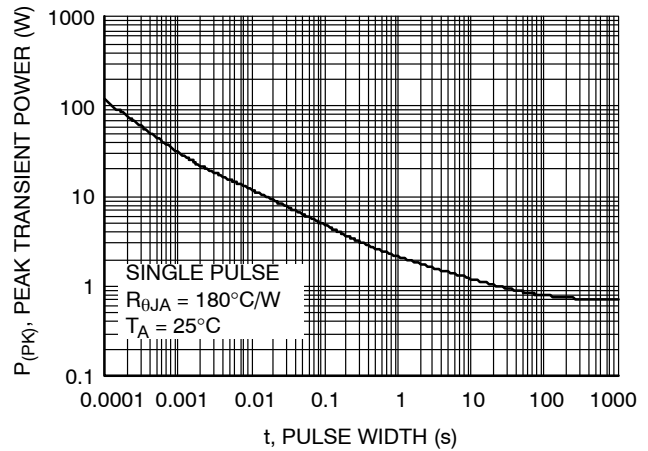


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

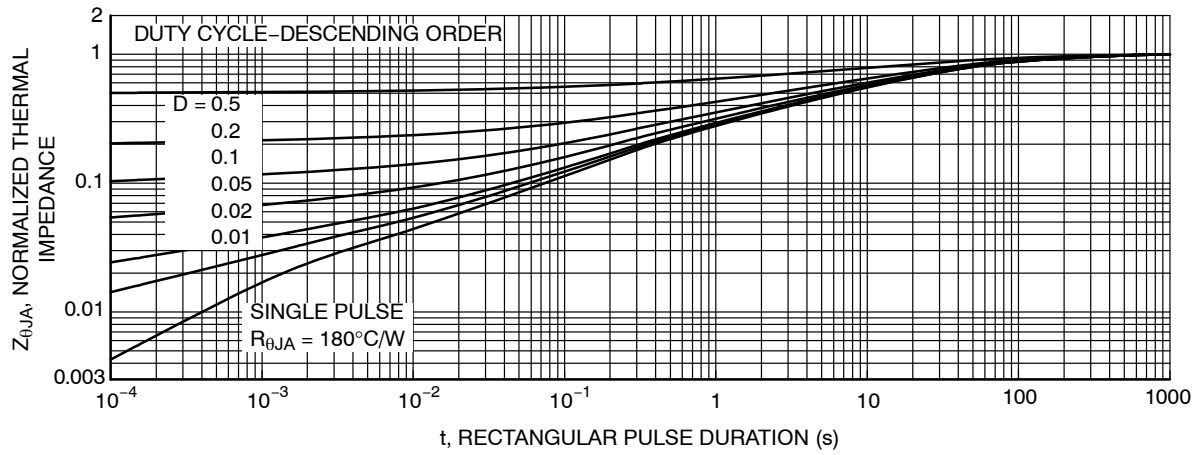


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted)

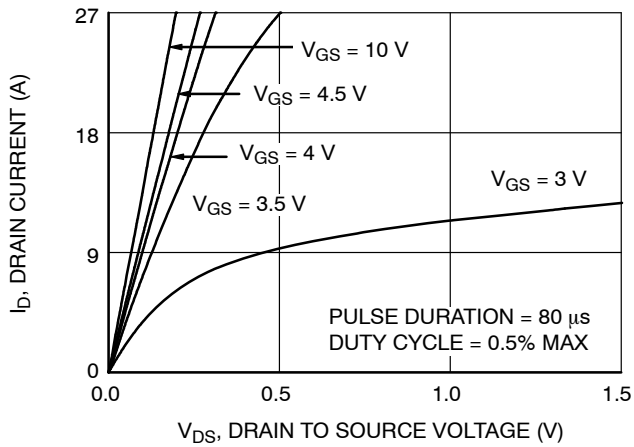


Figure 14. On-Region Characteristics

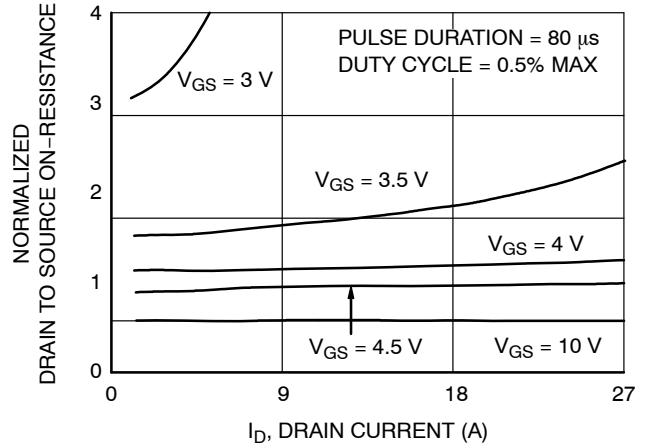


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

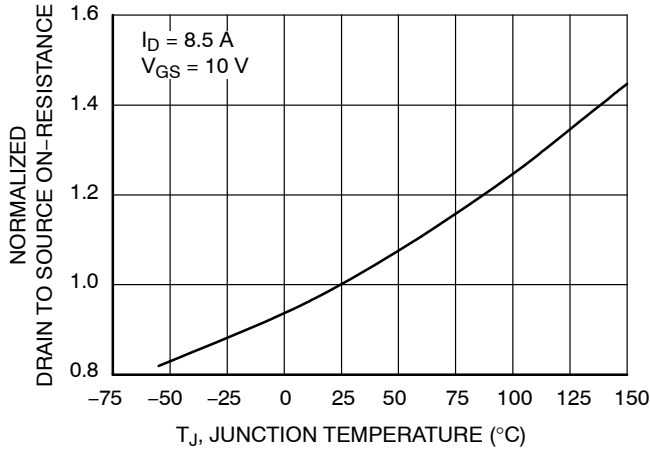


Figure 16. Normalized On Resistance vs. Junction Temperature

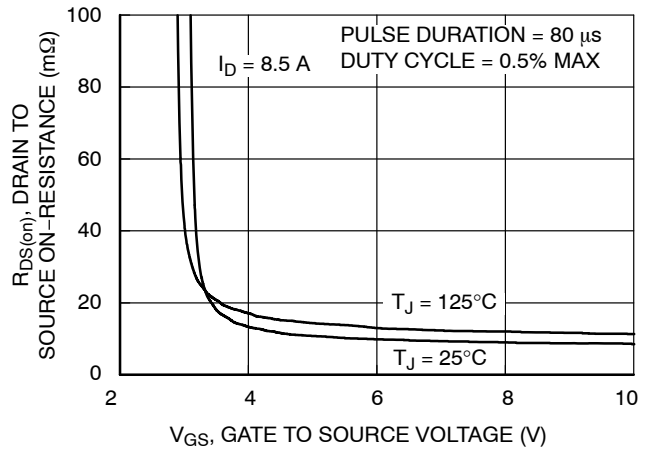


Figure 17. On-Resistance vs. Gate to Source Voltage

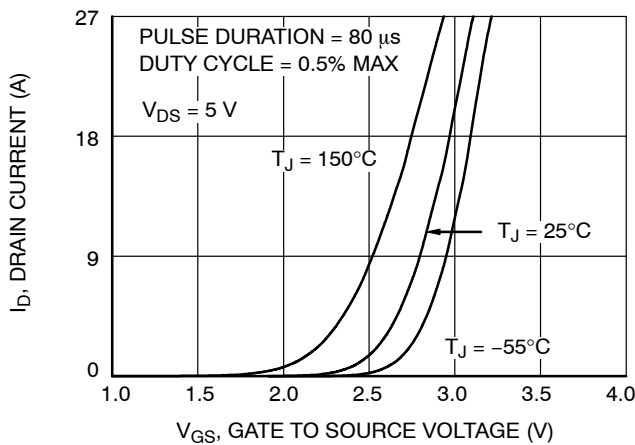


Figure 18. Transfer Characteristics

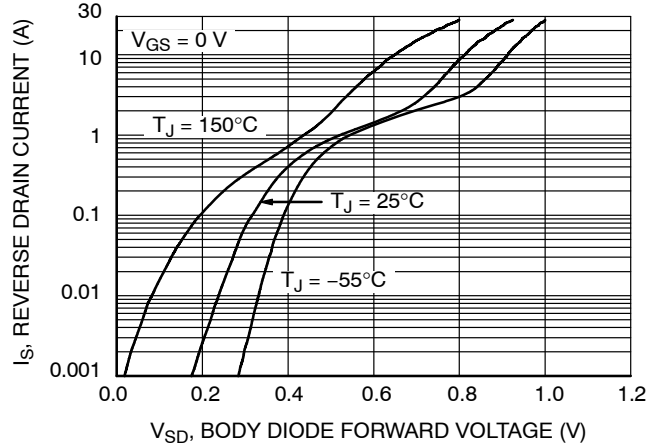


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

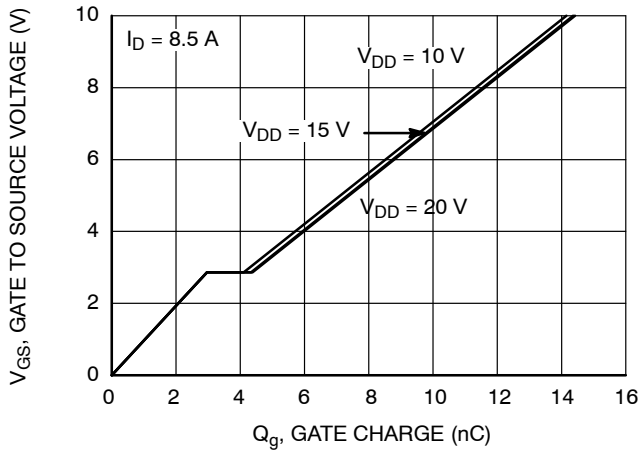


Figure 20. Gate Charge Characteristics

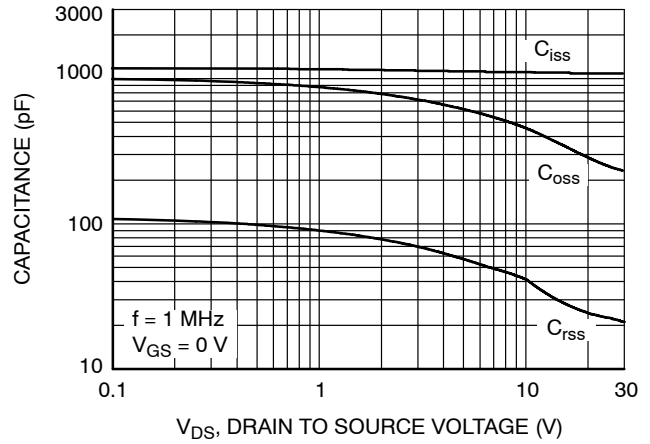


Figure 21. Capacitance vs. Drain to Source Voltage

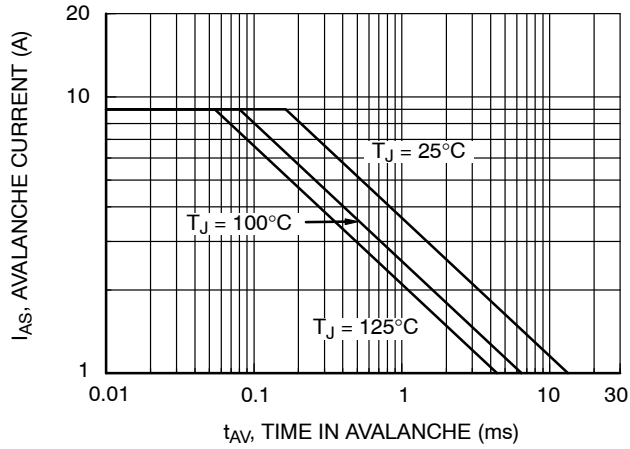


Figure 22. Unclamped Inductive Switching Capability

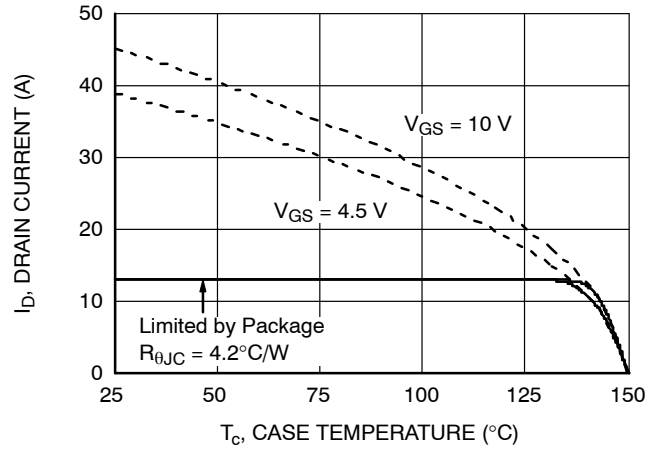


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

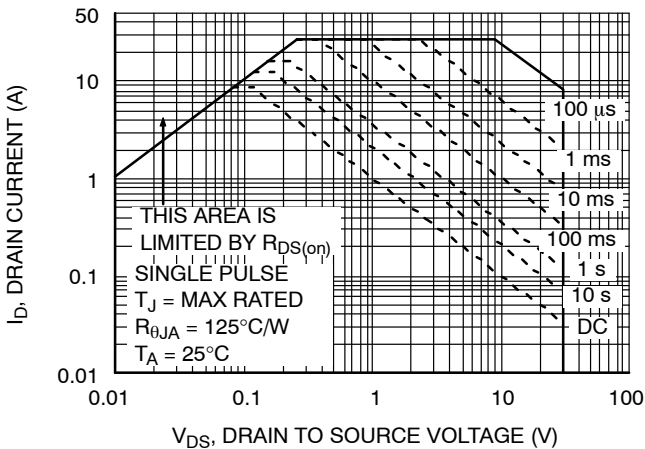


Figure 24. Forward Bias Safe Operating Area

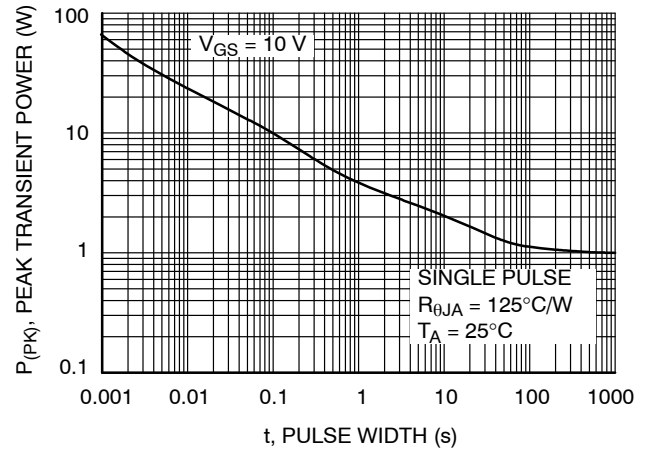


Figure 25. Single Pulse Maximum Power Dissipation

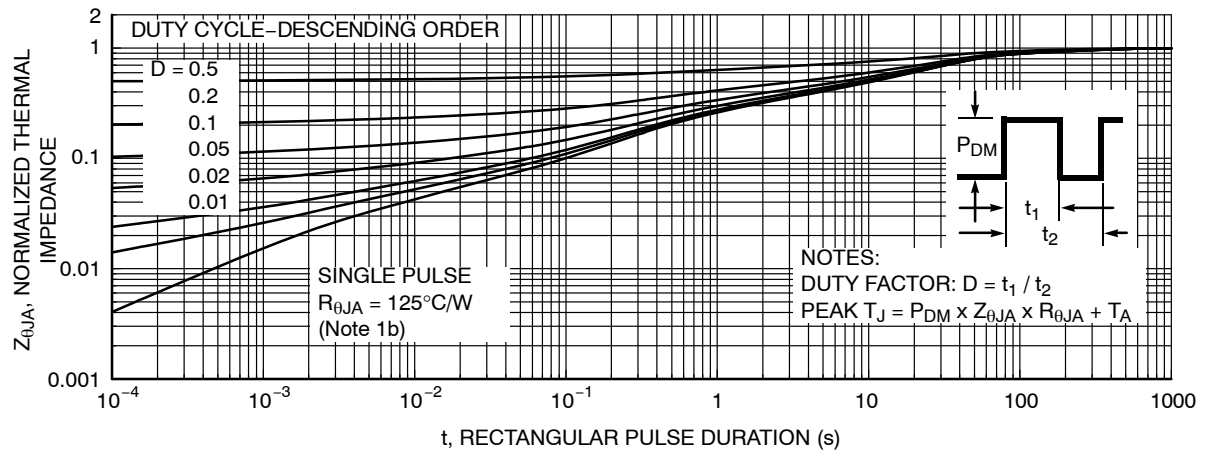
TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

Figure 26. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET™ Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMC7200S.

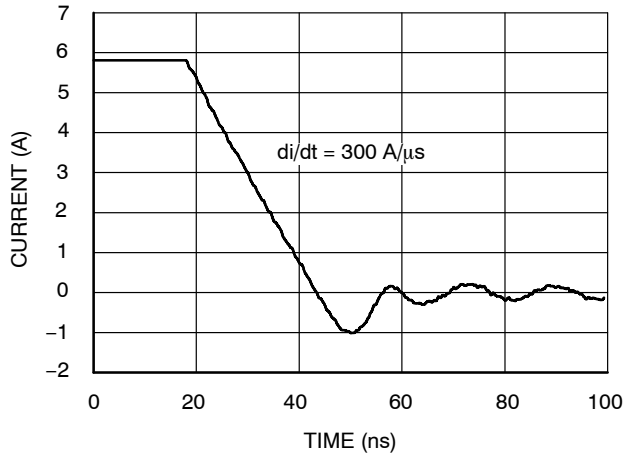


Figure 27. FDMC7200S SyncFET Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

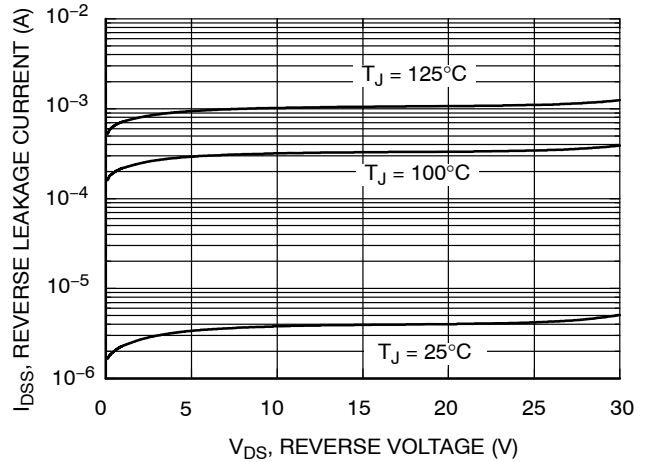


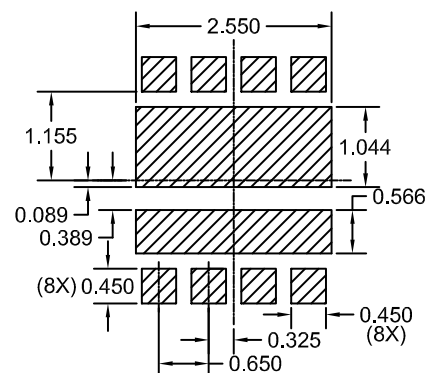
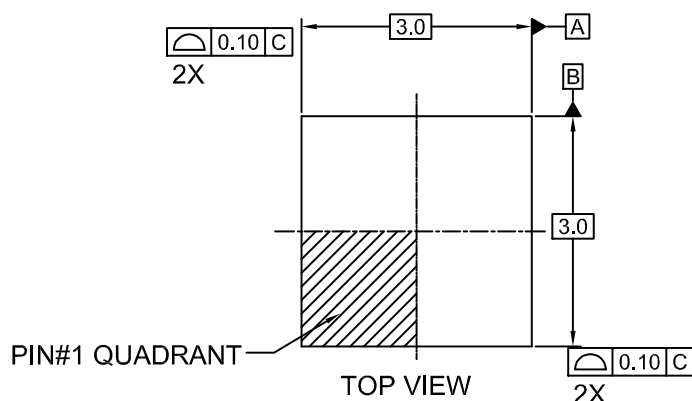
Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

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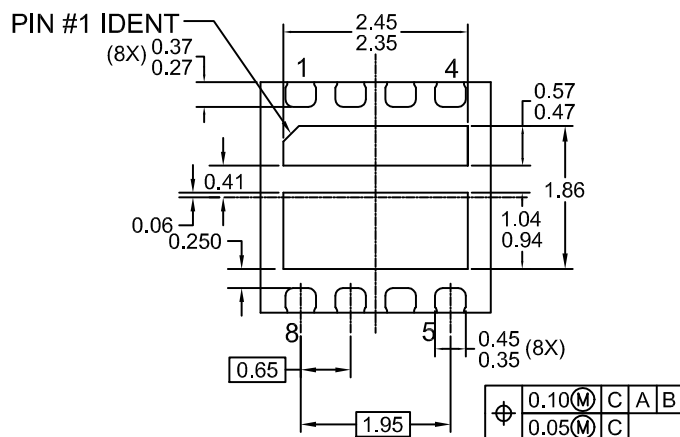
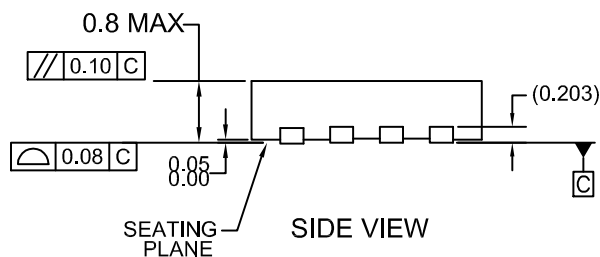
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WDFN8 3x3, 0.65P
CASE 511DE
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

- A. DOES NOT CONFORM TO JEDEC
REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

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