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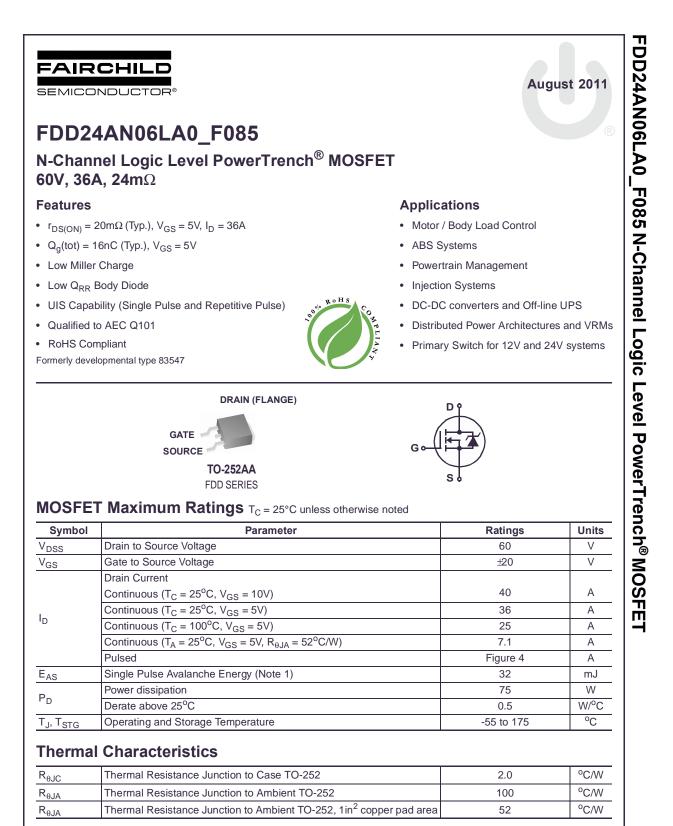


ON Semiconductor®

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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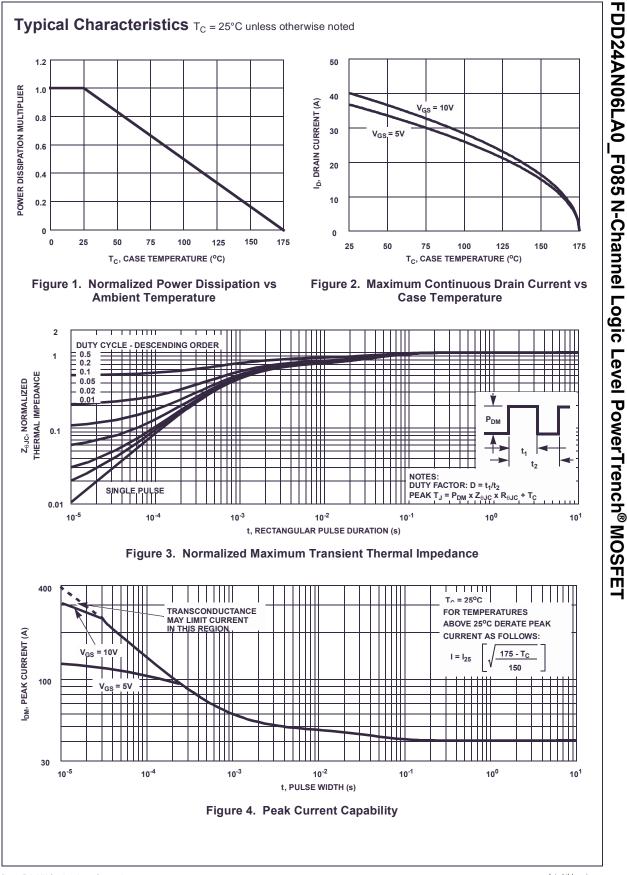


This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

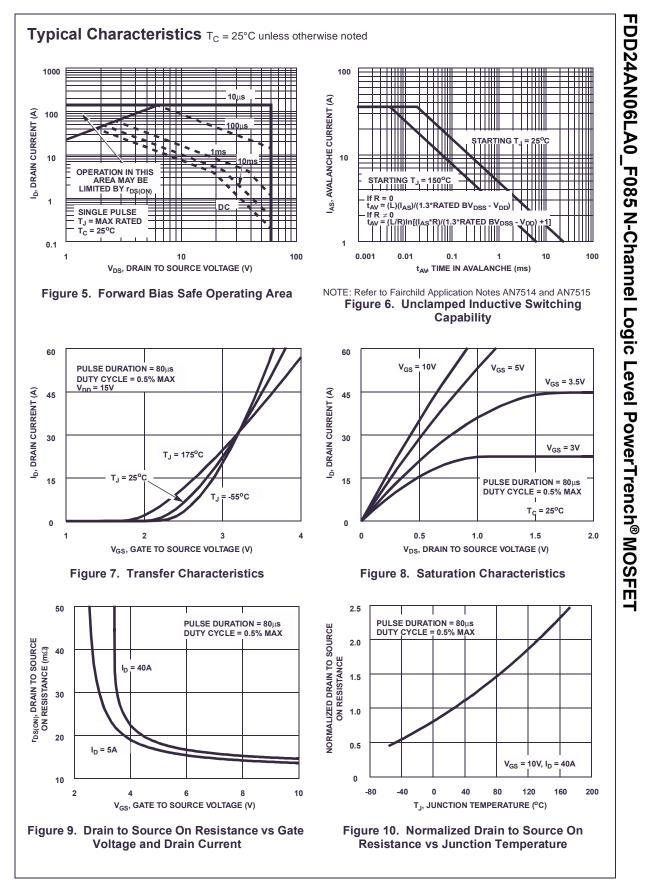
Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

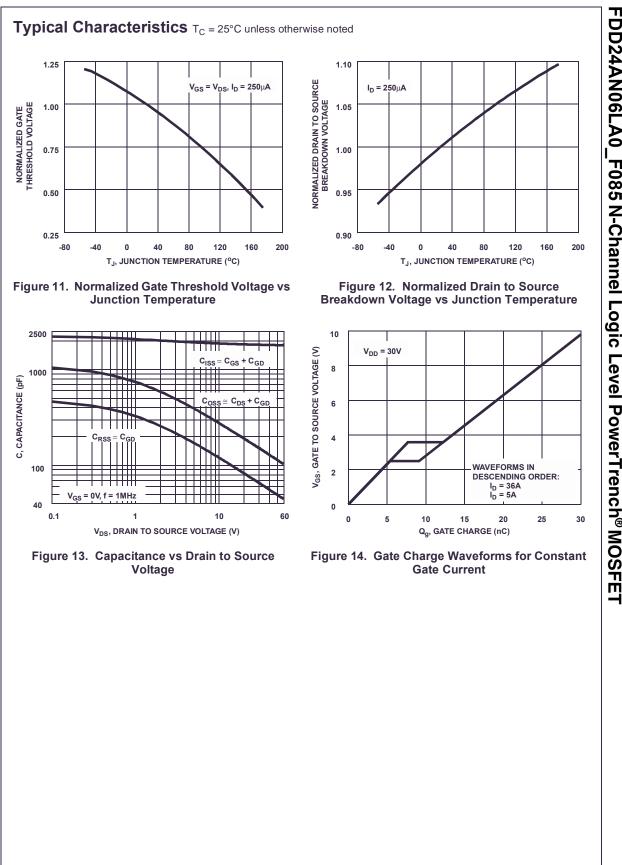
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I _{GSS} Ga On Characte V _{GS(TH)} V _{GS(TH)} Ga r _{DS(ON)} Dr	ate to Source Leakage Current ristics ate to Source Threshold Voltage	V _{GS} = ±20V	$T_{\rm C} = 150^{\rm o}{\rm C}$	-	1 1	1	
On Characte V _{GS(TH)} Ga r _{DS(ON)} Dr	aristics ate to Source Threshold Voltage			-	-	250	μΑ
V _{GS(TH)} Ga r _{DS(ON)} Dr	ate to Source Threshold Voltage	> \/\/		-	-	±100	nA
V _{GS(TH)} Ga r _{DS(ON)} Dr	ate to Source Threshold Voltage	> \/\/					
r _{DS(ON)} Dr			I_ = 250µA	1	-	2	V
D3(0N)		00 00	$\label{eq:GS} \begin{split} V_{GS} &= V_{DS}, \ I_D = 250 \mu A \\ \hline I_D &= 40A, \ V_{GS} = 10V \\ \hline I_D &= 36A, \ V_{GS} = 5V \\ \hline I_D &= 36A, \ V_{GS} = 5V, \\ \hline I_J &= 175^\circ C \end{split}$		0.016	0.019	v
D3(0N)					0.010	0.013	
Oh	Drain to Source On Resistance						Ω
D					0.047	0.056	
UVnamic i n	aracteristics						
	out Capacitance				1850		pF
.00	utput Capacitance	V _{DS} = 25V,	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz		180	_	pF
000	everse Transfer Capacitance	f = 1MHz			75	_	pF
1.00	tal Gate Charge at 5V	V _{GS} = 0V to	51/		16	21	nC
3(:=:)	reshold Gate Charge	$V_{GS} = 0V$ to		-	1.8	2.4	nC
	ate to Source Gate Charge	163 - 01 10	$I_{\rm D} = 36A$	-	6.3	-	nC
go	ate Charge Threshold to Platea	u	$I_a = 1.0 \text{mA}$	-	4.5	_	nC
goz	ate to Drain "Miller" Charge		9	-	5.0	-	nC
3-		I					
·	haracteristics $(V_{GS} = 5V)$ rn-On Time	—		-	-	195	20
	rn-On Delay Time			-	12	-	ns ns
u(011)	se Time		$V_{DD} = 30V, I_D = 36A$ $V_{GS} = 5V, R_{GS} = 9.1\Omega$		118	-	ns
· -	rn-Off Delay Time				26	-	ns
a(o)	II Time				41	-	ns
· –	rn-Off Time				-	101	ns
011				-		101	110
Drain-Source	e Diode Characteristics			-		4.05	
V _{SD} Sc	Source to Drain Diode Voltage		$I_{SD} = 36A$		-	1.25	V
		I _{SD} = 18A	$dt = 100 \Lambda/mc$	-	-	1.0 34	
	everse Recovery Time everse Recovered Charge		$I_{SD} = 36A, dI_{SD}/dt = 100A/\mu s$ $I_{SD} = 36A, dI_{SD}/dt = 100A/\mu s$		-	34 30	ns nC
Q _{RR} Re	everse Recovered Charge	ISD = 30A, 0	$H_{SD}/dt = 100 A/\mu S$	-		30	lic
Notes: 1: Starting T _J = 25°C,	$L = 80\mu H$, $I_{AS} = 28A$.						



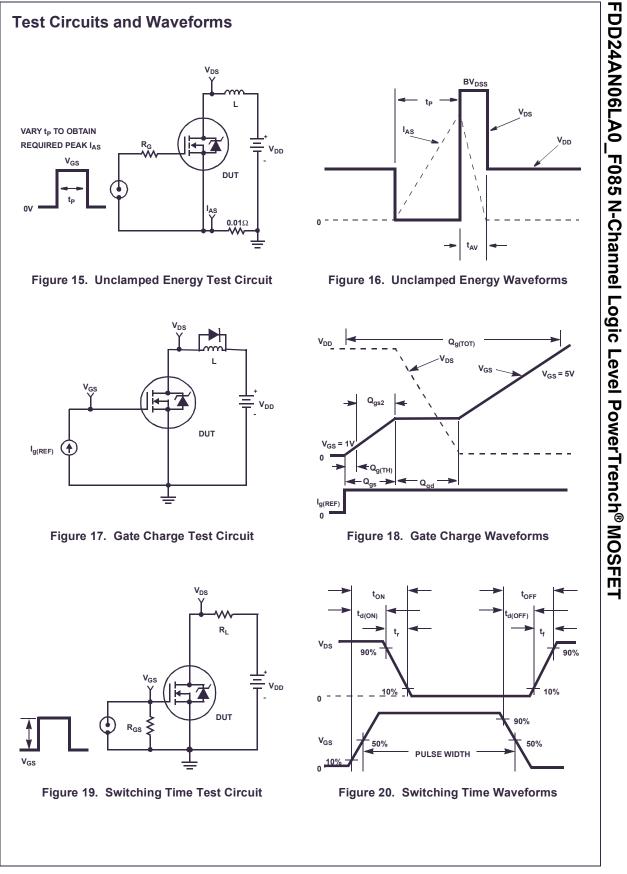
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FDD24AN06LA0_F085 N-Channel Logic Level PowerTrench[®] MOSFET



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Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}}$$
(EQ. 1)

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- 2. The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- 6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta,JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

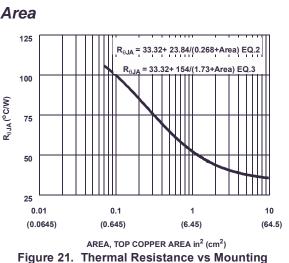
Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

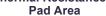
$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\Theta JA} = 33.32 + \frac{154}{(1.73 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared





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