FAN5602

Universal (Step-Up/Step-Down) Charge Pump Regulated DC/DC Converter

ON Semiconductor®

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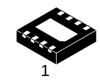
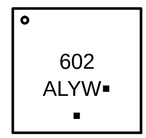


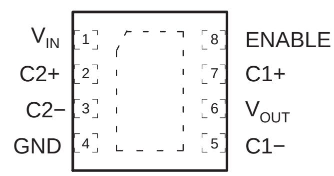
WDFN8 3x3, 0.65P
CASE 511CD

MARKING DIAGRAM



602 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENTS



3x3mm 8−Lead MLP

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

The FAN5602 is a universal switched capacitor DC/DC converter capable of step−up or step−down operation. Due to its unique adaptive fractional switching topology, the device achieves high efficiency over a wider input/ output voltage range than any of its predecessors. The FAN5602 utilizes resistance−modulated loop control, which produces lower switching noise than other topologies. Depending upon actual load conditions, the device automatically switches between constant−frequency and pulse−skipping modes of operation to extend battery life.

The FAN5602 produces a fixed regulated output within the range of 2.7 V to 5.5 V from any type of voltage source. High efficiency is achieved under various input/ output voltage conditions because an internal logic circuit automatically reconfigures the system to the best possi− ble topology. Only two 1 μF bucket capacitors and one 10 μF output capacitor are needed. During power on, soft−start circuitry prevents excessive current drawn from the supply. The device is protected against short−circuit and over−temperature conditions.

The FAN5602 is available with 4.5 V and 5.0 V output voltages in a 3x3 mm WDFN8 package.

Features

- Low−Noise, Constant−Frequency Operation at Heavy Load
- High−Efficiency, Pulse−Skip (PFM) Operation at Light Load
- Switch Configurations (1:3, 1:2, 2:3, 1:1, 3:2, 2:1, 3:1)
- 92% Peak Efficiency
- Input Voltage Range: 2.7 V to 5.5 V
- Output Current: 4.5 V, 100 mA at $V_{IN} = 3.6$ V
- ±3% Output Voltage Accuracy
- $I_{CC} < 1$ μA in Shutdown Mode
- 1 MHz Operating Frequency
- Shutdown Isolates Output from Input
- Soft−Start Limits Inrush Current at Startup
- Short−Circuit and Over−Temperature Protection
- Minimum External Component Count
- No Inductors
- This is a Pb−Free Device

Applications

- Cell Phones
- Handheld Computers
- Portable RF Communication Equipment
- Core Supply to Low−Power Processors
- Low−Voltage DC Bus
- DSP Supplies

ORDERING INFORMATION

Part Number	Output Voltage, N_{VOM}	Package	Packing Method†
FAN5602MP45X	4.5 V	WDFN8 3x3, 0.65P (Pb−Free)	3000 / Tape & Reel
FAN5602MP5X	5.0 V	WDFN8 3x3, 0.65P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

Application Diagram

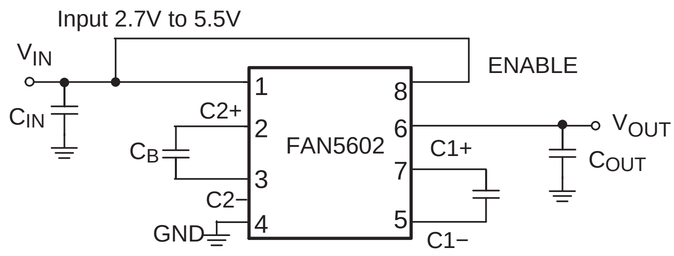


Figure 1. Typical Application Diagram

Block Diagram

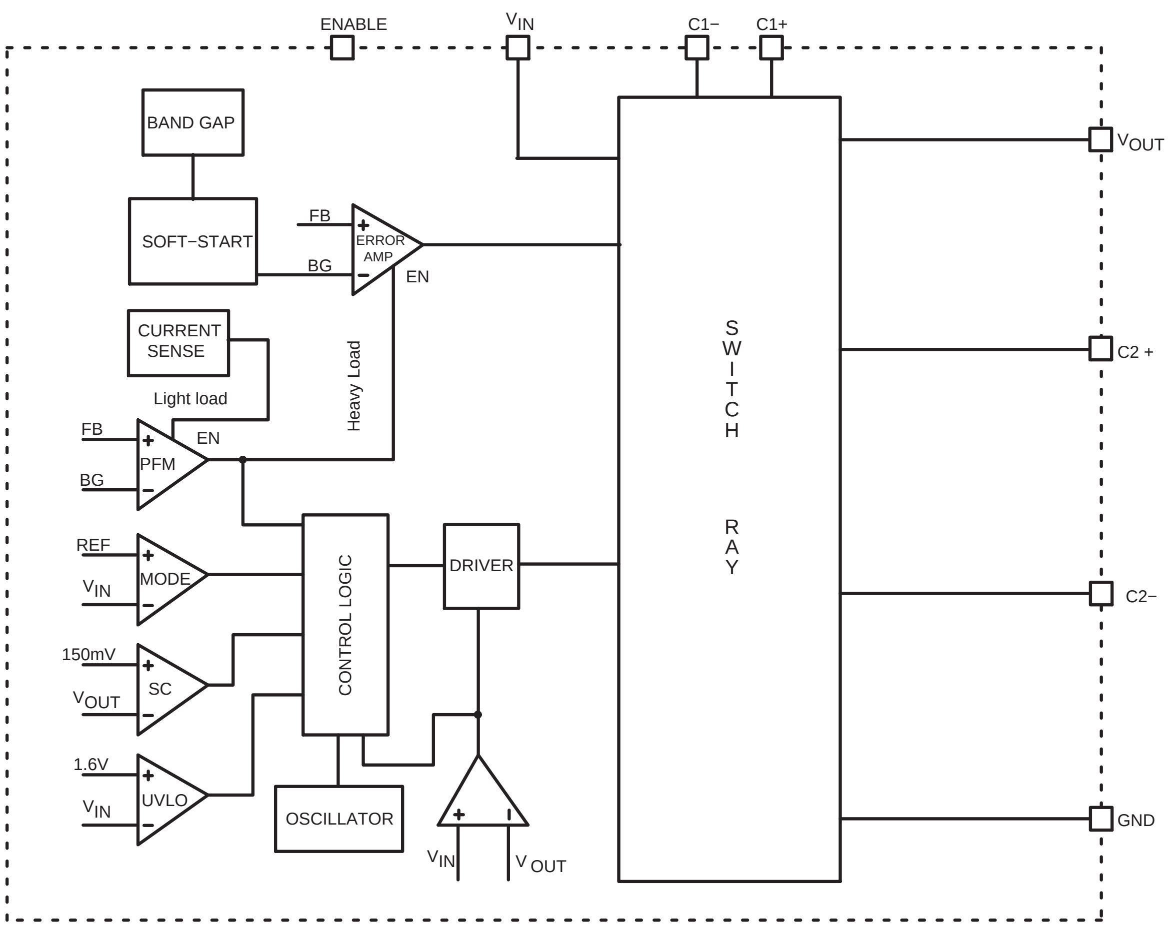
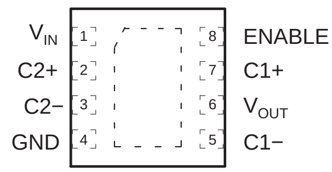


Figure 2. Block Diagram

Pin Assignments



3x3mm 8−Lead MLP

Figure 3. Pin Assignments

Table 1. PIN DESCRIPTIONS

Pin #	Name	Description
1	VIN	Supply Voltage Input.
2	C2+	Bucket Capacitor2. Positive Connection.
3	C2−	Bucket Capacitor2. Negative Connection.
4	GND	Ground
5	C1−	Bucket Capacitor1. Negative Connection.
6	VOUT	Regulated Output Voltage. Bypass this pin with 10 μF ceramic low−ESR capacitor.
7	C1+	Bucket Capacitor1. Positive Connection.
8	ENABLE	Enable Input. Logic high enables the chip and logic low disables the chip, reducing the supply current to less than 1 μA. Do not float this pin.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VIN	V_{IN}, V_{OUT}, ENABLE, Voltage to GND	−3.0	6.0	V
	Voltage at C1+,C1−,C2+, and C2−to GND	−3.0	V_{IN} + 0.3	V
P_D	Power Dissipation		Internally Limited	
T_L	Lead Soldering Temperature (10 seconds)		300	°C
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	−55	150	°C
ESD	Human Body Model (HBM)		2	kV
	Charged Device Model (CDM)		2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Using Mil Std. 883E, method 3015.7 (Human Body Model) and EIAJ/JESD22C101−A (Charged Device Model).

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN	Input Voltage		1.8		5.5	V
I_L	Load Current	V_{IN} < 2 V			30	mA
		4.5 & 5.5,V_{IN} = 3.6 V			100	
T_A	Ambient Temperature		−40		+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Refer to Figure 9 in Typical Performance Characteristics

Table 4. DC ELECTRICAL CHARACTERISTICS

V_{IN} = 2.7 V to 5.5 V, $C_1 = C_2$ = 1 μF, $C_{IN} = C_{OUT}$ = 10 μF, ENABLE = V_{IN}, T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{UVLO}	Input Under−Voltage Lockout			1.5	1.7	2.2	v
V_{OUT}	Output Voltage	$V_{IN} \geq 0.75 \times V_{NOM}$, 0 mA < I_{LOAD} < 100 mA		0.97 x V_{NOM}	VNOM	1.03 x V_{NOM}	V
I_Q	Quiescent Current	$V_{IN} \geq 1.1 \times V_{NOM}$, I_{LOAD} = 0 mA			170	300	μA
	Off Mode Supply Current	ENABLE = GND			0.1	1.0	μA
	Output Short−Circuit	V_{OUT} < 150 mV				200	mA
	Efficiency	$V_{IN} = 0.85 \times V_{NOM}$, I_{LOAD} = 30 mA	4.5, 5.0 V		80		%
		$V_{IN} = 1.1 \times V_{NOM}$, I_{LOAD} = 30 mA	4.5, 5.0 V		92		
f_{OSC}	Oscillator Frequency	T_A = 25°C		0.7	1.0	1.3	MHz
T_{SD}	Thermal Shutdown Threshold				145		°C
T_{SDHYS}	Thermal Shutdown Threshold Hysteresis				15		°C
V_{IH}	ENABLE Logic Input High Voltage			1.5			V
V_{IL}	ENABLE Logic Input Low Voltage					0.5	V
I_{EN}	ENABLE Logic Input Bias Current	ENABLE =V_{IN} or GND		−1		1	μA
t_{ON}	V_{OUT} Turn−On Time	$V_{IN} = 0.9 \times V_{NOM}$, I_{LOAD} = 0 mA,10% to 90%			0.5		ms
	V_{OUT} Ripple	V_{IN} = 2.5 V, I_{LOAD} = 200 mA			10		mVpp

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{OUT} = 4.5$ V unless otherwise noted.

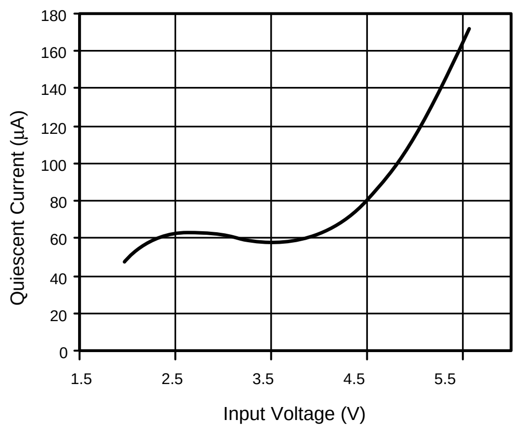


Figure 4. Quiescent Current vs. Input Voltage

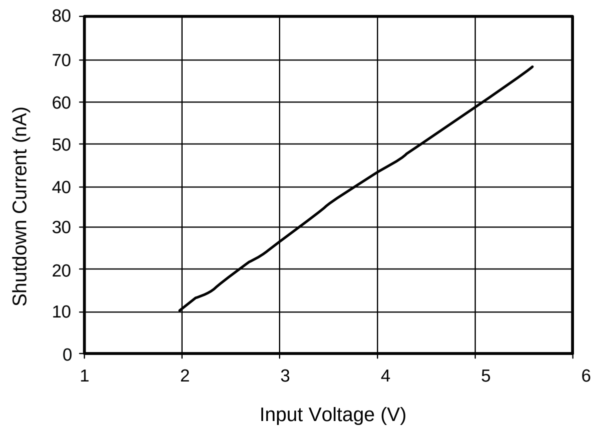


Figure 5. Shutdown Current vs. Input Voltage

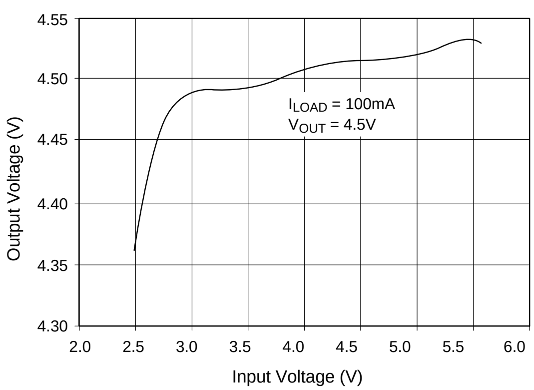


Figure 6. Line Regulation

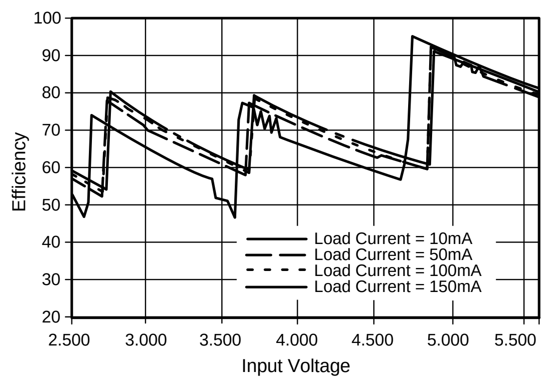


Figure 7. Efficiency vs. Input Voltage

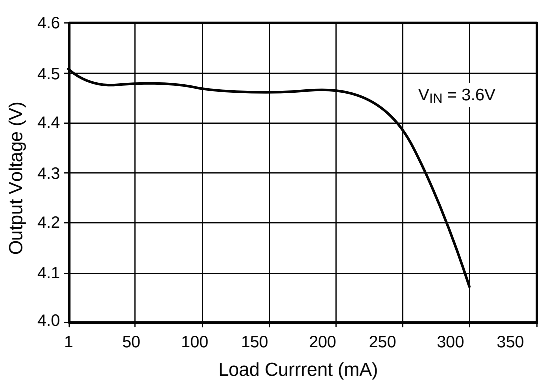


Figure 8. Load Regulation

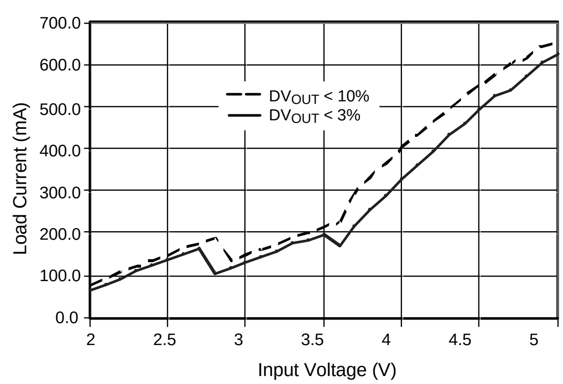


Figure 9. Output Current Capacity vs. Input voltage

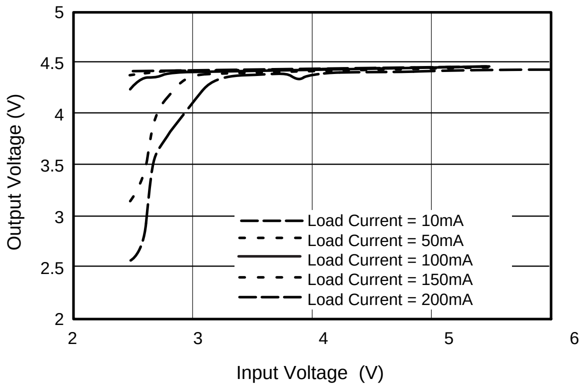


Figure 10. Output Voltage vs. Input Voltage

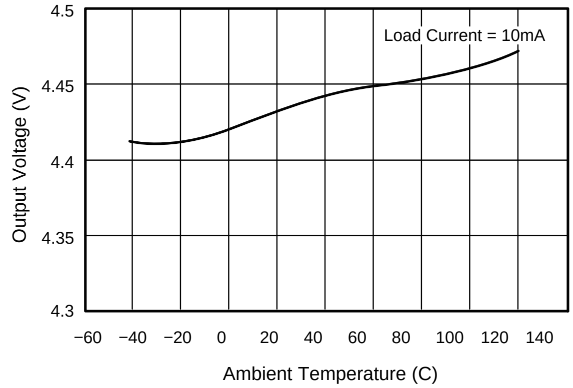


Figure 11. Output Voltage vs. Ambient Temperature

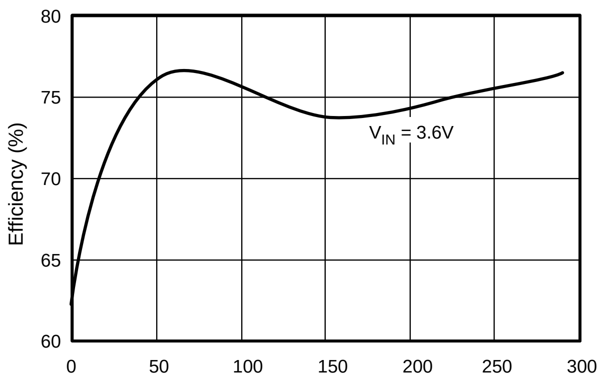


Figure 12. Peak Efficiency vs. Load Current

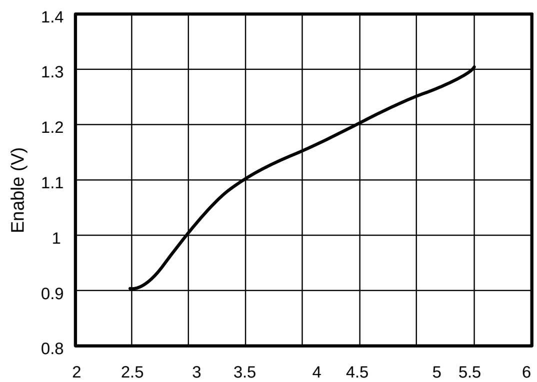


Figure 13. Enable Threshold vs. Input Voltage

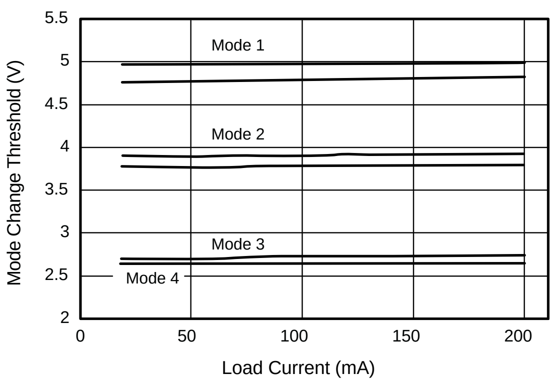


Figure 14. Mode Change Threshold and Hysteresis

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

$T_A = 25°C$, $C_{IN} = C_{OUT} = 10\ \mu F$, $C_B = 1\ \mu F$, $V_{OUT} = 4.5\ V$ unless otherwise noted.

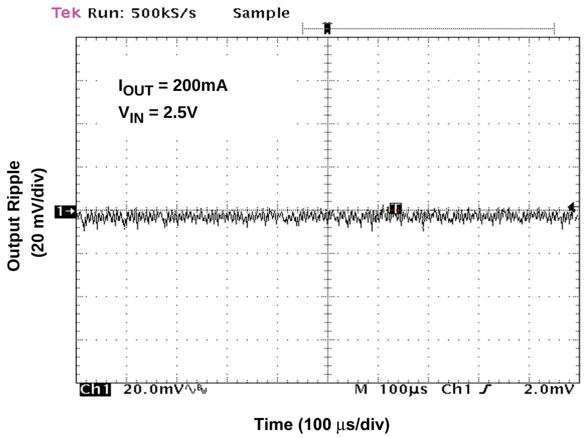


Figure 15. Output Ripple

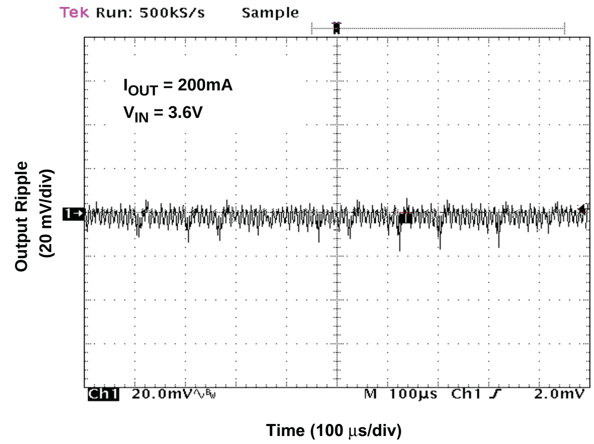


Figure 16. Output Ripple

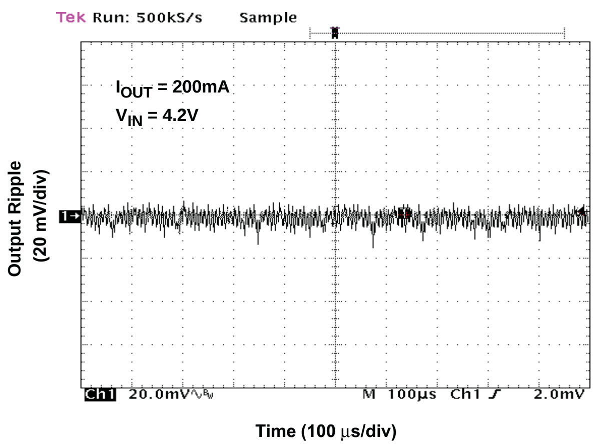


Figure 17. Output Ripple

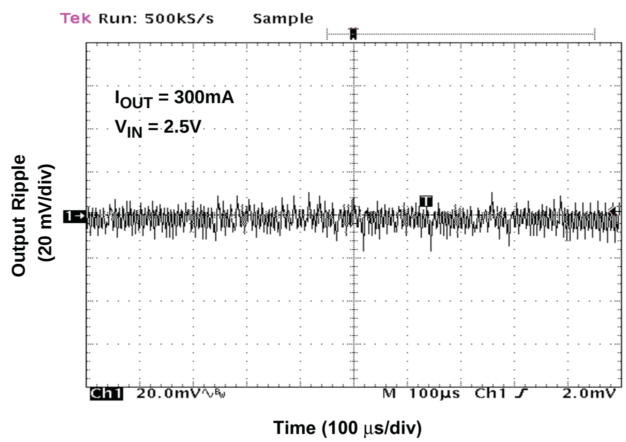


Figure 18. Output Ripple

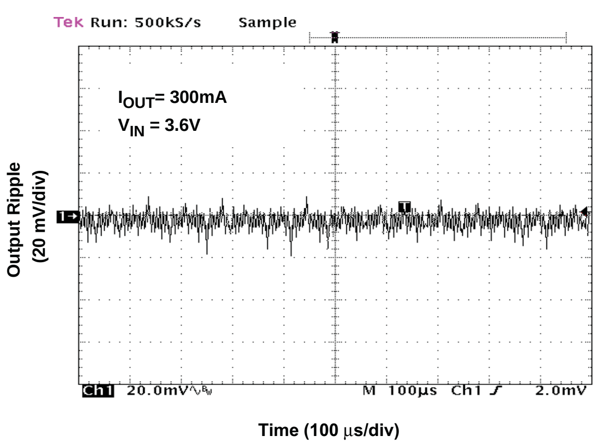


Figure 19. Output Ripple

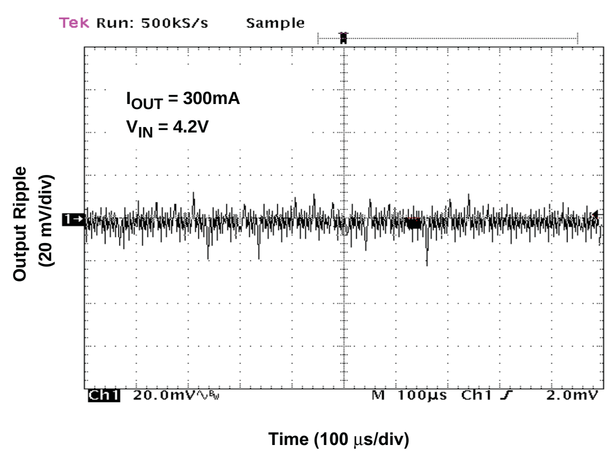


Figure 20. Output Ripple

FUNCTIONAL DESCRIPTION

FAN5602 is a high−efficiency, low−noise switched capacitor DC/DC converter capable of step−up and step−down operations. It has seven built−in switch configurations. Based on the ratio of the input voltage to the output volt− age, the FAN5602 automatically reconfigures the switch to achieve the highest efficiency. The regulation of the output is achieved by a linear regulation loop, which modulates the on−resistance of the power transistors so that the amount of charge transferred from the input to the flying capacitor at each clock cycle is controlled and is equal to the charge needed by the load. The current spike is reduced to minimum. At light load, the FAN5602 automatically switches to Pulse Frequency Modulation (PFM) mode to save power. The regulation at PFM mode is achieved by skipping pulses.

Linear Regulation Loop

The FAN5602 operates at constant frequency at load higher than 10 mA. The linear regulation loop consisting of power transistors, feedback (resistor divider), and error amplifier is used to realize the regulation of the out− put voltage and to reduce the current spike. The error amplifier takes feedback and reference as inputs and generates the error voltage signal. The error voltage signal is then used as the gate voltage of the power transistor and modulates the on−resistance of the power transistor and, therefore, the charge transferred from the input to the output is controlled and the regulation of the output is realized. Since the charge transfer is controlled, the FAN5602 has a small ESR spike.

Switch Array

Switch Configurations

The FAN5602 has seven built−in switch configurations, including 1:1, 3:2, 2:1 and 3:1 for step−down and 2:3, 1:2 and 1:3 for step−up.

When 1.5 x V_{OUT} > V_{IN} > V_{OUT}, the 1:1 mode shown in Figure 21 is used. In this mode, the internal oscillator is

turned off. The power transistors connecting the input and the output become pass transistors and their gate voltages are controlled by the linear regulation loop, the rest of power transistors are turned off. In this mode, the FAN5602 operates exactly like a low dropout (LDO) regulator and the ripple of the output is in the micro−volt range.

When 1.5 x V_{IN} > V_{OUT} > V_{IN}, the 2:3 mode (step−up) shown in Figure 22 is used. In the charging phase, two flying capacitors are placed in series and each capacitor is charged to a half of the input voltage. In pumping phase, the flying capacitors are placed in parallel. The input is connected to the bottom the capacitors so that the top of the capacitors is boosted to a voltage that equals V_{IN}/2 + V_{IN}, i.e., 3/2 x V_{IN}. By connecting the top of the capacitors to the output, one can ideally charge the output to 3/2 x V_{IN}. If 3/2 x V_{IN} is higher than the needed V_{OUT}, the linear regulation loop adjusts the on− resistance to drop some voltage. Boosting the voltage of the top of the capacitors to 3/2 x V_{IN} by connecting V_{IN} the bottom of the capacitors, boosts the power efficiency 3/2 times. In 2:3 mode, the ideal power efficiency is V_{OUT}/1.5 x V_{IN}. For example, if V_{IN} = 2 V, V_{OUT} = 2 x V_{IN} = 4 V, the ideal power efficiency is 100%.

When 2 x V_{IN} > V_{OUT} > 1.5 x V_{IN}, the 1:2 mode (step−up) shown in Figure 23 is used. Both in the charging phase and in pumping phase, two flying capacitors are placed in parallel. In charging phase, the capacitors are charged to the input voltage. In the pumping phase, the input volt− age is placed to the bottom of the capacitors. The top of the capacitors is boosted to 2 x V_{IN}. By connecting the top of the capacitors to the output, one can ideally charge the output to 2 x V_{IN}. Boosting the voltage on the top of the capacitors to 2V_{IN} boosts the power efficiency 2 times. In 1:2 mode, the ideal power efficiency is V_{OUT}/2 x V_{IN}. For example, V_{IN} = 2V, V_{OUT} = 2 x V_{IN} = 4V, the ideal power efficiency is 100%.

When 3 x V_{IN} > V_{OUT} > 2 x V_{IN}, the 1:3 mode (step−up) shown in Figure 24 is used. In charging phase, two flying capacitors are placed in parallel and each is charged to V_{IN}. In the pumping phase, the two flying capacitors are placed in series and the input is connected to the bottom of the series connected capacitors. The top of the series connected capacitors is boosted to 3 x V_{IN}. The ideal power efficiency is boosted 3 times and is equal to V_{OUT}/ 3$V_{IN.}$ For example, V_{IN} = 1 V, V_{OUT} = 3 x V_{IN} = 3 V, the ideal power efficiency is 100%. By connecting the output to the top of the series connected capacitors, one can charge the output to 3 x V_{IN}.

The internal logic in the FAN5602 monitors the input and the output compares them, and automatically selects the switch configuration to achieve the highest efficiency.

The step−down modes 3:2, 2:1, and 3:1 can be under− stood by reversing the function of V_{IN} and V_{OUT} in the above discussion.

The built−in modes improve power efficiency and extend the battery life. For example, if V_{OUT} = 5 V, mode 1:2 needs a minimum V_{IN} = 2.5 V. By built−in 1:3 mode, the minimum battery voltage is extended to 1.7 V.

Switch Array Modes

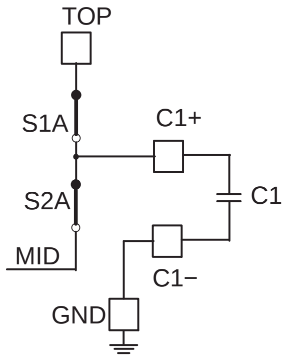


Figure 21. Mode 1 (1:1)

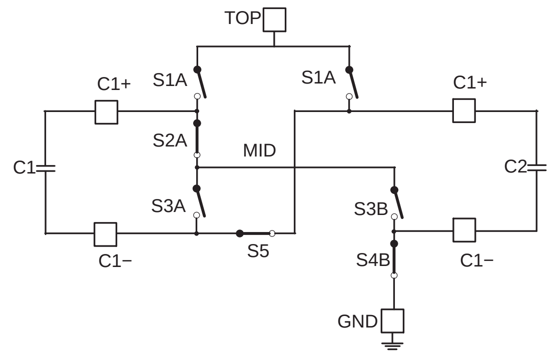


Figure 22. Mode 2 (2:3 or 3:2) All Switches Set for Phase 1 and Reverse State for Phase 2

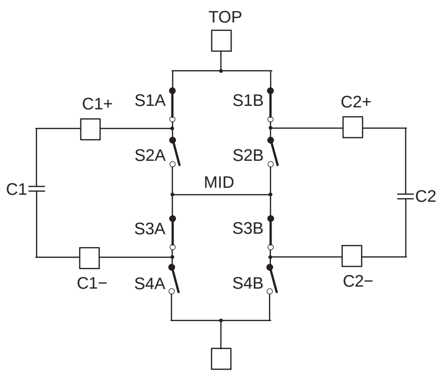


Figure 23. Mode 3 (1:2 or 2:1) All Switches Set for Phase 1 and Reverse State for Phase 2

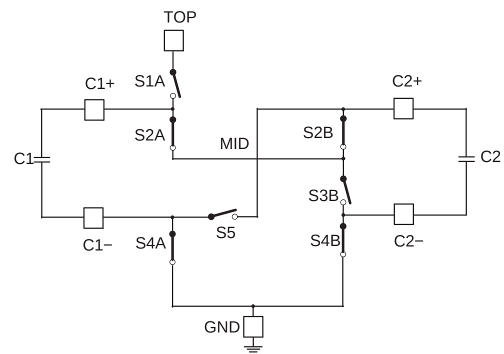


Figure 24. Mode 4 (1:3 or 3:1) All Switches Set for Phase 1 and Reverse State for Phase 2

Light−Load Operation

The power transistors used in the charge pump are very large in size. The dynamic loss from the switching the power transistors is not small and increases its propor− tion of the total power consumption as the load gets light. To save power, the FAN5602 switches, when the load is less than 10mA, from constant frequency to pulse−skip− ping mode (PFM) for modes 2:3(3:2), 1:2(2:1) and 1:3(3:1), except mode 1:1. In PFM mode, the linear loop is disabled and the error amplifier is turned off. A PFM comparator is used to setup an upper threshold and a lower threshold for the output. When the output is lower than the lower threshold, the oscillator is turned on and the charge pump starts working and keeps delivering charges from the input to the output until the output is higher than the upper threshold. The oscillator shuts off power transistors and delivers the charge to the output from the output capacitor. PFM operation is not used for Mode 1:1, even if at light load. Mode 1:1 is designed as an LDO with the oscillator off. The power transistors at LDO mode are not switching and therefore do not have the dynamic loss.

Switching from linear operation to PFM mode (I_{LOAD} < 10 mA) and from PFM to linear mode (I_{LOAD} > 10 mA) is automatic, based on the load current, which is monitored all the time.

Short Circuit

When the output voltage is lower than 150mV, the FAN5602 enters short−circuit condition. In this condition, all power transistors are turned off. A small transistor shorting the input and the output turns on and charges the output. This transistor stays on as long as the V_{OUT} < 150 mV. Since this transistor is very small, the current from the input to the output is limited. Once the short at the output is eliminated, this transistor is large enough to charge the output higher than 150mV and the FAN5602 enters soft−start period.

Soft Start

The FAN5602 uses a constant current, charging a low−pass filter to generate a ramp. The ramp is used as reference voltage during the startup. Since the ramp starts at zero and goes up slowly, the output follows the ramp and inrush current is restricted. When the ramp is higher than bandgap voltage, the bandgap voltage supersedes ramp as reference and the soft start is over. The soft start takes about 500 μs.

Thermal Shutdown

The FAN5602 goes to thermal shutdown if the junction temperature is over 150°C with 15°C hysteresis.

APPLICATION INFORMATION

Using the FAN5602 to Drive LCD Backlighting

The FAN5602 4.5V option is ideal for driving the back−lighting and flash LEDs for portable devices. One FAN5602 device can supply the roughly 150mA needed to power both the backlight and the flash LEDs. Even though drawing this much current from the FAN5602 drives the part out of the 3% output regulation, it is not a problem. The backlight and flash LEDs still produce opti− mal brightness at the reduced regulation. When building this circuit, use ceramic capacitors with low ESR. All capacitors should be placed as close as possible to the FAN5602 in the PCB layout.

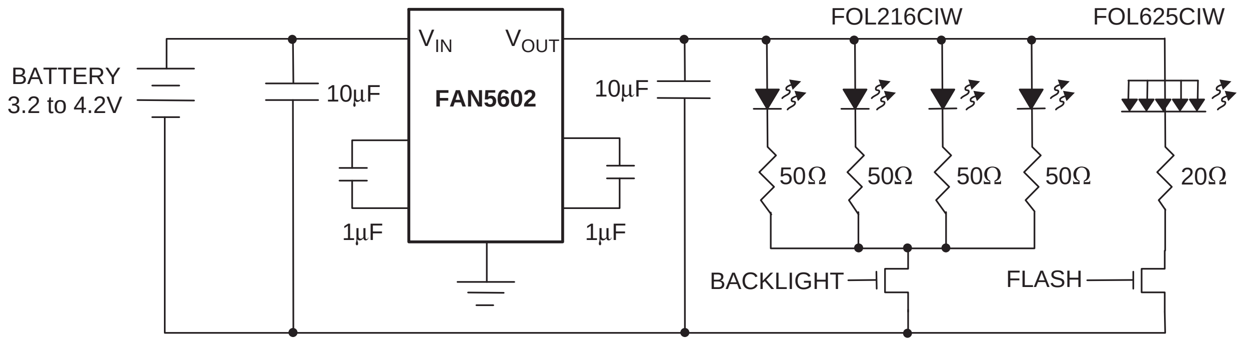
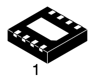


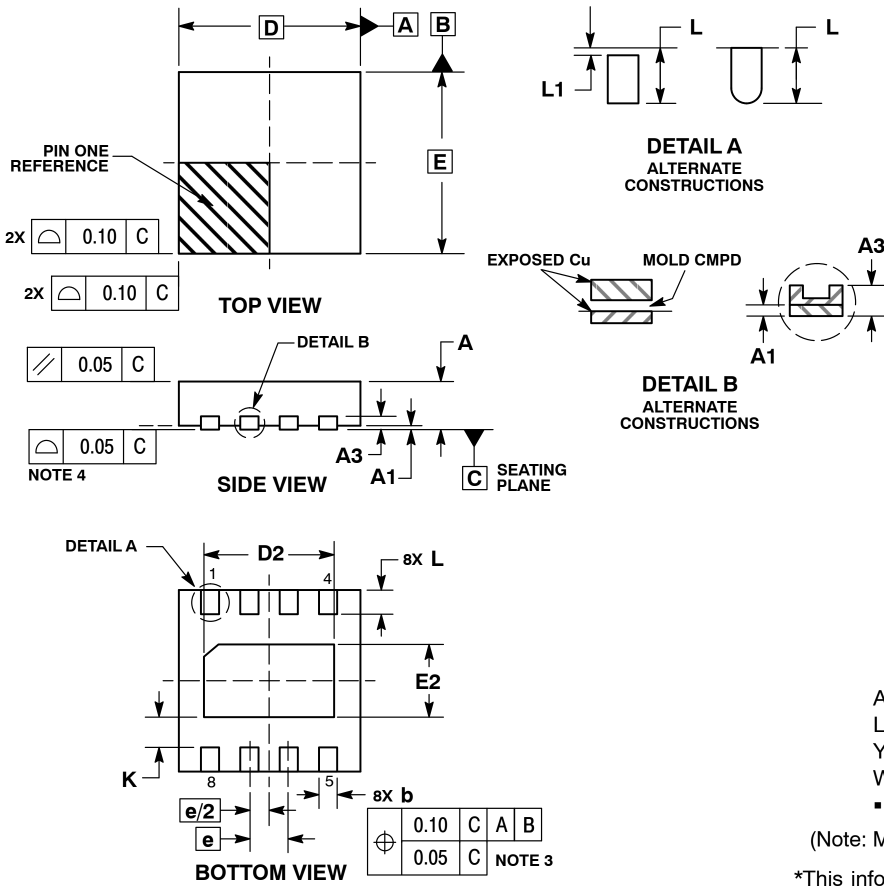
Figure 25. Circuit for Backlighting / Flash Application



SCALE 2:1

WDFN8 3x3, 0.65P
CASE 511CD
ISSUE O

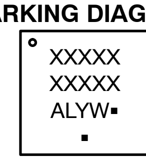
DATE 29 APR 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.05	2.25
E	3.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

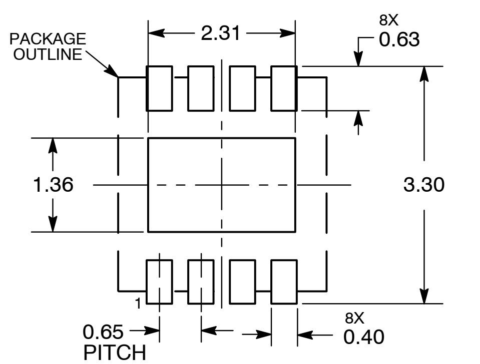


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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