Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor’s system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.
FAN4149
Ground Fault Interrupter

Features
- Meets 2015 UL943 Self-Test Requirements (in combination with FAN41501)
- Precision Sense Amplifier and Bandgap Reference
- Low-V_{OS} Offset for Direct DC Coupling of Sense Coil
- Built-in Noise Filter
- High-Current SCR Gate Driver
- Adjustable Sensitivity
- 500 µA Quiescent Current
- Minimum External Components
- Ideal for 120 V or 220 V Systems
- Space-Saving, SOT23, 6-Pin Package

Applications
- GFCI Output Receptacle
- GFCI Circuit Breakers
- Portable GFCI Cords
- Residual-Current Devices (RCD)

Description
The FAN4149 is a low-power controller for detecting hazardous current paths to ground and ground-to-neutral faults. The FAN4149 application circuit opens the load contacts before a harmful shock occurs.

The FAN4149, in combination with the FAN41501 auto-monitoring digital controller, meets the 2015 UL943 self-test requirements for permanently connected GFCI products. The FAN4149 detects and protects against a hot-wire-to-ground fault and a neutral-to-line/load short. The FAN41501 periodically monitors the FAN4149 and critical GFI components to comply with the 2015 UL943 requirements. The minimum number of components and the small 6-pin package allow for a dense, flexible, application solution.

The FAN4149 contains a precision bandgap 14 V shunt regulator, precision low-V_{OS} sense amplifier, time-delay noise filter, window-detection comparators, and an SCR driver. The shunt regulator operates with a low quiescent current, which allows for a high value, low-wattage series supply resistor. The internal temperature compensated shunt regulator, sense amplifier, and bias circuitry provide for precision ground-fault detection. This enables the use of larger component variations so that binning or trimming external components is not required. The typical ±50 µV V_{OS} sense amplifier offset allows for direct DC coupling of the sense coil. This eliminates the large AC-coupling capacitor. The internal delay filter rejects high-frequency noise spikes common with inductive loads. This decreases false nuisance tripping. The SCR driver provides increased current and temperature compensation to allow for a wider selection of external SCRs.

The minimum number of external components and the 6-pin SOT23 package allow a low-cost, compact design and layout.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN4149M6X</td>
<td>-35°C to +85°C</td>
<td>6-Lead, SOT23, JEDEC M0-178, 1.6 mm</td>
<td>Tape and Reel</td>
</tr>
</tbody>
</table>
Block Diagram

Figure 1. Block Diagram

Typical Application

Figure 2. Typical Application(1,2)

Table 1. Typical Values

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R1: 75 kΩ</td>
<td>R₂: 75 kΩ</td>
<td>R3: 1 MΩ</td>
<td>R4: 909 kΩ</td>
<td>C1: 22 nF</td>
</tr>
<tr>
<td>R₁: 470 Ω</td>
<td>C3: 5.6 nF</td>
<td>C4: 220 nF</td>
<td>C5: 1 μF</td>
<td></td>
</tr>
<tr>
<td>R.TEST₁: 15 kΩ</td>
<td>R.TEST₂: 10 kΩ</td>
<td>R.SET: 750 kΩ (3)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

XMFR: Magnetic Metals 5029/F3006

Notes:
1. Contact Fairchild for self-test requirement details.
2. Portions of this schematic are subject to U.S. patents 8,085,516 and 8,760,824.
3. Value depends on sense-coil characteristics and application.
**Pin Configuration**

![Pin Configuration Diagram]

**Figure 3. Pin Configuration**

**Pin Definitions**

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SCR</td>
<td>Gate drive for external SCR</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Supply input for FAN4149 circuitry</td>
</tr>
<tr>
<td>3</td>
<td>VS</td>
<td>Supply input for FAN4149 circuitry</td>
</tr>
<tr>
<td>4</td>
<td>VREF</td>
<td>Non-inverting input for current sense amplifier</td>
</tr>
<tr>
<td>5</td>
<td>VFB</td>
<td>Inverting input for current sense amplifier</td>
</tr>
<tr>
<td>6</td>
<td>Amp Out</td>
<td>An external resistor connected to VFB sets the IFAULT sensitivity threshold</td>
</tr>
</tbody>
</table>
## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>Continuous Current, VS to GND</td>
<td>15</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>Continuous Voltage to GND, All Pins</td>
<td>-0.8</td>
<td>16.0</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature Range</td>
<td>Human Body Model, ANSI/ESDA/JEDEC JS-001-2012</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge Capability</td>
<td>Charged Device Model, JESD22-C101</td>
<td>2.5</td>
<td></td>
<td>kV</td>
</tr>
</tbody>
</table>

## DC Electrical Characteristics

Unless otherwise specified, $T_A=25^\circ$C, $I_{\text{shunt}}=1$ mA, and referencing Figure 2.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{REG}}$</td>
<td>Power Supply Shunt Regulator Voltage</td>
<td>VS to GND</td>
<td>13.7</td>
<td>14.0</td>
<td>14.3</td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>Line to GND=10 V</td>
<td>425</td>
<td>500</td>
<td>575</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{\text{REF}}$</td>
<td>Reference Voltage</td>
<td>$V_{\text{REF}}$ to GND</td>
<td>6.85</td>
<td>7.00</td>
<td>7.15</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{TH}}$</td>
<td>Trip Threshold</td>
<td>Amp Out to $V_{\text{REF}}$</td>
<td>4.35</td>
<td>4.50</td>
<td>4.65</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{OS}}$</td>
<td>Amplifier Offset</td>
<td>Gain=1000</td>
<td>-175</td>
<td>±50</td>
<td>175</td>
<td>µV</td>
</tr>
<tr>
<td>$I_{\text{OS}}$</td>
<td>Amplifier Input Offset&lt;sup&gt;(5)&lt;/sup&gt;</td>
<td>Design Value</td>
<td>-50</td>
<td>0</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>$G$</td>
<td>Amplifier DC Gain&lt;sup&gt;(5)&lt;/sup&gt;</td>
<td>Design Value</td>
<td>100</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$f_{\text{GBW}}$</td>
<td>Amplifier Gain Bandwidth&lt;sup&gt;(5)&lt;/sup&gt;</td>
<td>Design Value</td>
<td>3</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$V_{\text{SW}+}$</td>
<td>Amplifier Positive Voltage Swing</td>
<td>Amp Out to $V_{\text{REF}}$, $I_{\text{FAULT}}=10$ µA</td>
<td>5.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{SW}-}$</td>
<td>Amplifier Negative Voltage Swing</td>
<td>$V_{\text{REF}}$ to Amp Out, $I_{\text{FAULT}}=-10$ µA</td>
<td>5.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{sink}}$</td>
<td>Amplifier Current Sink</td>
<td>Amp Out=$V_{\text{REF}} + 3 V_{FB}=V_{\text{REF}} + 100$ mV</td>
<td>400</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{SRL}}$</td>
<td>Amplifier Current Source</td>
<td>Amp Out=$V_{\text{REF}} - 3 V_{FB}=V_{\text{REF}} - 100$ mV</td>
<td>400</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$t_d$</td>
<td>Delay Filter</td>
<td>Delay from $C_1$ Trip to SCR L→H</td>
<td>0.65</td>
<td>1.00</td>
<td>1.35</td>
<td>ms</td>
</tr>
<tr>
<td>$R_{\text{OUT}}$</td>
<td>SCR Output Resistance</td>
<td>SCR to GND=250 mV, Amp Out=$V_{\text{REF}}$</td>
<td>0.5</td>
<td>1.0</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>$V_{\text{OUT}}$</td>
<td>SCR Output Voltage</td>
<td>SCR to GND, Amp Out=$V_{\text{REF}}$</td>
<td>1</td>
<td>10</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{\text{OUT}}$</td>
<td>SCR Output Voltage</td>
<td>SCR to GND, Amp Out=$V_{\text{REF}} + 4$ V</td>
<td>3.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{OUT}}$</td>
<td>SCR Output Current</td>
<td>SCR to GND=1 V Amp Out=$V_{\text{REF}} + 4$ V, $I_{\text{shunt}}=2$ mA</td>
<td>650</td>
<td>725</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

**Notes:**

1. Maximum $V_{\text{OS}}$ offset temperature cycling drift from initial value (JEDEC JESD22-A104).
2. Guaranteed by design, not tested in production.
Functional Description

Refer to Figure 2.

The FAN4149 is a GFCI controller for AC ground-fault circuit interrupters. The low-V_{OS} offset for the sense amplifier allows for direct DC coupling of the sense coil when the FAN4149 is biased with a full-wave diode bridge. This allows for the FAN4149 to be used with the FAN41501 digital auto-monitoring controller to provide for a low-BOM-cost, complete, GFI solution with self testing for the critical GFCI components.

The internal shunt regulator rectifier circuit is supplied from the full-wave rectifier bridge and 75 kΩ series resistor. A typical 220 nF V_s bypass capacitor is used to filter the V_{AC} ripple voltage. The internal 14 V shunt regulator uses a precision temperature-compensated bandgap reference. The combination of precision reference circuitry and precision sense amplifier provides for an accurate ground-fault tolerance. This allows for selection of external components with wider and lower-cost parameter variations. Due to the low quiescent current, a high-value external series resistor (R_s) can be used to reduce the maximum power wattage required for this resistor. The 14 V shunt regulator generates the V_{REF} reference voltage for the sense amplifier's (A_1) non-inverting input (AC ground reference). It also supplies the bias for the delay timer (t_1), comparators (C_1 & C_2), and the SCR driver.

The secondary winding of the sense transformer is connected to pin 4 (VREF) and to a resistor, R_{IN}, which is directly DC connected to the inverting input of the sense amplifier at pin 5 (VFB). The feedback resistor (R_{SET}) converts the sense transformer’s secondary current to a voltage at pin 6 (Amp Out). This voltage is compared to the internal window comparator (C_1 & C_2). When the Amp Out voltage exceeds the ±V_{TH} threshold voltage, the window comparator triggers the internal delay timer. The output of the window comparator must stay HIGH for the duration of the t_1 timer. If the window comparator's output goes LOW, the internal delay timer starts a reset cycle. If the window comparator's output is still HIGH at the end of the t_1 pulse, the SCR driver enforces current source I_1 and disables Q1. Current source I_1 then enables the SCR, which energizes the solenoid, opens the contact switches to the load, and removes the hazardous ground fault. The window comparator allows for detection of a positive or negative I_{FAULT} signal, independent from the phase of the line voltage.

Calculation of R_{SET} Resistor

The Amp Out signal must exceed the window comparator's V_{TH} threshold voltage for longer than the delay timer and calculated by:

\[ V_{TH} = I_{FAULT} \times 1.22 \times R_{SET} \times \cos(2\pi \times (t/2P)) / N \]  
\[ R_{SET} = (V_{TH} \times N) / (1.22 \times I_{FAULT} \times \cos(\pi \times t/P)) \]  

where:

\[ V_{TH} = 4.5 \text{ V} \]  
\[ I_{FAULT} = 5 \text{ mA}_{\text{RMS}} \text{ (UL943)} \]

T = 1 ms (timer delay)
P = Period of the AC Line (1/60 Hz)
N = Ratio of secondary-to-primary turns (1000:1)
R_{SET} = 750 kΩ (standard 1% value)

In practice, the transformer is non-ideal, so R_{SET} may need to be adjusted by up to 30% to obtain the desired I_{FAULT} trip threshold.

Calculation of V_{OS} Trip Threshold Error

Since the sense coil is directly connected to the feedback of the sense amplifier, the V_{OS} offset introduces an I_{FAULT} threshold error. This error can be calculated as follows:

\[ \text{%Error} = 100 \times (V_{OS} \times R_{SET}) / (R_{IN} + R_{LDC}) / V_{TH} \]  

where:

\[ V_{OS} = \pm 175 \mu \text{V} \text{ (worst case)} \]  
\[ \pm 50 \mu \text{V} \text{ (typical)} \]  
\[ R_{SET} = 750 \text{ kΩ} \]  
\[ R_{IN} = 470 \text{ Ω} \text{ (typical value)} \]  
\[ R_{LDC} = 75 \text{ Ω} \text{ (sense coil secondary DC resistance)} \]  
\[ V_{TH} = 4.5 \text{ V} \]  
\[ \text{%Error} = \pm 5.4\% \text{ (worst case)} \]  
\[ \pm 1.5\% \text{ (typical)} \]

The V_{OS} ±100 µV maximum drift specification is based on temperature cycling per JEDEC JESD22-A104, Condition B, 850 temperature cycles at -55°C to +125°C.

Grounded Neutral Detection

If the neutral load terminal side is incorrectly connected to the earth ground, the sense coil does not correctly detect the hazardous ground fault current from "load hot" to earth ground due to the partial I_{FAULT} current flowing from the grounded neutral fault (load neutral) to earth ground.

To detect a grounded neutral fault, a grounded neutral coil is required. When a low resistive path occurs from the line neutral and load neutral terminals, the sense and neutral coils are mutually coupled. The mutual coupling produces a positive feedback path around the sense amplifier, which causes the sense amplifier to oscillate. When the peak oscillation voltage exceeds the SCR trigger threshold, the internal delay timer is enabled. Since the amplifier's output signal is crossing the window comparator's trip threshold typically at 6 kHz, the delay timer alternates between detection of a fault/no-fault. The ratio of the fault/no-fault detection time interval determines if the SCR driver is enabled.

The sensitivity of the grounded neutral detection can be changed by the neutral coil turns and the value of C_2 and C_3.
GFCI Self Test Requirement

Starting in June of 2015, UL943 requires all permanently connected GFCI products to perform a self-test function. By adding Fairchild’s FAN41501 product to the FAN4149 application (see Figure 2), a fully compliant 2015 UL943 self-test function can be achieved with two, small, independent, 6-pin, 1.6 mm-wide devices and a minimum number of external components. The 2015 UL code requires that, at power up, the GFCI self test the critical GFCI components -- FAN4149, SCR, sense coil, and solenoid -- within five seconds and thereafter within every three hours. The self-test cycle cannot open the load contacts. If a component failure is detected, the load power must be denied. Refer to the FAN41501 datasheet for more details about the UL943 self-test features.
Typical Performance Characteristics

Unless otherwise specified, $T_A = 25^\circ C$ and according to Figure 2 with SCR disconnected.

Figure 4. Typical Waveforms, No Ground Fault

Figure 5. Typical Waveforms, 4 mA Ground Fault

Figure 6. Typical Waveforms, 5 mA Ground Fault

Figure 7. Typical Waveforms for Grounded Neutral Detection

Continued on the following page…
Typical Performance Characteristics (Continued)

Unless otherwise specified, $T_A = 25^\circ C$ and according to Figure 1 with SCR disconnected.

Figure 8. Typical Waveform for Grounded Neutral Detection

Ch2: AmpOut (Pin 6), 2 V/Div
Typical Temperature Characteristics

Figure 9. Shunt Regulator Voltage vs. Temperature

Figure 10. Quiescent Current vs. Temperature

Figure 11. Reference Voltage vs. Temperature

Figure 12. VH Threshold Voltage vs. Temperature

Figure 13. VL Threshold Voltage vs. Temperature

Figure 14. Typical V_{DS} vs. Temperature

Figure 15. I_{OUT} SCR Out vs. Temperature
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC MO-178, VARIATION AB.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
D. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
E. DIMENSIONS AND TOLERANCING AS PER ASME Y14.5M-1994
F. DRAWING FILE NAME: MA06EREV2

SEE DETAIL A

FAIRCHILD SEMICONDUCTOR

6LD,SOT23,JEDEC
MO-178 VARIATION AB,
6LD,SOT23,JEDEC
SEE DETAIL A

1.30
1.00
0.15
0.05

PIN 1 INDEX AREA

R0.10MIN

GAGE PLANE

R0.10MIN

8°
0°

0.60 REF

0.60
0.30

SEATING PLANE

1.45 MAX

0.15
0.05

C

SYMM

(0.95)
(0.95)

(1.00MIN)

(0.70MIN)

(2.60)

1.90

LAND PATTERN RECOMMENDATION

0.08
0.22

E.C.N. DATE BY/APP'D

A-B

REVISIONS

DESCRIPTION

SYMM

1:1 NA MKT-MA06E 2

11/4/2006 H.ALMEN

22/9/2006 L.HUEBENER

17 JULY 07

17 JULY 07

5 JULY 07

3 JULY 07

CAHNER SHUHMAN KIM TONG MINCHUL

5 JULY 07

DRAWING FILE NAME: MA06EREV2

APPROVALS

DATE

L.HUEBENER

5 JULY 07

H. ALLEN

5 JULY 07

17 JULY 07