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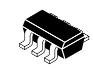
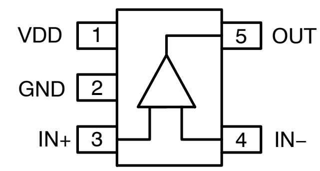
# Single 1 A High-Speed, Low-Side Gate Driver

# FAN3111C, FAN3111E

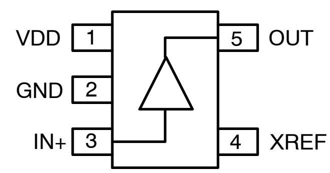


SOT23−5
CASE 527AH

### PIN ASSIGNMENT

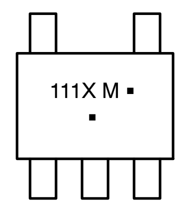



FAN3111C (Top View)




FAN3111E (Top View)

### MARKING DIAGRAM




111X = Specific Device Code
X = C or E
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

### Description

The FAN3111 1 A gate driver is designed to drive an N−channel enhancement−mode MOSFET in low−side switching applications.

Two input options are offered: FAN3111C has dual CMOS inputs with thresholds referenced to $V_{DD}$ for use with PWM controllers and other input−signal sources that operate from the same supply voltage as the driver. For use with low−voltage controllers and other inputsignal sources that operate from a lower supply voltage than the driver, that supply voltage may also be used as the reference for the input thresholds of the FAN3111E. This driver has a single, non−inverting, low−voltage input plus a DC input $V_{XREF}$ for an external reference voltage in the range 2 to 5 V.

The FAN3111 is available in a lead−free finish industry−standard 5−pin SOT23.

### Features

- 1.4 A Peak Sink/Source at $V_{DD}$ = 12 V
- 1.1 A Sink/0.9 A Source at $V_{OUT}$ = 6 V
- 4.5 to 18 V Operating Range
- FAN3111C Compatible with FAN3100C Footprint
- Two Input Configurations:
  - Dual CMOS Inputs Allow Configuration as Non−Inverting or Inverting with Enable Function
  - Single Non−Inverting, Low−Voltage Input for Compatibility with Low−Voltage Controllers
- Small Footprint Facilitates Distributed Drivers for Parallel Power Devices
- 15 ns Typical Delay Times
- 9 ns Typical Rise/8 ns Typical Fall times with 470 pF Load
- 5−Pin SOT23 Package
- Rated from –40°C to 125°C Ambient
- These Devices are Pb−Free and Halogen Free

### Applications

- Switch−Mode Power Supplies
- Synchronous Rectifier Circuits
- Pulse Transformer Driver
- Logic to Power Buffer
- Motor Control

## THERMAL CHARACTERISTICS (Note 1)

| Package | $\Theta_{JL}$ (Note 2) | $\Theta_{JT}$ (Note 3) | $\Theta_{JA}$ (Note 4) | $\Psi_{JB}$ (Note 5) | $\Psi_{JT}$ (Note 6) | Unit |
|---|---|---|---|---|---|---|
| 5−Pin SOT23 | 58 | 102 | 161 | 53 | 6 | °C/W |

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL ($\Theta_{JL}$): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT ($\Theta_{JT}$): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top−side heatsink.
4. Theta_JA ($\Theta_{JA}$): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51−2, JESD51−5, and JESD51−7, as appropriate.
5. Psi_JB ($\Psi_{JB}$): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the MLP−8 package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOIC−8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT ($\Psi_{JT}$): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

## PIN DEFINITIONS

| Pin Number | Name | Description |
|---|---|---|
| 1 | VDD | Supply Voltage. Provides power to the IC. |
| 2 | GND | Ground. Common ground reference for input and output circuits. |
| 3 | IN+ | Non−Inverting Input. Connect to VDD to enable output. |
| 4 | IN− | FAN3111C Inverting Input. Connect to GND to enable output. |
| | XREF | FAN3111E External Reference Voltage. Reference for input thresholds, 2 V to 5 V. |
| 5 | OUT | Gate Drive Output. Held low unless required inputs are present. |

## OUTPUT LOGIC WITH DUAL−INPUT CONFIGURATION

| IN+ | IN− | OUT |
|---|---|---|
| 0 (Note 7) | 0 | 0 |
| 0 (Note 7) | 1 (Note 7) | 0 |
| 1 | 0 | 1 |
| 1 | 1 (Note 7) | 0 |

7. Default input signal if no external connection is made.

## BLOCK DIAGRAMS

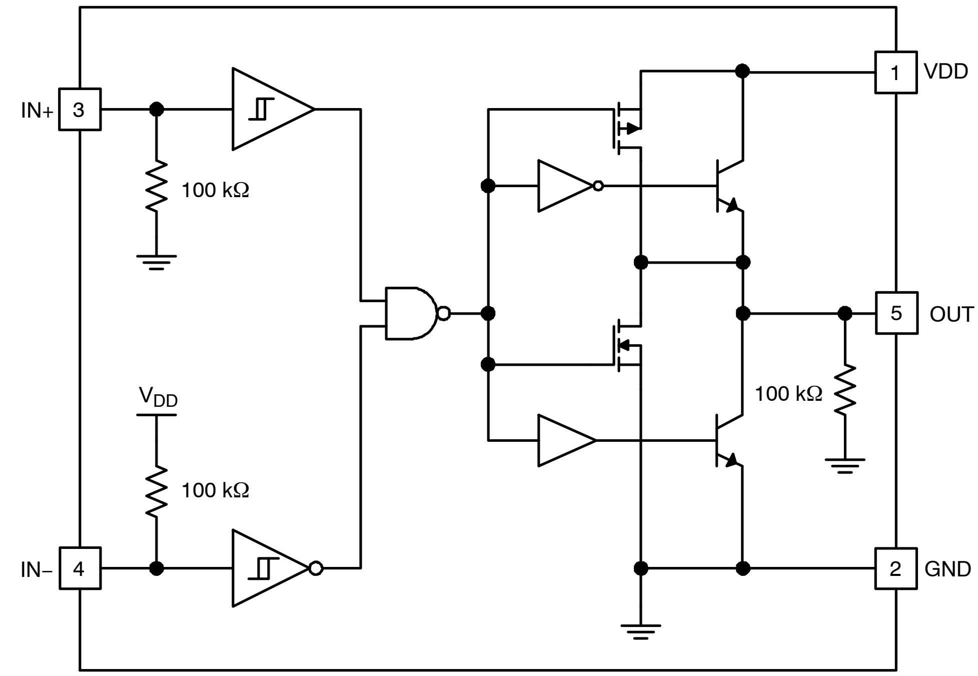



**Figure 1. FAN3111C Simplified Block Diagram**

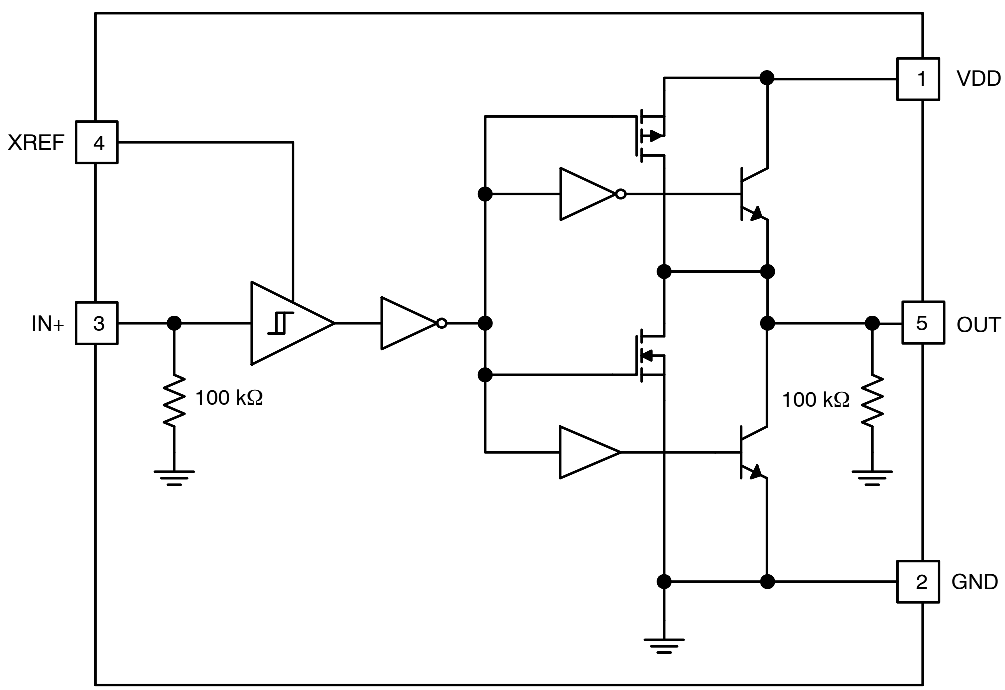



**Figure 2. FAN3111E Simplified Block Diagram**

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | VDD to GND | | −0.3 | 20.0 | V |
| $V_{IN}$ | Voltage on IN to GND | FAN3111C | −0.3 | $V_{DD}$ + 0.3 | V |
| | | FAN3111E | −0.3 | $V_{XREF}$ + 0.3 | V |
| $V_{XREF}$ | Voltage on XREF to GND | FAN3111E | −0.3 | 5.5 | V |
| $V_{OUT}$ | Voltage on OUT to GND | | −0.3 | $V_{DD}$ + 0.3 | V |
| $T_L$ | Lead Soldering Temperature (10 Seconds) | | – | +260 | °C |
| $T_J$ | Junction Temperature | | – | +150 | °C |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | | 4.5 | 18.0 | V |
| $V_{IN}$ | Input Voltage IN | FAN3111C | 0 | $V_{DD}$ | V |
| | | FAN3111E | 0 | $V_{XREF}$ | V |
| $V_{XREF}$ | External Reference Voltage XREF | FAN3111E | 2.0 | 5.0 | V |
| $T_A$ | Operating Ambient Temperature | | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ($V_{DD}$ = 12 V, $V_{XREF}$ = 3.3 V, $T_J$ = −40°C to +125°C unless otherwise noted. Currents are defined as positive into the device and negative out of the device.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $V_{DD}$ | Operating Range | | 4.5 | | 18.0 | V |
| $I_{DD}$ | Static Supply Current | Inputs Not Connected | | 5 | 10 | μA |
| **INPUTS (FAN3111C)** | | | | | | |
| $V_{IL\_C}$ | IN Logic, Low−Voltage Threshold | | 30 | 38 | | %$V_{DD}$ |
| $V_{IH\_C}$ | IN Logic, High−Voltage Threshold | | | 55 | 70 | %$V_{DD}$ |
| $I_{INL}$ | IN Current, Low | IN from 0 to $V_{DD}$ | −1 | | 175 | μA |
| $I_{INH}$ | IN Current, High | IN from 0 to $V_{DD}$ | −175 | | 1 | μA |
| $V_{HYS\_C}$ | Input Hysteresis Voltage | | | 17 | | %$V_{DD}$ |
| **INPUTS (FAN3111E)** | | | | | | |
| $V_{IL\_E}$ | IN Logic, Low−Voltage Threshold | | 25 | 30 | | %$V_{XREF}$ |
| $V_{IH\_E}$ | IN Logic, High−Voltage Threshold | | | 50 | 60 | %$V_{XREF}$ |
| $I_{INL}$ | IN Current, Low | IN from 0 to $V_{XREF}$ | −1 | | 50 | μA |
| $I_{INH}$ | IN Current, High | IN from 0 to $V_{XREF}$ | −50 | | 1 | μA |
| $V_{HYS\_E}$ | Input Hysteresis Voltage | | | 20 | | %$V_{XREF}$ |
| **OUTPUTS** | | | | | | |
| $I_{SINK}$ | OUT Current, Mid−Voltage, Sinking (Note 8) | OUT at $V_{DD}$/2, $C_{LOAD}$ = 47 nF, f = 1 kHz | | 1.1 | | A |
| $I_{SOURCE}$ | OUT Current, Mid−Voltage, Sourcing (Note 8) | OUT at $V_{DD}$/2, $C_{LOAD}$ = 47 nF, f = 1 kHz | | −0.9 | | A |

**ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = 12 V, $V_{XREF}$ = 3.3 V, $T_J$ = −40°C to +125°C unless otherwise noted. Currents are defined as positive into the device and negative out of the device.) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | |
| $I_{PK\_SINK}$ | OUT Current, Peak, Sinking (Note 8) | $C_{LOAD}$ = 47 nF, f = 1kHz | | 1.4 | | A |
| $I_{PK\_SOURCE}$ | OUT Current, Peak, Sourcing (Note 8) | $C_{LOAD}$ = 47 nF, f = 1 kHz | | −1.4 | | A |
| $t_{RISE}$ | Output Rise Time (Note 9) | $C_{LOAD}$ = 470 pF | | 9 | 18 | ns |
| $t_{FALL}$ | Output Fall Time (Note 9) | $C_{LOAD}$ = 470 pF | | 8 | 17 | ns |
| $t_{D1}$, $t_{D2}$ | Output Prop. Delay (Note 9) | **FAN3111C:** 0−12 $V_{IN}$, 1 V/ns Slew Rate | | 15 | 30 | ns |
| | | **FAN3111E:** 0−3.3 $V_{IN}$, 1 V/ns Slew Rate | | | | |
| $I_{RVS}$ | Output Reverse Current Withstand (Note 8) | | | 250 | | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Not tested in production.
9. *See Timing Diagrams*.

## TIMING DIAGRAMS

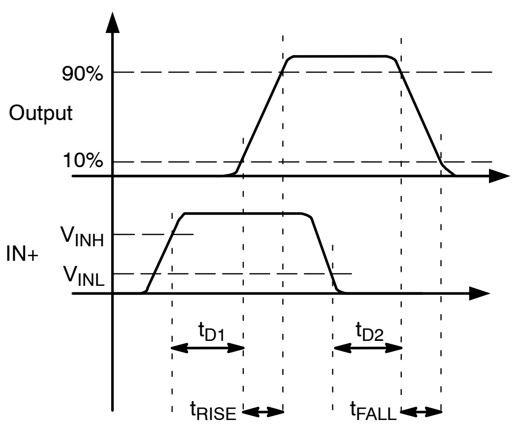



Figure 3. Non−Inverting Waveforms

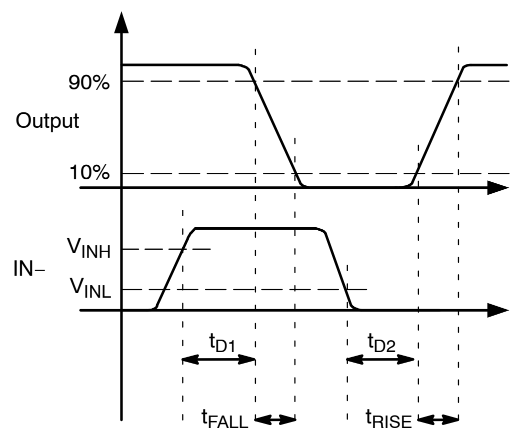



Figure 4. Inverting Waveforms

## TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at 25°C and $V_{DD}$ = 12 V and $V_{XREF}$ = 3.3 V unless otherwise noted)

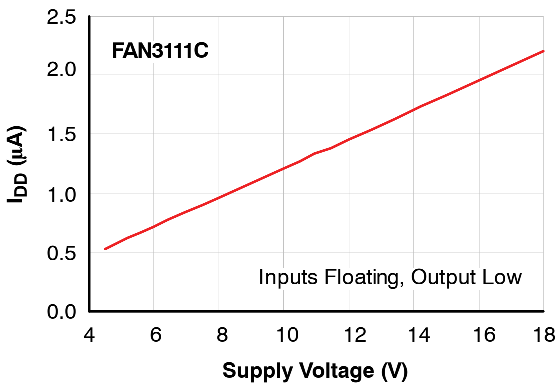



Figure 5. $I_{DD}$ (Static) vs. Supply Voltage

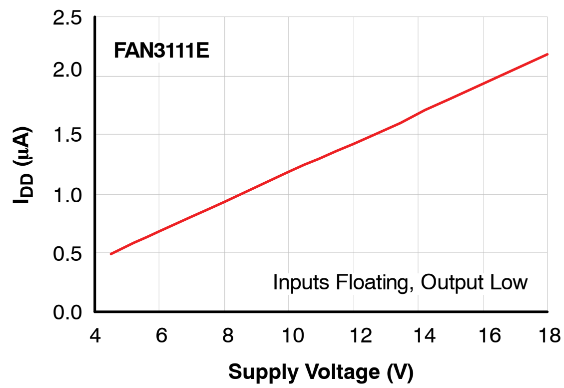



Figure 6. $I_{DD}$ (Static) vs. Supply Voltage

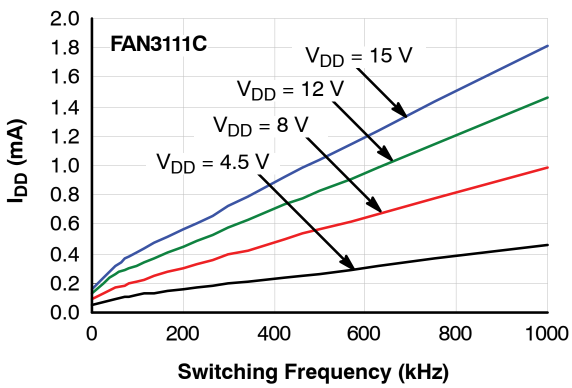



Figure 7. $I_{DD}$ (No−Load) vs. Frequency

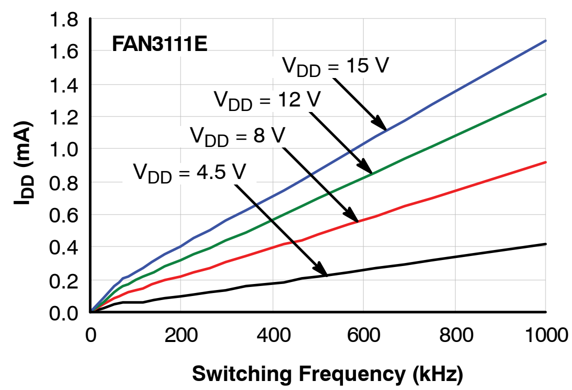



Figure 8. $I_{DD}$ (No−Load) vs. Frequency

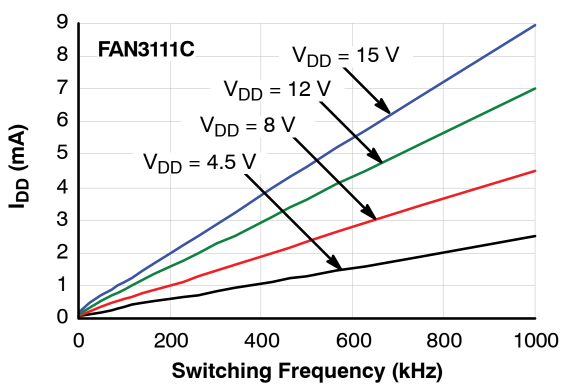



Figure 9. $I_{DD}$ (470 pF Load) vs. Frequency

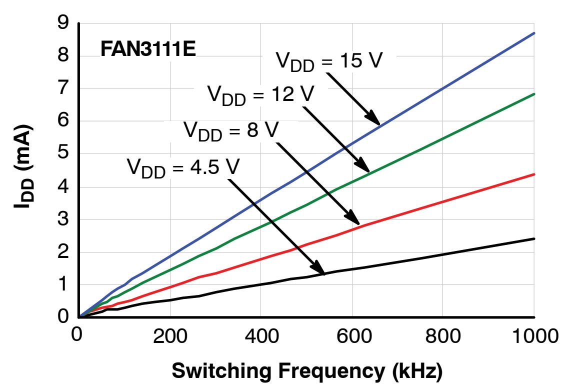



Figure 10. $I_{DD}$ (470 pF Load) vs. Frequency

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and $V_{DD}$ = 12 V and $V_{XREF}$ = 3.3 V unless otherwise noted)

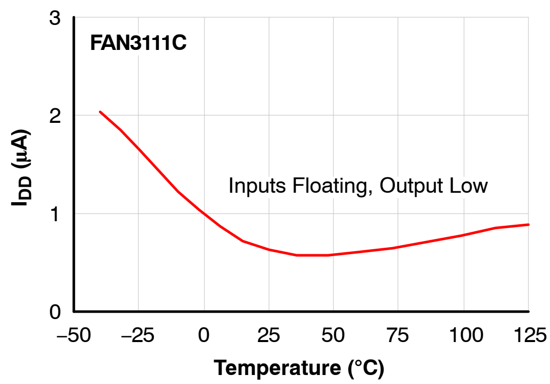



**Figure 11. $I_{DD}$ (Static) vs. Temperature**

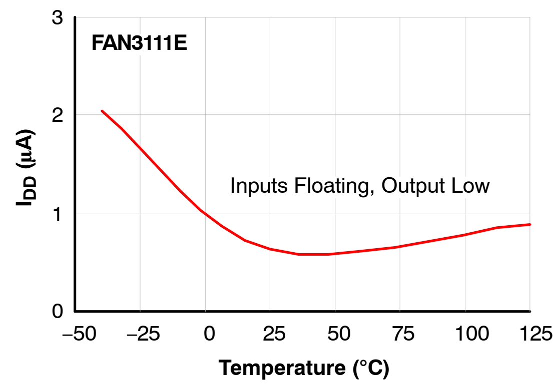



**Figure 12. $I_{DD}$ (Static) vs. Temperature**

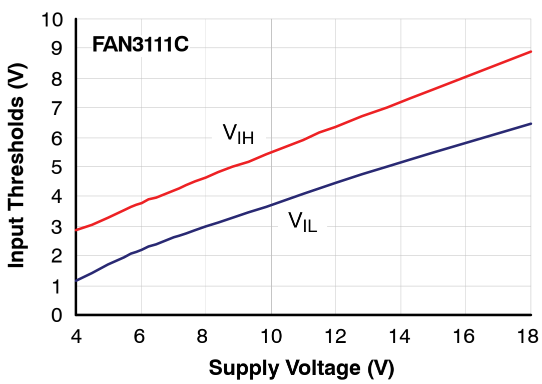



**Figure 13. Input Thresholds vs. Supply Voltage**

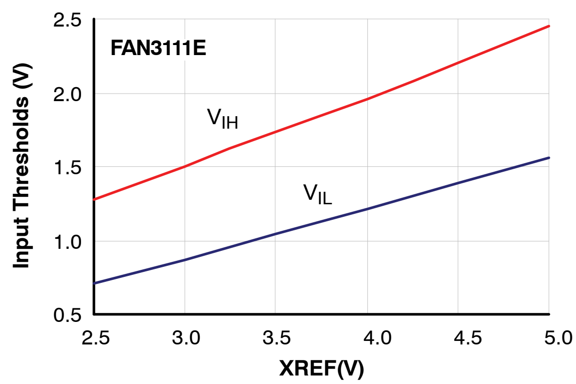



**Figure 14. Input Thresholds vs. XREF Voltage**

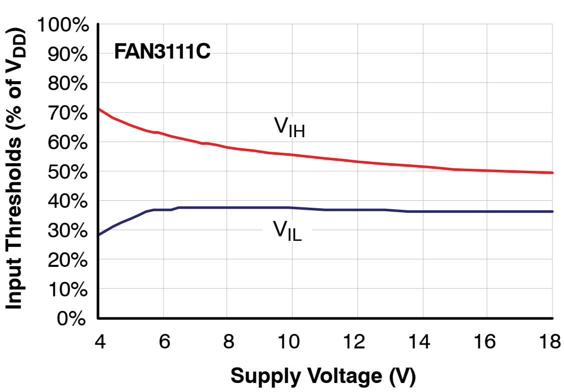



**Figure 15. Input Thresholds % vs. Supply Voltage**

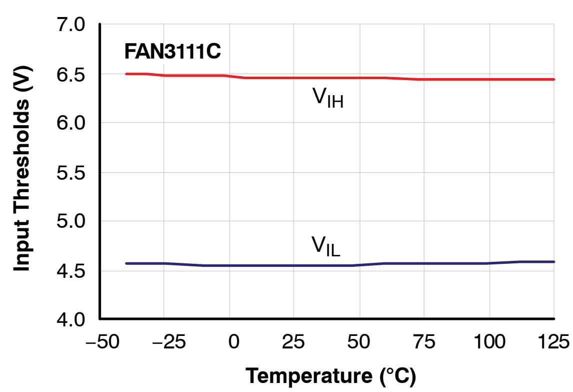



**Figure 16. Input Thresholds vs. Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and $V_{DD}$ = 12 V and $V_{XREF}$ = 3.3 V unless otherwise noted)

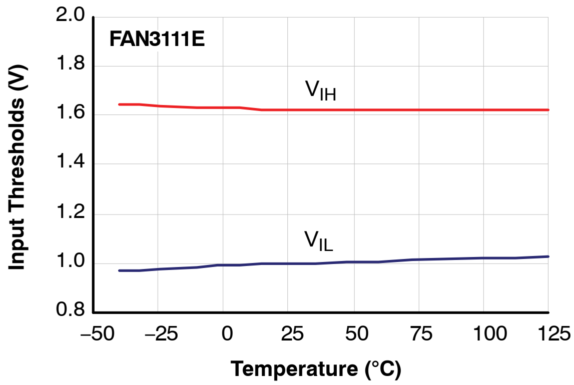



Figure 17. Input Thresholds vs. Temperature

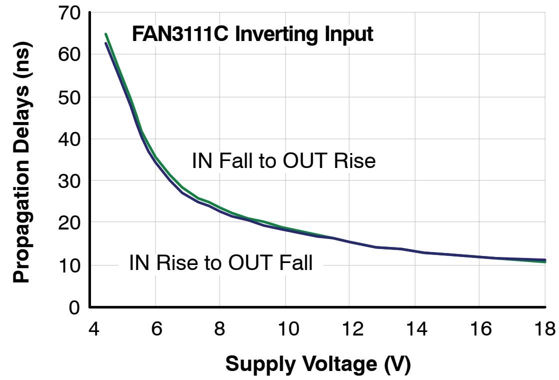



Figure 18. Propagation Delays vs. Supply Voltage

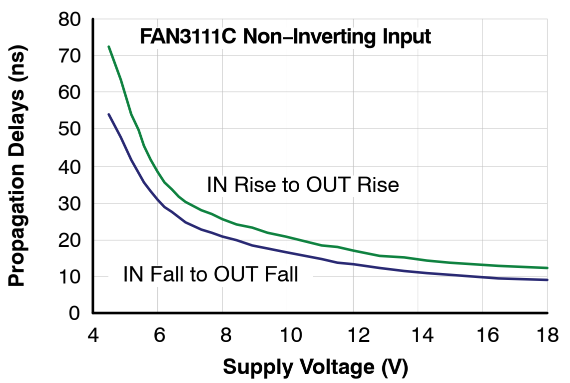



Figure 19. Propagation Delays vs. Supply Voltage

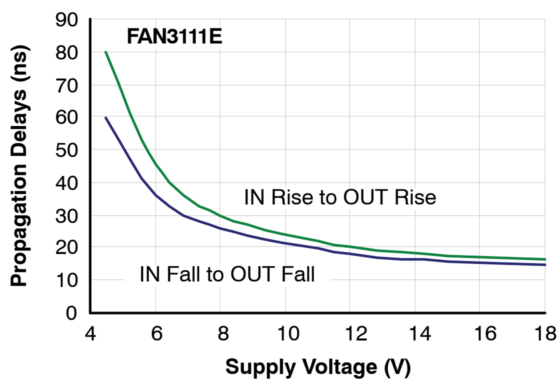



Figure 20. Propagation Delays vs. Supply Voltage

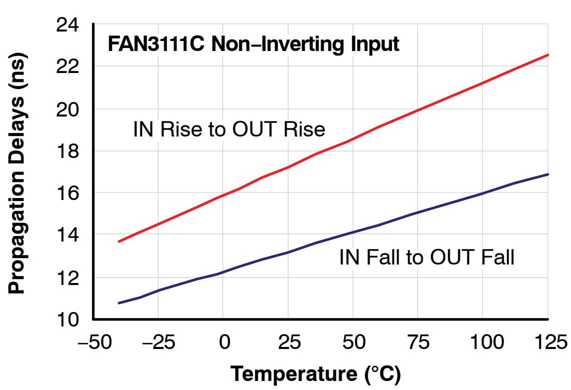



Figure 21. Propagation Delays vs. Temperature

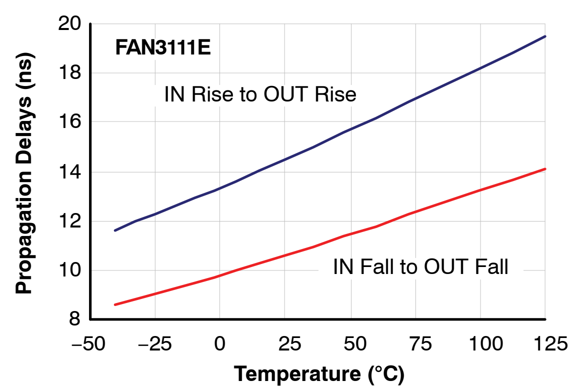



Figure 22. Propagation Delays vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and $V_{DD}$ = 12 V and $V_{XREF}$ = 3.3 V unless otherwise noted)

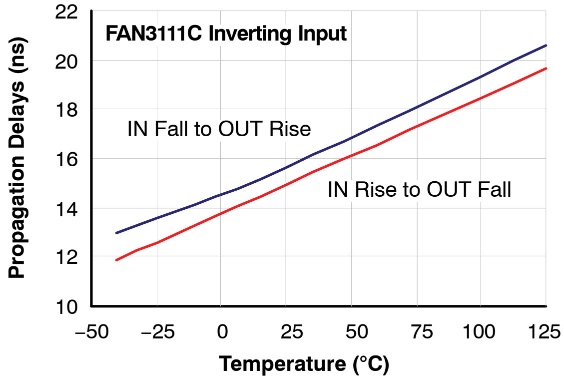



Figure 23. Propagation Delays vs. Temperature

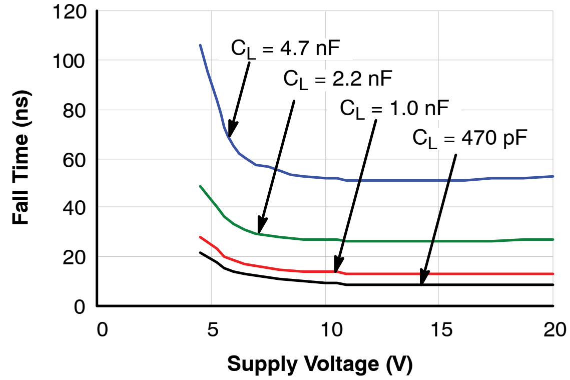



Figure 24. Fall Time vs. Supply Voltage

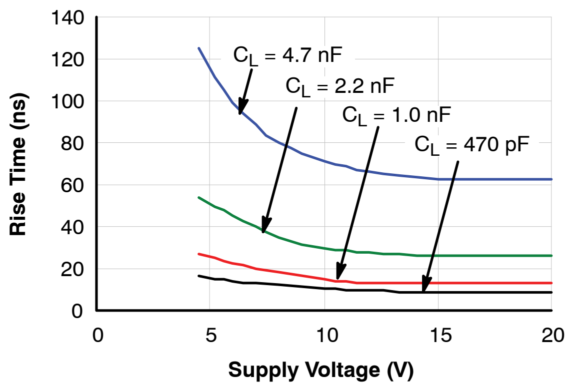



Figure 25. Rise Time vs. Supply Voltage

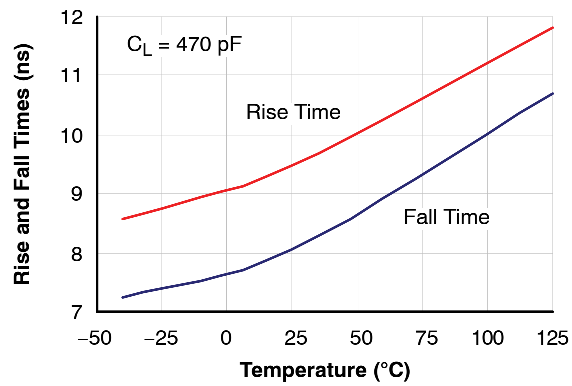



Figure 26. Rise and Fall Times vs. Temperature

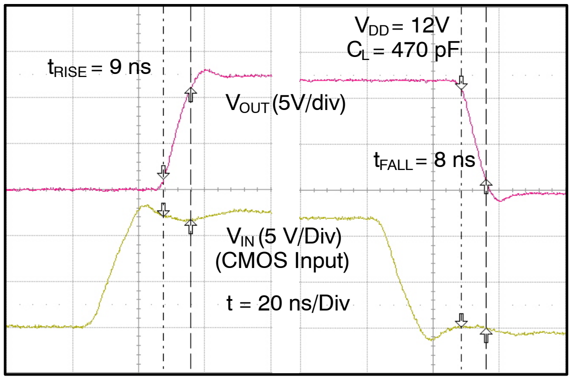



Figure 27. Rise and Fall Waveforms (470 pF)

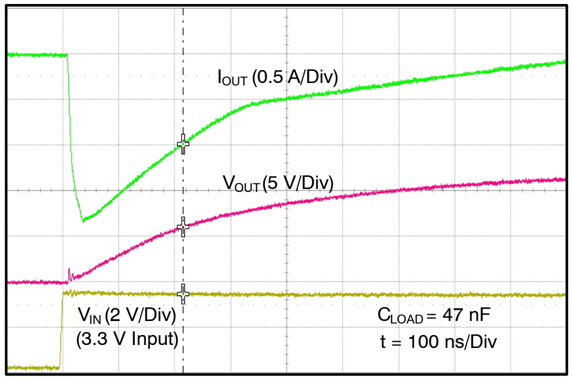



Figure 28. Quasi–Static Source Current ($V_{DD}$ = 12 V)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and $V_{DD}$ = 12 V and $V_{XREF}$ = 3.3 V unless otherwise noted)

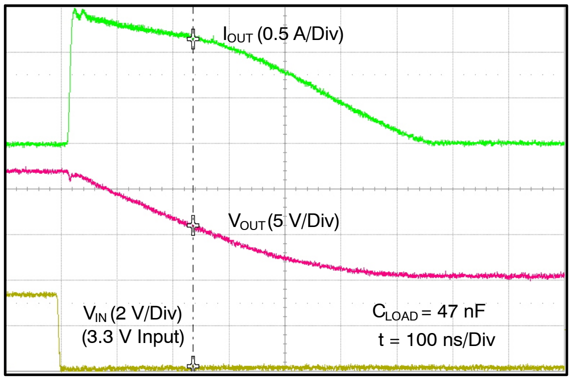



**Figure 29. Quasi−Static Sink Current ($V_{DD}$ = 12 V)**

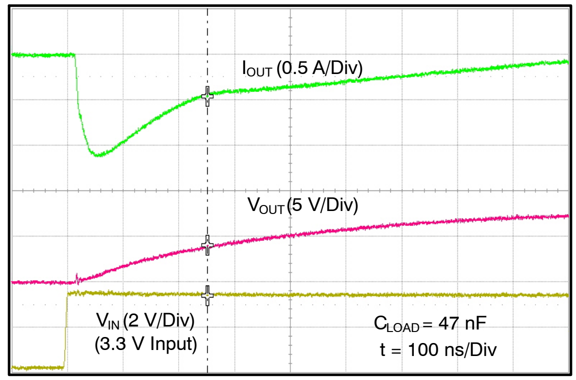



**Figure 30. Quasi−Static Source Current ($V_{DD}$ = 8 V)**

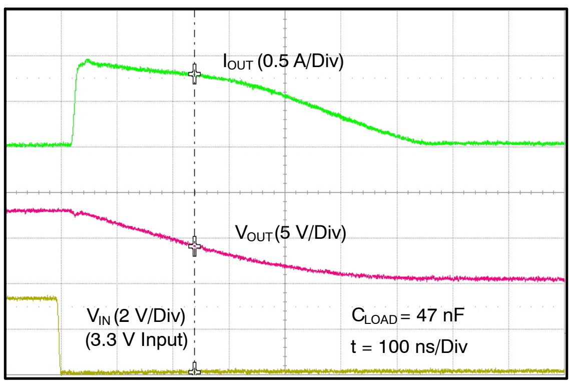



**Figure 31. Quasi−Static Sink Current ($V_{DD}$ = 8 V)**

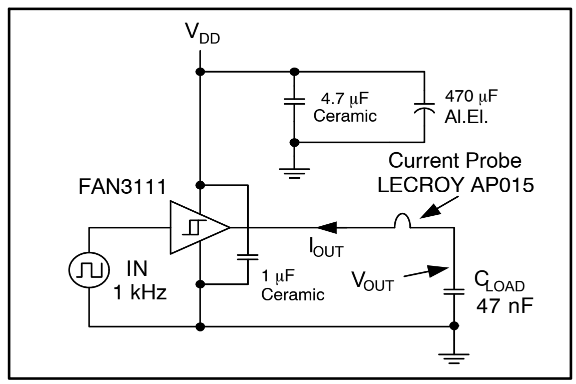



**Figure 32. Quasi−Static $I_{OUT}$/$V_{OUT}$ Test Circuit**

## APPLICATIONS INFORMATION

The FAN3111 offers CMOS− or logic−level−compatible input thresholds. In the FAN3111C, the logic input thresholds are dependent on the $V_{DD}$ level and, with $V_{DD}$ of 12 V, the logic rising−edge threshold is approximately 55% of $V_{DD}$ and the input falling−edge threshold is approximately 38% of $V_{DD}$. The CMOS input configuration offers a hysteresis voltage of approximately 17% of $V_{DD}$. The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input−voltage hysteresis window. This allows setting precise timing intervals by fitting an R−C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

In the FAN3111E, the input thresholds are dependent on the VXREF voltage that typically is chosen between 2 V and 5 V. This range of $V_{XREF}$ allows compatibility with TTL and other logic levels up to 5 V by connecting the XREF pin to the same source as the logic circuit that drives the FAN3111E input stage. The logic rising edge threshold is approximately 50% of $V_{XREF}$ and the input falling−edge threshold is approximately 30% of $V_{XREF}$. The TTL−like input configuration offers a hysteresis voltage of approximately 20% of $V_{XREF}$.

### Startup Operation

The FAN3111 internal logic is optimized to drive ground referenced N−channel MOSFETs as $V_{DD}$ supply voltage rises during startup operation. As $V_{DD}$ rises from 0 V to approximately 2 V, the OUT pin is held LOW by an internal resistor, regardless of the state of the input pins. When the internal circuitry becomes active at approximately 2 V, the output assumes the state commanded by the inputs.

Figure 33 illustrates FAN3111C startup operation with VDD increasing from 0 to 12 V, with the output commanded to the low level (IN+ and IN− tied to ground). Note that OUT is held LOW to maintain an N−channel MOSFET in the OFF state.

Figure 34 illustrates startup operation as $V_{DD}$ increases from 0 to 12 V with the output commanded to the high level (IN+ tied to $V_{DD}$, IN− tied to GND). This configuration might not be suitable for driving high−side P−channel MOSFETs because the low output voltage of the driver would attempt to turn the P−channel MOSFET on with low $V_{DD}$ levels.

Figure 35 illustrates FAN3111E startup operation with the output commanded to the low level (IN+ tied to ground) and the voltage on XREF ramped from 0 to 3.3 V.

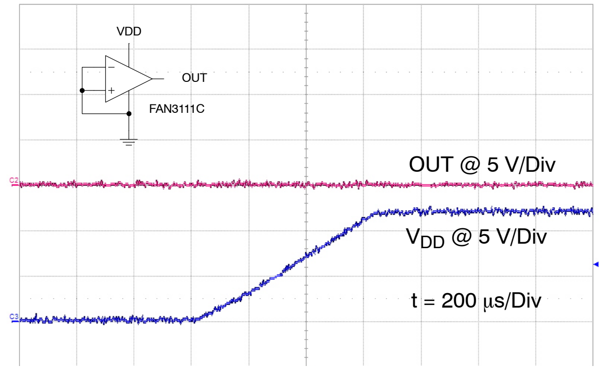



**Figure 33. FAN3111C Startup Operation**

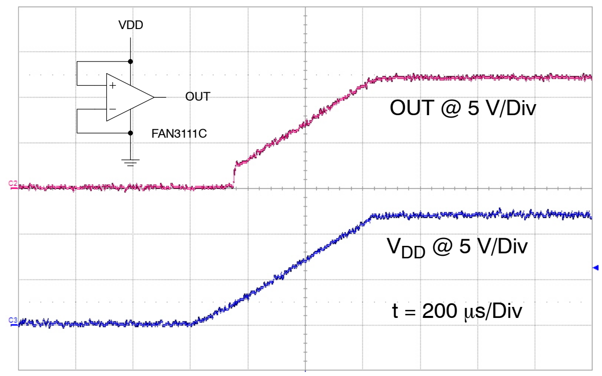



**Figure 34. Startup Operation as $V_{DD}$ Increases**

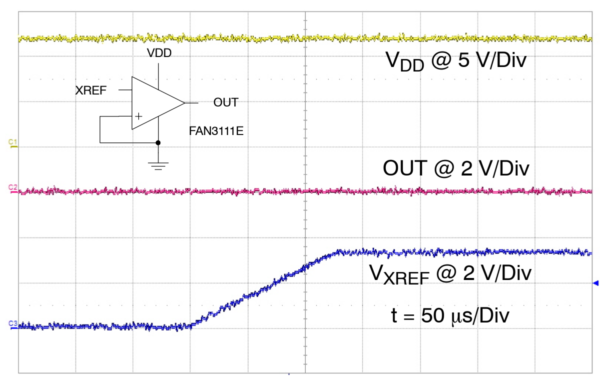



**Figure 35. FAN3111E Startup Operation**

### MillerDrive™ Gate−Drive Technology

FAN3111 drivers incorporate the MillerDrive architecture shown in Figure 36 for the output stage, a combination of bipolar and MOS devices capable of providing large currents over a wide range of supply−voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between

1/3 to 2/3 $V_{DD}$ and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive architecture is to speed up switching by providing the highest current during the Miller plateau region when the gate−drain capacitance of the MOSFET is being charged or discharged as part of the turn−on/turn−off process. For applications with zero voltage switching during the MOSFET turn−on or turn−off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output−pin slew rate is determined by $V_{DD}$ voltage and the load on the output. It is not user adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

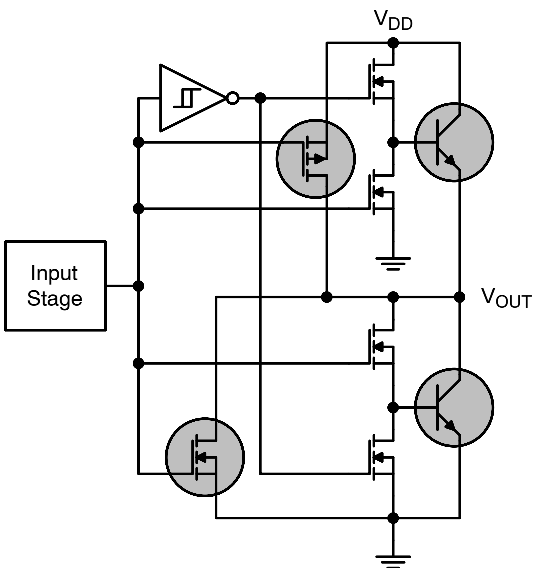



**Figure 36. MillerDrive Output Architecture**

### $V_{DD}$ Bypass Capacitor Guidelines

To enable this IC to turn a power device on quickly, a local, high−frequency, bypass capacitor $C_{BYP}$ with low ESR and ESL should be connected between the $V_{DD}$ and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF often found on driver and controller bias circuits.

A typical criterion for choosing the value of $C_{BYP}$ is to keep the ripple voltage on the $V_{DD}$ supply ±5%. Often this is achieved with a value ≥ 20 times the equivalent load capacitance $C_{EQV}$, defined here as $Q_{gate}/V_{DD}$. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R, which have good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of CBYP may be increased to 50−100 times the $C_{EQV}$ or $C_{BYP}$ may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1−10 nF, mounted closest to the $V_{DD}$ and GND pins to carry the higher−frequency components of the current pulses.

### Layout and Connection Guidelines

The FAN3111 incorporates fast reacting input circuits, short propagation delays, and output stages capable of delivering current peaks over 1 A to facilitate voltage transition times from under 10 ns to over 100 ns. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high−speed switching, while reducing the loop area that can radiate EMI to the driver inputs and other surrounding circuitry.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re−triggering. These effects can be especially obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn−on and turn−off current paths should be minimized as discussed in the following sections.

Figure 37 shows the pulsed gate−drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, $C_{BYP}$, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized $C_{BYP}$ acts to contain the high peak−current pulses within this driver−MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

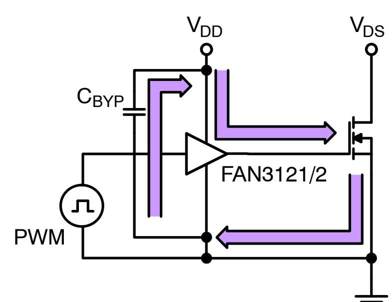



**Figure 37. Current Path for MOSFET Turn−On**

Figure 38 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn−off times, the resistance and inductance in this path should be minimized.

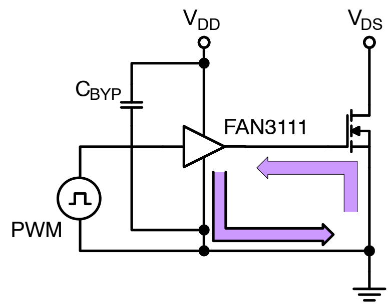



**Figure 38. Current Path for MOSFET Turn−Off**

### Truth Table of Logic Operation

The FAN3111 truth table indicates the operational states using the dual−input configuration. In a non−inverting driver configuration, the IN− pin should be a logic low signal. If the IN− pin is connected to logic high, a disable function is realized, and the driver output remains low regardless of the state of the IN+ pin.

**Table 1. FAN3111 TRUTH TABLE**

| IN+ | IN− | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

In the non−inverting driver configuration in Figure 39, the IN− pin is tied to ground and the input signal (PWM) is applied to the IN+ pin. The IN− pin can be connected to logic high to disable the driver and the output remains low, regardless of the state of the IN+ pin.

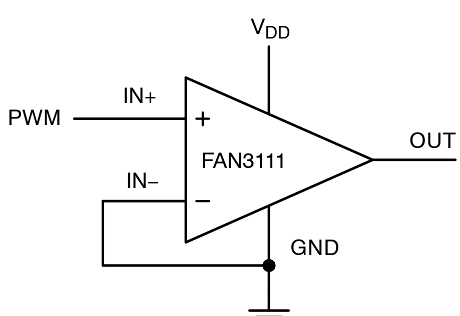



**Figure 39. Dual−Input Driver Enabled, Non−Inverting Configuration**

In the inverting driver application shown in Figure 40, the IN+ pin is tied high. Pulling the IN+ pin to GND forces the output low, regardless of the state of the IN− pin.

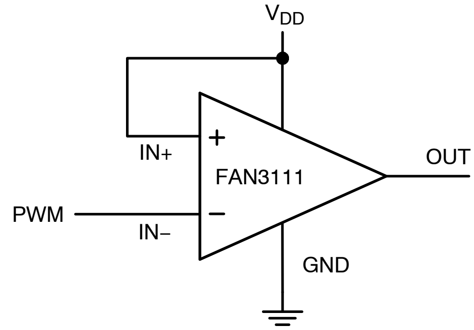



**Figure 40. Dual−Input Driver Enabled, Inverting Configuration**

### Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of three components; $P_{GATE}$, $P_{QUIESCENT}$, and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \qquad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate−source voltage, $V_{GS}$, with gate charge, $Q_G$, at switching frequency, $f_{SW}$, is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \qquad \text{(eq. 2)}$$

Dynamic Pre−drive/Shoot−through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up/pull−down resistors, can be obtained using the graphs in Figure 9 and Figure 10 in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from $V_{DD}$ under actual operating conditions:

$$P_{DYMANIC} = I_{DYNAMIC} \cdot V_{DD} \qquad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction temperature rise with respect to the device lead can be evaluated using thermal equation:

$$T_J = P_{TOTAL} \cdot \theta_{JB} + T_B \qquad \text{(eq. 4)}$$

where:

$T_J$ = driver junction temperature;

$\theta_{JL}$ = thermal resistance from junction to lead;

$T_L$ = lead temperature of device in application.

The power dissipated in a gate−drive circuit is independent of the drive−circuit resistance and is split proportionately among the resistances present in the driver, any discrete series resistor present, and the gate resistance internal to the power switching MOSFET. Power dissipated in the driver may be estimated using the following equation:

$$P_{PKG} = P_{TOTAL}\left(\frac{R_{OUT,DRIVER}}{R_{OUT,DRIVER} + R_{EXT} + R_{GATE,FET}}\right) \quad \text{(eq. 5)}$$

where:

$P_{PKG}$ = power dissipated in the driver package;

$R_{OUT,DRIVER}$ = estimated driver impedance derived from $I_{OUT}$ vs. $V_{OUT}$ waveforms;

$R_{EXT}$ = external series resistance connected between the driver output and the gate of the MOSFET; and

$R_{GATE,FET}$ = resistance internal to the load MOSFET gate and source connections.

## TYPICAL APPLICATION DIAGRAMS

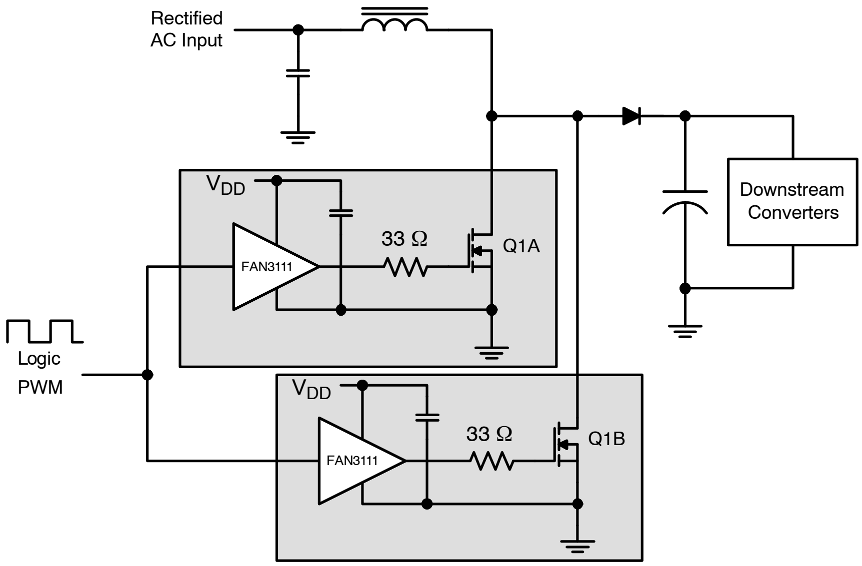



**Figure 41. PFC Boost Circuit Utilizing Distributed Drivers for Parallel Power Switches Q1A and Q1B**

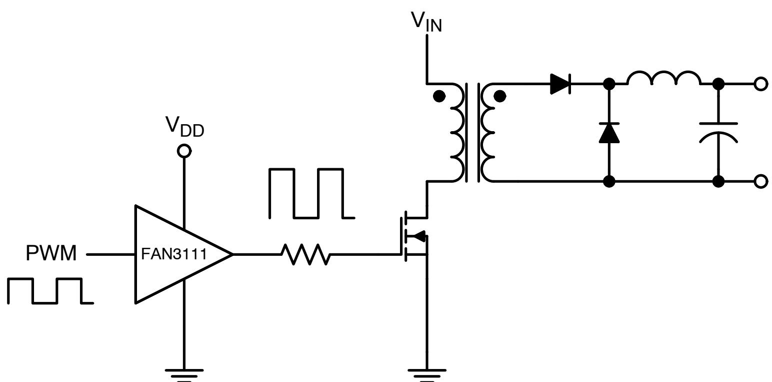



**Figure 42. Driver for Forward Converter Low−Side Switch**

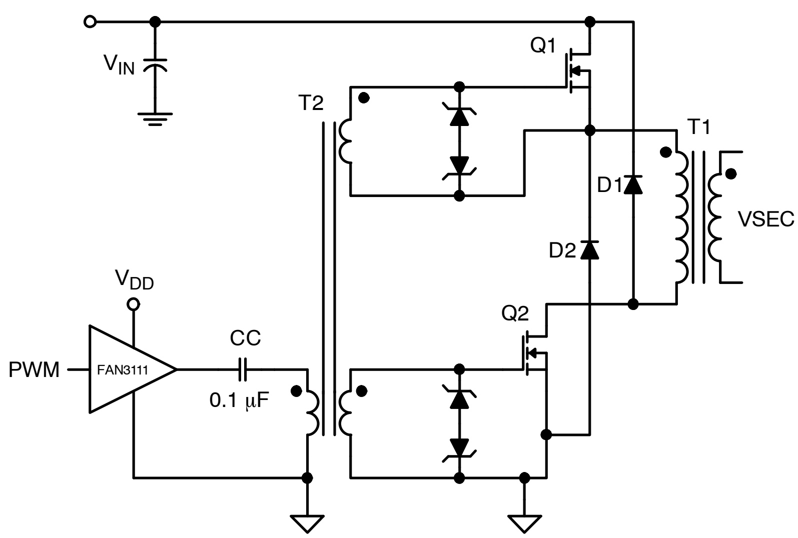



**Figure 43. Driver for Two−Transistor, Forward−Converter Gate Transformer**

## ORDERING INFORMATION

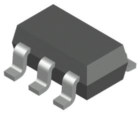
| Part Number | Input Threshold | Package | Shipping† |
|---|---|---|---|
| FAN3111CSX | CMOS | 5−Pin SOT23 | 3,000 / Tape & Reel |
| FAN3111ESX | External | 5−Pin SOT23 | 3,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Table 2. RELATED PRODUCTS**

| Part Number | Type | Gate Drive (Note 10) (Sink/Src) | Input Threshold | Logic | Package |
|---|---|---|---|---|---|
| **FAN3111C** | **Single 1 A** | **+1.1 A/−0.9 A** | **CMOS** | **Single Channel of Dual−Input/Single−Output** | **SOT23−5** |
| **FAN3111E** | **Single 1 A** | **+1.1 A/−0.9 A** | **External (Note 11)** | **Single Non−Inverting Channel with External Reference** | **SOT23−5** |
| FAN3100C | Single 2 A | +2.5 A/−1.8 A | CMOS | Single Channel of Two−Input/One−Output | SOT23−5, MLP6 |
| FAN3100T | Single 2 A | +2.5 A/−1.8 A | TTL | Single Channel of Two−Input/One−Output | SOT23−5, MLP6 |
| FAN3226C | Dual 2 A | +2.4 A/−1.6 A | CMOS | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3226T | Dual 2 A | +2.4 A/−1.6 A | TTL | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3227C | Dual 2 A | +2.4 A/−1.6 A | CMOS | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3227T | Dual 2 A | +2.4 A/−1.6 A | TTL | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3228C | Dual 2 A | +2.4 A/−1.6 A | CMOS | Dual Channels of Two−Input/One−Output, Pin Config.1 | SOIC8, MLP8 |
| FAN3228T | Dual 2 A | +2.4 A/−1.6 A | TTL | Dual Channels of Two−Input/One−Output, Pin Config.1 | SOIC8, MLP8 |
| FAN3229C | Dual 2 A | +2.4 A/−1.6 A | CMOS | Dual Channels of Two−Input/One−Output, Pin Config.2 | SOIC8, MLP8 |
| FAN3229T | Dual 2 A | +2.4 A/−1.6 A | TTL | Dual Channels of Two−Input/One−Output, Pin Config.2 | SOIC8, MLP8 |
| FAN3268T | Dual 2 A | +2.4 A/−1.6 A | TTL | 18 V Half−Bridge Driver: Non−Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables | SOIC8 |
| FAN3223C | Dual 4 A | +4.3 A/−2.8 A | CMOS | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3223T | Dual 4 A | +4.3 A/−2.8 A | TTL | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3224C | Dual 4 A | +4.3 A/−2.8 A | CMOS | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3224T | Dual 4 A | +4.3 A/−2.8 A | TTL | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3225C | Dual 4 A | +4.3 A/−2.8 A | CMOS | Dual Channels of Two−Input/One−Output | SOIC8, MLP8 |
| FAN3225T | Dual 4 A | +4.3 A/−2.8 A | TTL | Dual Channels of Two−Input/One−Output | SOIC8, MLP8 |
| FAN3121C | Single 9 A | +9.7 A/−7.1 A | CMOS | Single Inverting Channel + Enable | SOIC8, MLP8 |
| FAN3121T | Single 9 A | +9.7 A/−7.1 A | TTL | Single Inverting Channel + Enable | SOIC8, MLP8 |
| FAN3122T | Single 9 A | +9.7 A/−7.1 A | CMOS | Single Non−Inverting Channel + Enable | SOIC8, MLP8 |
| FAN3122C | Single 9 A | +9.7 A/−7.1 A | TTL | Single Non−Inverting Channel + Enable | SOIC8, MLP8 |

10. Typical currents with OUT at 6 V and $V_{DD}$ = 12 V.
11. Thresholds proportional to an externally supplied reference voltage.



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ISSUE A

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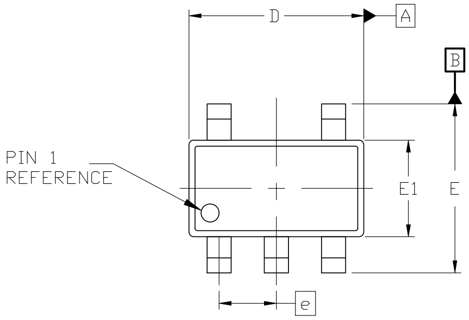
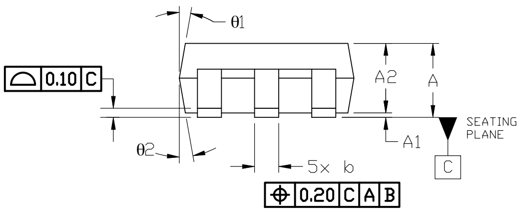
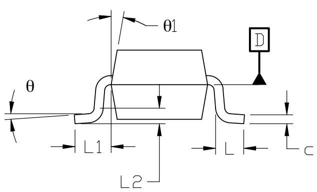



TOP VIEW



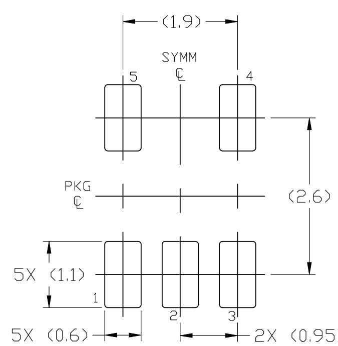

SIDE VIEW




END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

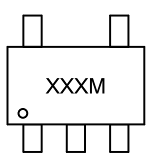
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.90 | — | 1.45 |
| A1 | 0.00 | — | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | — | 0.50 |
| c | 0.08 | — | 0.22 |
| D | 2.90 BSC | | |
| E | 2.80 BSC | | |
| E1 | 1.60 BSC | | |
| e | 0.95 BSC | | |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| L2 | 0.25 REF | | |
| θ | 0° | 4° | 8° |
| θ1 | 0° | 10° | 15° |
| θ2 | 0° | 10° | 15° |




**RECOMMENDED MOUNTING FOOTPRINT**

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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