EVBUM2716/D

500 W, Wide-Mains, NCP1618A-driven Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

The NCP1618A is an innovative multimode power factor controller [1]. The circuit naturally transitions from one operation mode (CCM, CrM or DCM) to another depending on the switching period duration so that the efficiency is optimized over the line/load range. In very light−load conditions, the circuit enters the soft−SKIP mode for minimized losses. Housed in a SO−9 package, the circuit further incorporates the features necessary for building robust and compact PFC stages, with few external components.

The evaluation board is a 500 W wide−mains PFC stage.

EVB ELECTRICAL SPECIFICATIONS

Description	Value	Units
Input Voltage Range	90−265	V rms
Line Frequency Range	45 to 66	Hz
Output Power	500	W
Minimum Output Load Current	13	mA
Maximum Output Load Current	1300	mA
Load Conditions For Efficiency Measurements (10%, 20%,..)	10−100	%
Minimum Efficiency Over the Line/Load Range	94	%
Minimum PF Over The Line Range At Full Load	95	%
Hold−Up Time (the output voltage remaining above 300 V)	> 20	ms
Peak−To−Peak Low Frequency Output Ripple	< 8	%

Note that the evaluation board does not need an external source to power the NCP1618A V_{CC}. A charge pump is implemented on the board which typically provides V_{CC} with a 23−V voltage.

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Publication Order Number:
EVBUM2716/D

THE BOARD

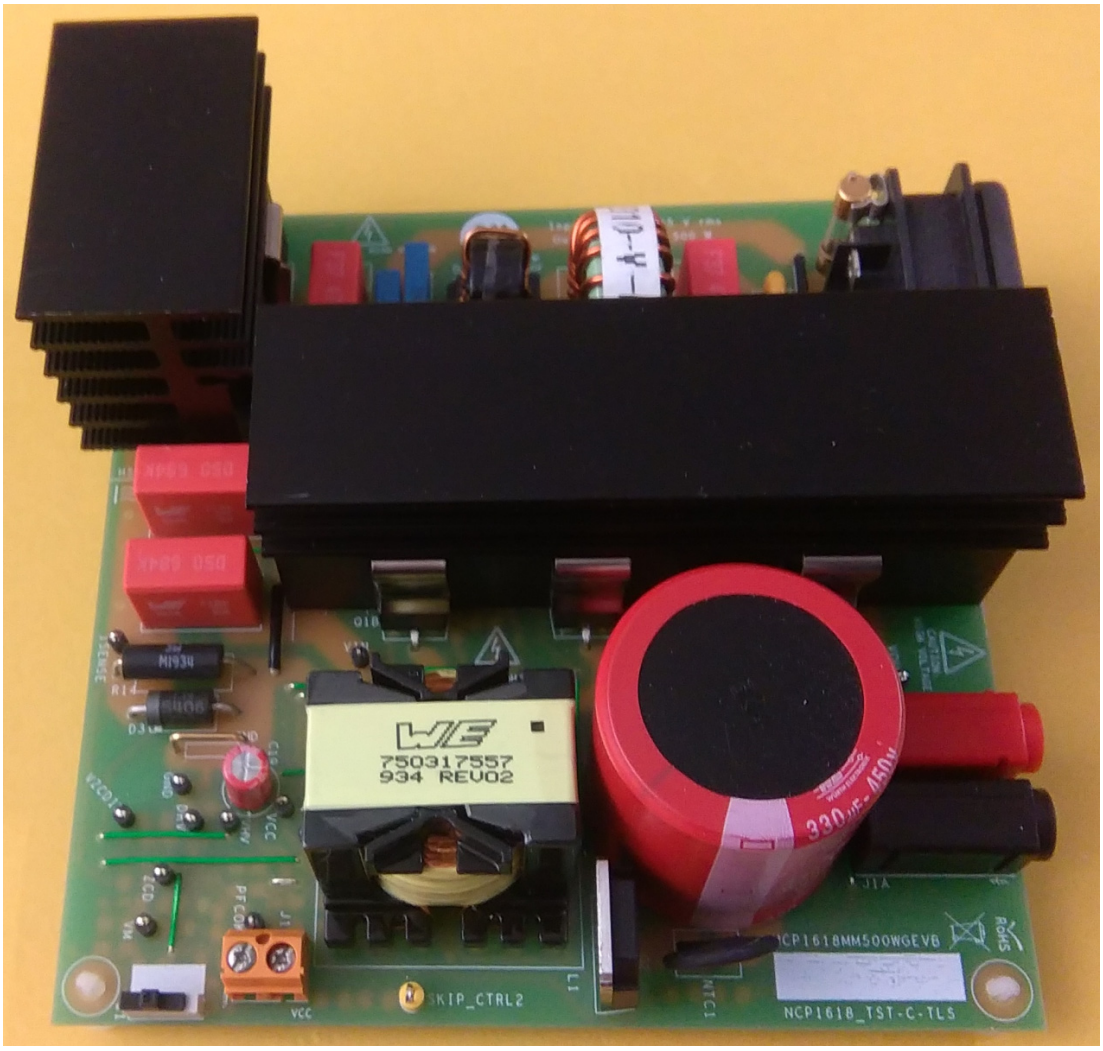


Figure 1. The Wide−Mains, 500 W PFC Stage

APPLICATION SCHEMATIC

Power Section

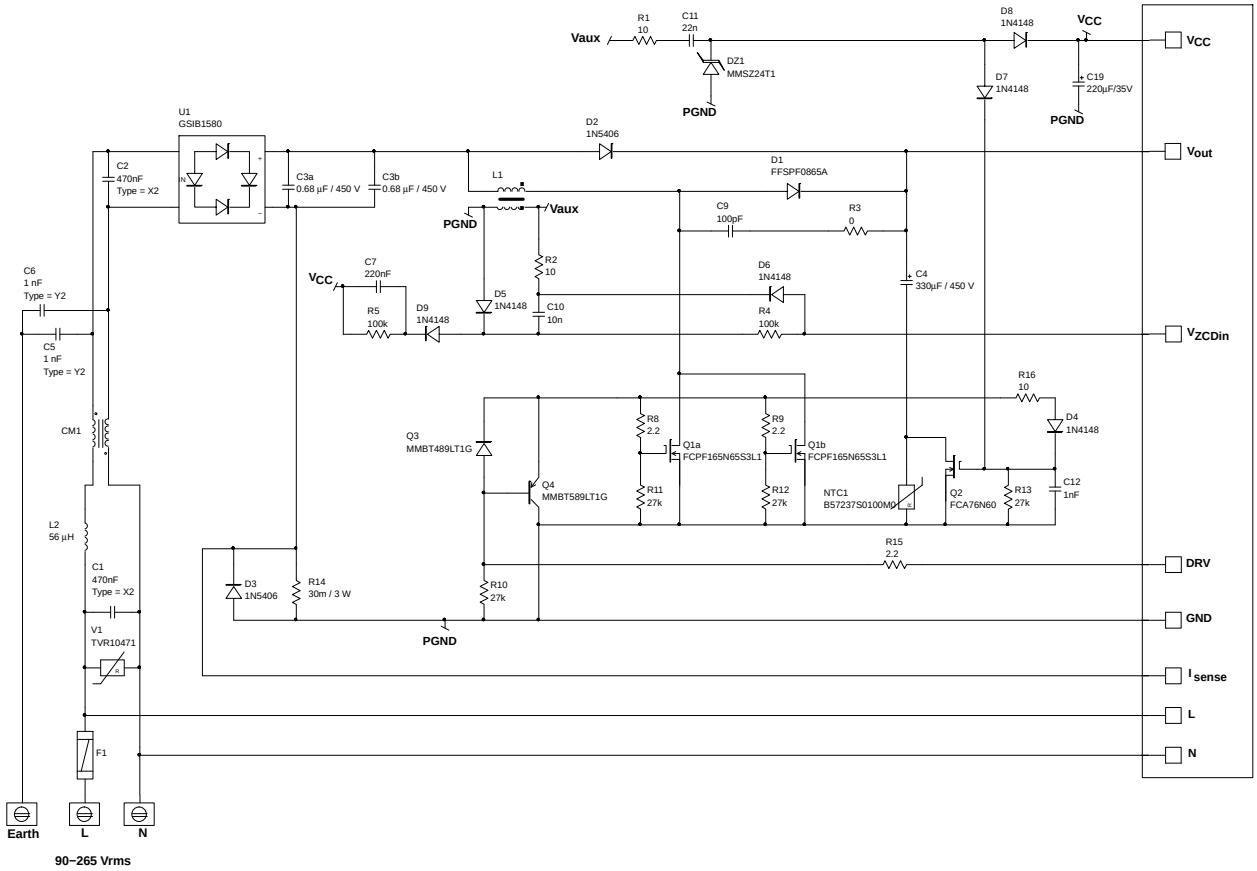


Figure 2. Power Section of the Application Schematic

Figure 2 shows the power section of the application schematic. Charge pump (R_1, C_{11}, D_{Z1}) provides the V_{CC} voltage using an auxiliary winding of the PFC choke. Two ON Semiconductor FCPF165N65 MOSFETS (Q_{1a} and Q_{1b}) are paralleled [2]. A Silicon Carbide Schottky diode (SiC) FFSPF0865A from ON Semiconductor is used as the boost diode [3]. An NTC is placed in series with the bulk capacitor C_4 to limit inrush currents when the PFC stage is plugged in. MOSFET Q_2 (FCA76N60 − 600 V, 36 mΩ, TO−3P MOSFET from ON Semiconductor [4]) is implemented to bypass the NTC when the bulk capacitor is charged. Practically, the drive voltage and a V_{CC} charge pump output are applied to Q_2 gate so that Q_2 is on and the NTC bypassed as soon as the PFC stage is in operation. The evaluation board supports the use of a totem pole (Q_3, Q_4) to shorten the MOSFET transitions. However, if the pnp transistor (Q_4) is implemented to speed−up the turning off event, in this application, npn transistor Q_3 is not used (only its base−emitter junction is used as a diode for turning on current).

Control Section

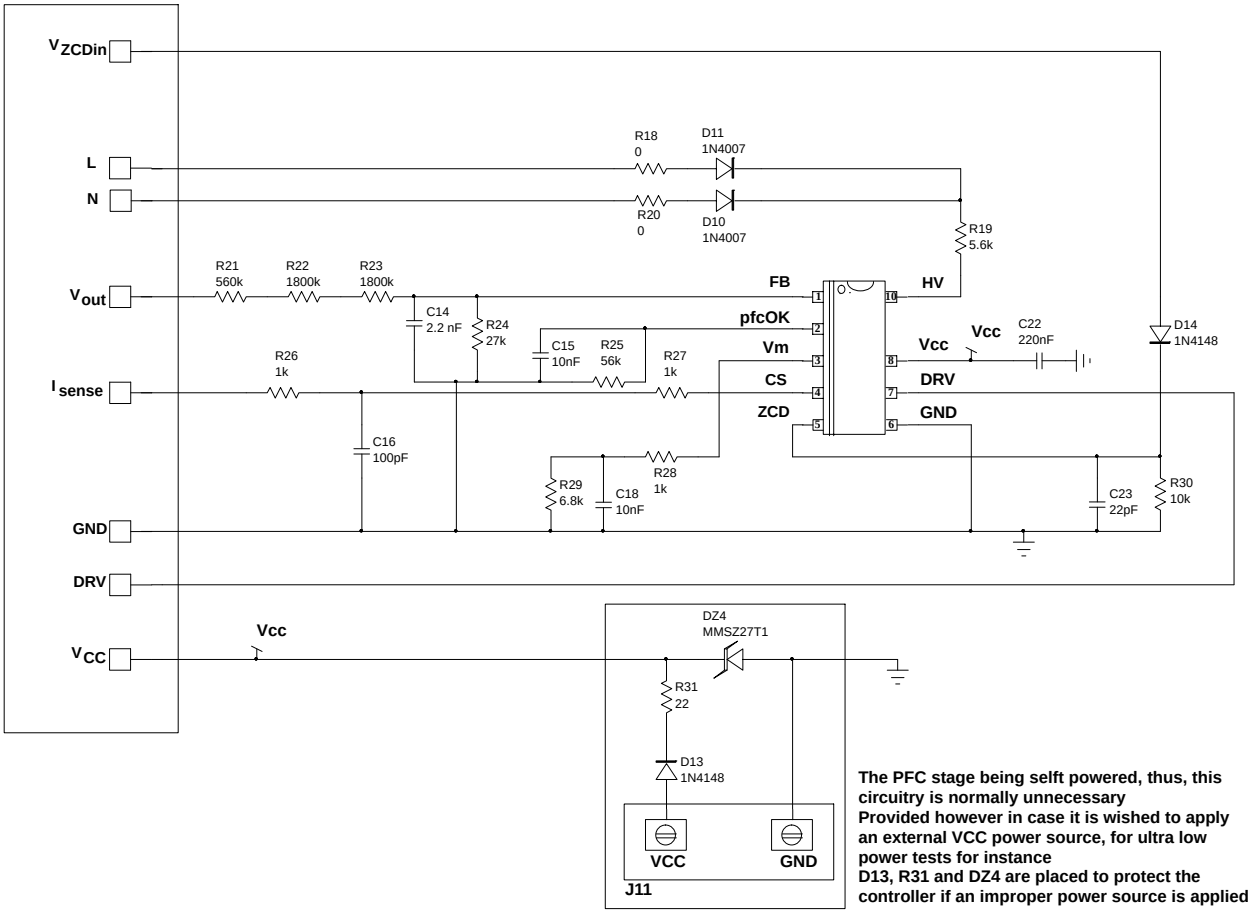


Figure 3. Control Section of the Application Schematic

Pin 5 of the NCP1618 is designed to monitor a signal from an auxiliary winding for detecting the core reset when this voltage drops to zero. This function ensures valley turn on in discontinuous and critical conduction modes (DCM and CrM). This pin can also be used to detect an over−voltage condition of the bulk voltage, hence offering a redundant OVP protection (OVP2). However, as detailed in [5] direct sensing of the bulk voltage for OVP2 may cause too much a power dissipation when an ultra−low standby consumption is targeted. That is why this board instead uses the auxiliary winding voltage to reconstruct a voltage representative of the bulk voltage. More specifically, charge pump R_2, C_{10} and D_5 of Figure 2 provides a signal representative of the drain−source voltage of the MOSFET ($N*V_{DS}$), where N is the turns ratio (auxiliary winding number of turns / primary winding number of turns). This voltage biases the ZCD circuitry and as it is equal to ($N*V_{BULK}$) during the demagnetization phase, it is sensed for OVP2. Components R_5, C_7 and D_9 clamps reconstructed ($N*V_{DS}$) signal to prevent that when the circuit starts or restarts operation after an interruption, an incorrect initial value of the C_{10} voltage causes OVP2 spurious tripping. See [5] for more details.

Circuitry for Soft−SKIP Testing

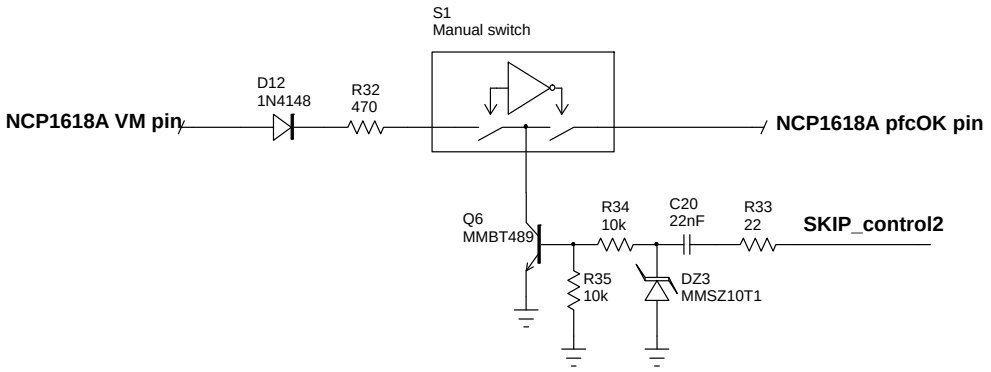


Figure 4. Circuitry for Soft−SKIP Mode Testing

The NCP1618A is designed to enter the soft−SKIP mode at very light load. Soft−SKIP minimizes losses by forcing a very low frequency burst−mode of operation. First, the circuit charges the output voltage to 103% of its nominal voltage and at that moment, enters a deep idle mode where no DRV pulses are generated and all non−necessary circuitries are turned off so that the circuit consumption is reduced to a minimum (250 μA typically). The circuit wakes up and restarts a new active burst cycle when the output voltage has dropped to 98% of its nominal level. In other words, as illustrated by Figure 17a, the output voltage swings between 103% and 98% of its nominal value. The NCP1618A can be externally forced to enter the soft−SKIP mode by grounding the V_M pin or applying negative pulses on the pfcOK pin (refer to [1] for more details). In the absence of a downstream converter, the circuit of Figure 4 can be used to provide the soft−SKIP signal. A square−wave signal varying between about 0 and an upper voltage of 5 to 15 V should be applied to the SKIP_control2 input of the board. According to the position of manual switch S_1, either the V_M or the pfcOK pin will be used for controlling the soft−SKIP mode.

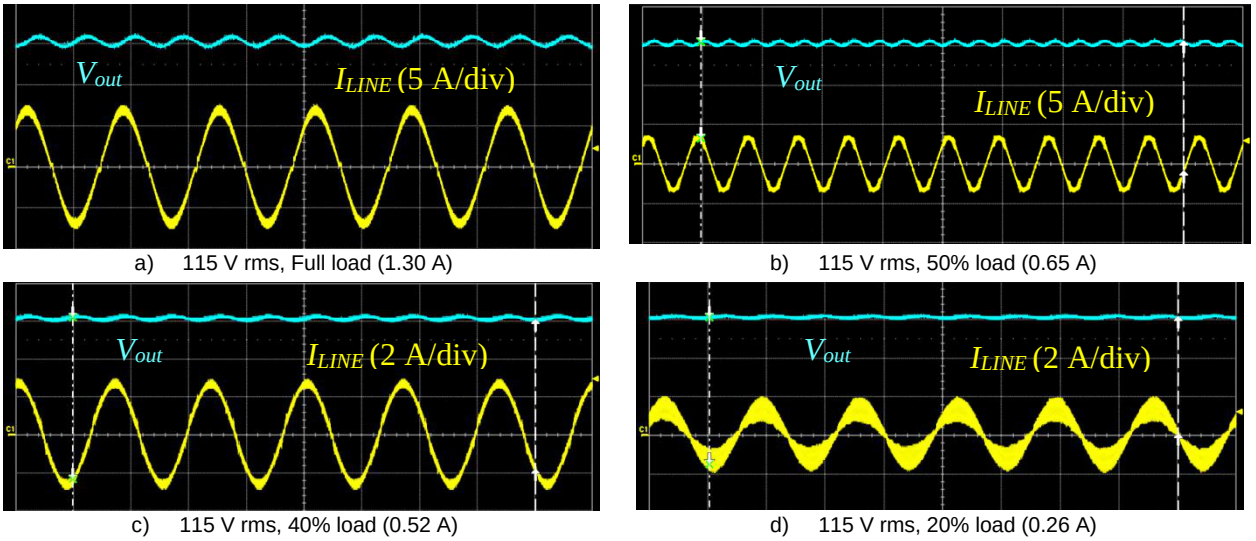
Important Remark:

Proposed circuitry was designed to illustrate the NCP1618 operation. It should not be re−used in practical applications as is unless appropriate verifications are made to check that it can meet reliability and safety requirements and comply with relevant norms. In particular, the inrush management circuitry may not be re−used if risks exist that the NTC is not properly shorted when the PFC stage starts switching. If the NTC is not shorted, the V_{OUT} voltage will be the sum of the bulk capacitor voltage plus the voltage produced by the inductor current across the NTC ($V_{C4} + (R_{NTC} * I_L)$) and in this case, too high a ($R_{NTC} * I_L$) voltage can be destructive for the application. It must be also noted that the inrush management circuitry increases the current loop when the boost stage fuels the bulk capacitor, making the layout less optimal for very high−speed switching operation, particularly with high t_{RR} boost diodes.

TYPICAL WAVEFORMS

Figure 5 shows the line current at 115 V rms and at below different load levels:

- At full load, the NCP1618 operates in CCM.
- At 50% of the load, the system operates in critical conduction mode
- At 40% of the load, the 130 kHz frequency clamp starts to trip (Frequency−clamped critical conduction mode) leading to critical conduction mode operation at the top of the sinusoid and valley−2 operation near the line zero crossing as illustrated by Figure 6.
- At 20% load, the NCP1618 frequency foldback makes the PFC stage operate at nearly 30 kHz. Note that the circuit continues turning on at the valley and that the number of valleys depends on the line instantaneous voltage. For instance, the number of skipped valleys is high at the top of the sinusoid where the resonant period is short while turn on in the second valley is obtained at the line zero crossing where the resonant period is long. See Figure 7. However, the NCP1618 always turns on at the valley as long as valleys are detectable.



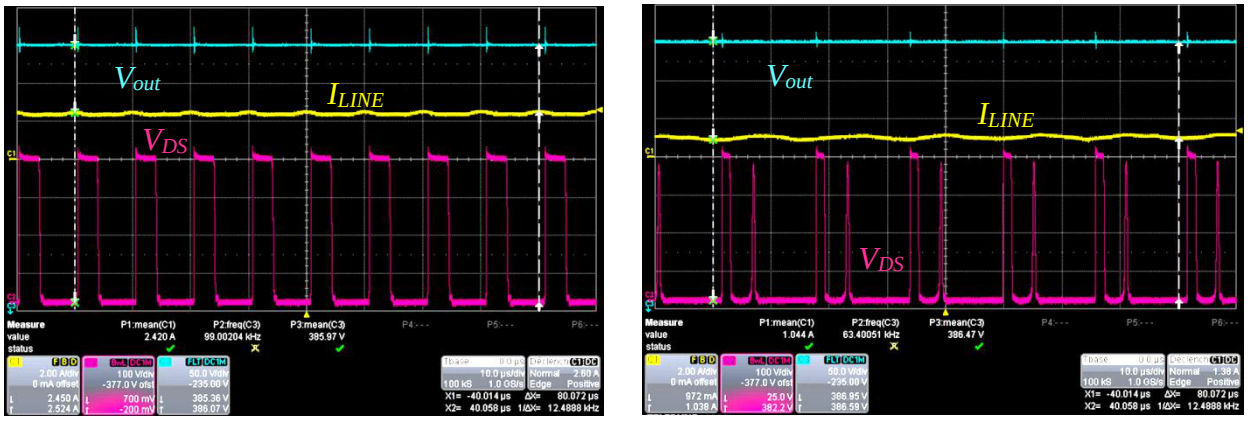
a) 115 V rms, Full load (1.30 A)

b) 115 V rms, 50% load (0.65 A)

c) 115 V rms, 40% load (0.52 A)

d) 115 V rms, 20% load (0.26 A)

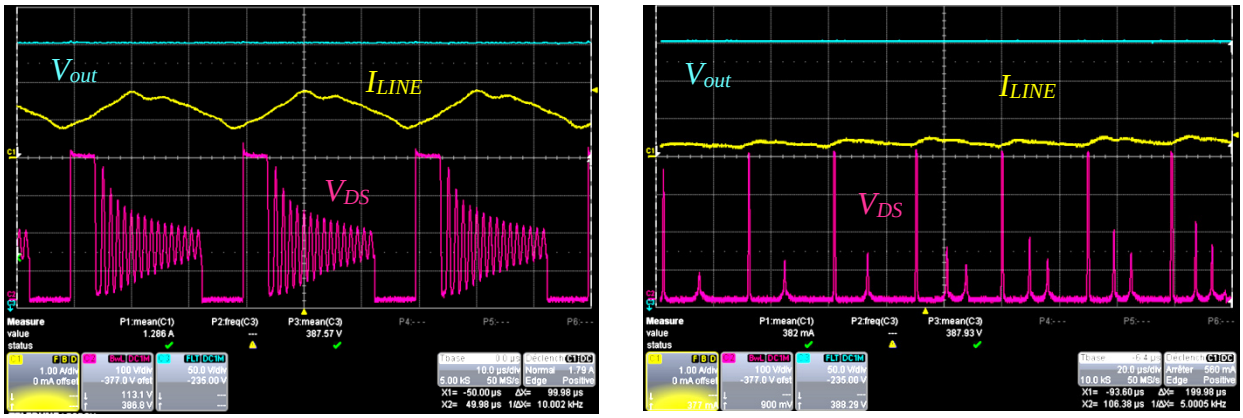
Figure 5. Line Current at 115 V rms



a) Top of the sinusoid

b) Near the line zero crossing

Figure 6. Operation at 115 V rms, 40% Load



a) Top of the sinusoid

b) Near the line zero crossing

Figure 7. Low Frequency Operation at 115 V rms, 20% Load

CCM Operation

The transition point is measured by increasing /decreasing the load by 1 mA steps.

Line rms voltage	Load current for exiting CCM	Load current for entering CCM
90 V	524 mA	610 mA
115 V	779 mA	893 mA
150 V	1034 mA	1205 mA
180 V	1133 mA	1460 mA
230 V	888 mA	1021 mA
265 V	798 mA	922 mA

Board Performance

- Efficiency

The efficiency is measured on an automated bench at 90 V rms, 115 V rms, 230 V rms and 265 V rms. After a 30−mn warm−up time at full load, the load is decreased from 1.30 A down to 0.13 A by 0.13−A steps. The measure is made after 5 mn of operation at the operating point under test.

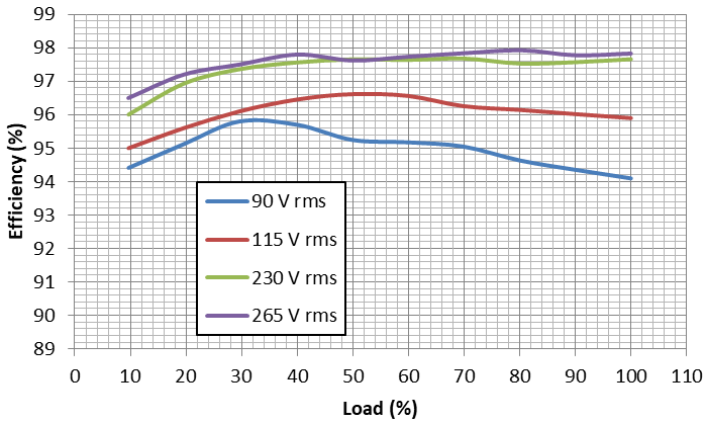
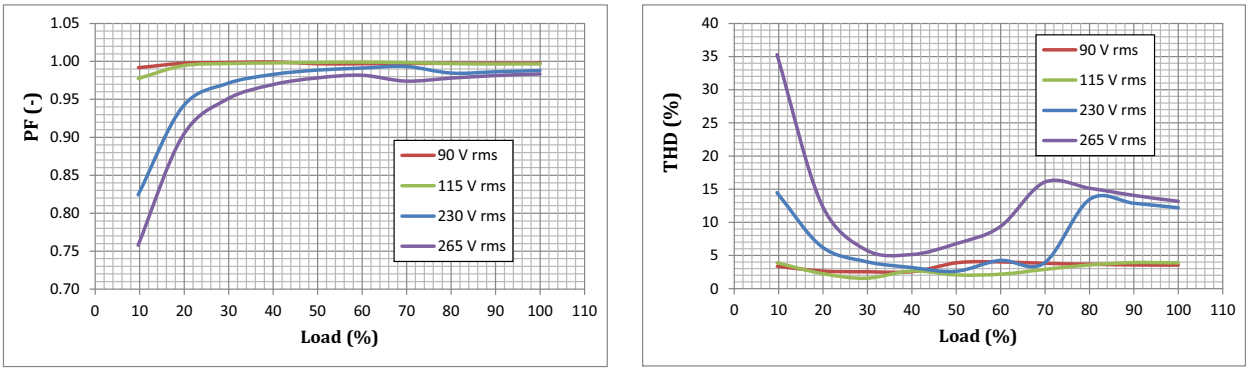


Figure 8. Efficiency vs. Load

The efficiency remains above 94% from 10% to 100% of the load at the 4 tested line levels (90 V rms, 115 V rms, 230 V rms and 265 V rms).

- Power Factor and THD

Power factor and THD are measured over the load range. Practically, the load current is swept starting from 1300 mA to 130 mA with 130 mA steps.



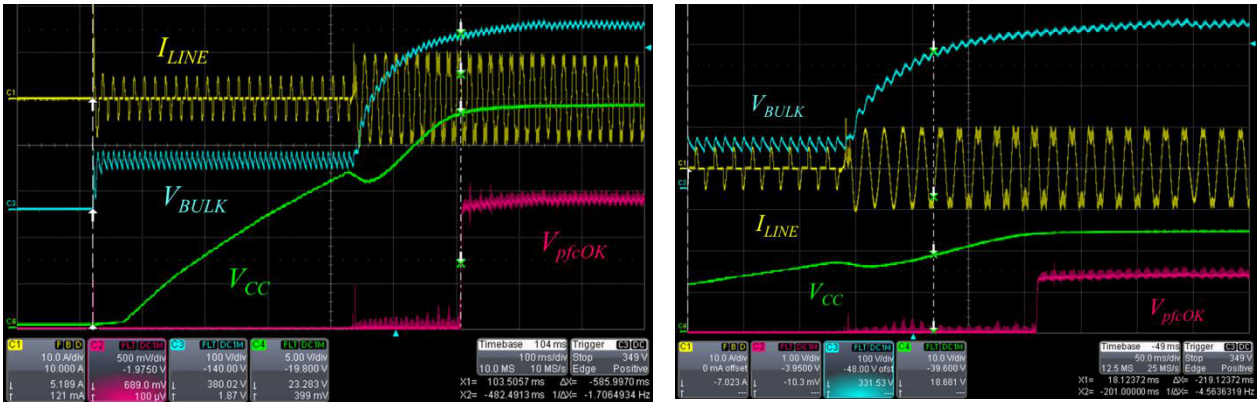
a) Power factor (PF) b) Total harmonic distortion (THD)

Figure 9. PF and THD versus Load

On the 20% to 100% load range, the power factor remains higher than 0.9 and the THD well below 20% at the four tested line levels.

Startup Sequences

When the board is plugged in, the circuit first turns on the internal high−voltage start−up current source to charge up the V_{CC} capacitor. When V_{CC} reaches $V_{CC(on)}$ (17 V typically), operation can begin and the PFC stage starts to deliver energy. When the bulk capacitor is charged to 98% of its nominal voltage, the pfcOK pin turns high to enable the downstream converter. As indicated in the data sheet, a 100 μF V_{CC} capacitor is typically charged from 0 to $V_{CC(on)}$ in about 215 ms. The total V_{CC} capacitance of our board being 220 μF, we can hence expect the PFC stage to start about 470 ms after it is plugged in.

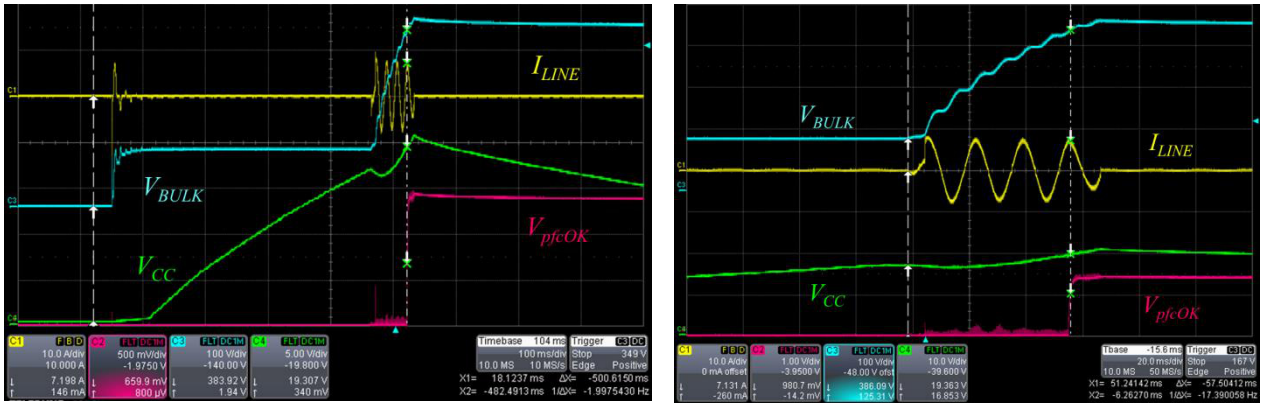


a) General view b) Magnified view

Figure 10. Startup Sequence at Full Load, Low Line

Figure 10 shows a start−up sequence done at full load (1.3 A) and at the lowest line level (90 V), the V_{CC} capacitor being discharged when the board is plugged in. As illustrated by Figure 10a, the total time necessary to have pfcOK high from PFC stage plug−in is nearly 590 ms (about 420 ms to raise V_{CC} and 170 ms to charge the output capacitor). Magnified view of Figure 10b shows that it takes less than a line cycle to reach the full input current capability.

Note that two rising slopes can be seen on the plot of Figure 10a during the V_{CC} charge phase. This is because the NCP1618 startup current is limited to 1 mA (typically) until the V_{CC} voltage exceeds about 0.8 V. This feature prevents the internal high−voltage current source from overheating if the V_{CC} pin happens to be accidentally grounded. When this first sequence is completed, the NCP1618 sources the nominal charge current of 12 mA typically.



a) General view b) Magnified view

Figure 11. Startup Sequence at No Load, Low Line (90 V rms)

However, **in normal operation, the PFC stage starts up with no load** since the downstream converter is normally disabled until pfcOK gets high. Figure 11a shows that in this practical condition, the total start−up time is significantly less than 500 ms: the V_{CC} still takes about 420 ms and the bulk capacitor is charged within 60 ms.

TYPICAL BEHAVIOR AND WAVEFORMS

Abrupt Line Variations

The circuit detects the line range. Practically, the high−line mode is set when the HV pin voltage exceeds 236 V (typically) and recovers the low−line mode when the HV pin voltage remains less than 222 V for more than 25 ms (typical values). More practically, these voltage levels corresponds to line rms values of 167 V and 157 V respectively.

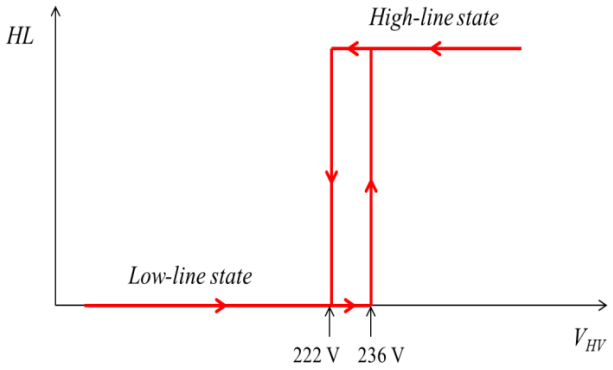


Figure 12. High−line Detection

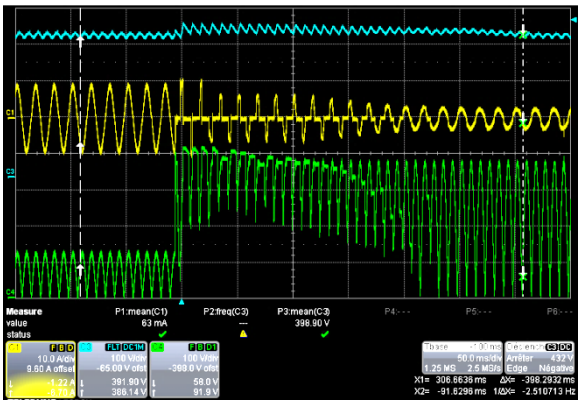


Figure 13. 90 V rms to 265 V rms Line Step at Full Load

The line range detection circuit optimizes the operation for universal (wide input mains) applications. Practically, in “high−line”:

- The regulation bandwidth is divided by 4
- The power expression defining the threshold below which frequency foldback is engaged is changed (see data sheet [1]).

Figure 13 shows a low− to high−line transition at full load (I_{out} = 1.3 A). This abrupt line change causes a voltage increase well−contained by the over−voltage protection. Figure 14 details a high− to low−line transition at full load. The circuit moderately reacts to the abrupt line change during the 25 ms necessary for low−line detection. After this delay, the NCP1618 sharply reacts and effectively limits the output voltage decay. Practically, the output voltage remains above 320 V.

a) General view b) Magnified view

Figure 14. 265 V rms to 90 V rms Line Drop at Full Load

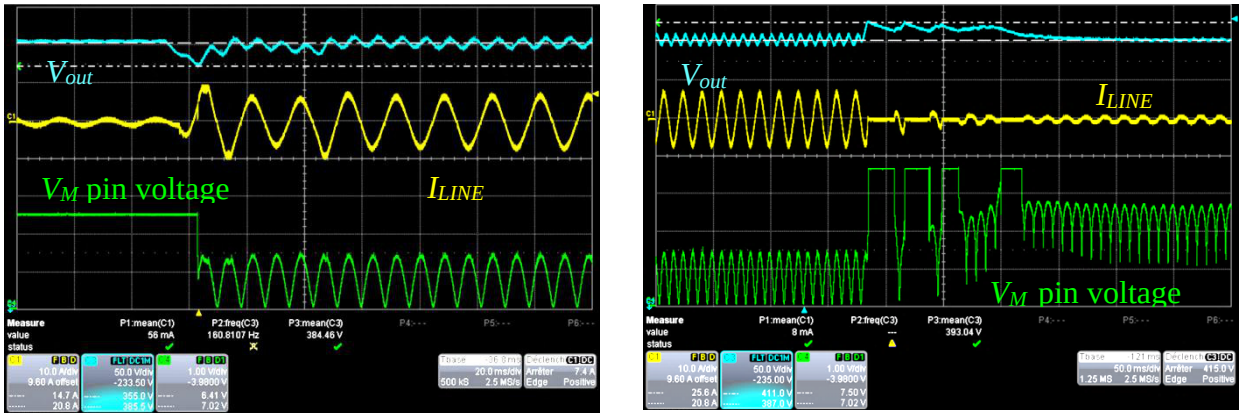
Load Steps

In essence, PFC stages are slow systems. Thus, the output voltage of PFC stages may exhibit excessive over− and under−shoots because of abrupt load or input voltage variations (e.g. at start−up). The NCP1618 incorporates a fast line / load compensation to avoid such large output voltage variations. Practically, the circuit monitors the output voltage and limits possible deviations with respect to the regulation nominal voltage ($V_{out,nom}$). More specifically, the NCP1618:

- Disables the drive to stop delivering power when the output voltage exceeds the over voltage protection level (105% of $V_{out,nom}$) and until V_{out} has decayed back to 103% of $V_{out,nom}$ (typical values).
- Drastically speeds−up the regulation loop (Dynamic Response Enhancer) when the output voltage goes below 95.5 % of $V_{out,nom}$.

To illustrate these functions, every 500 ms, the load is abruptly changed from 0.13 A to 1.30 A (respectively 10% and 100% of the full load) and vice versa, with 2 A/µs edges.

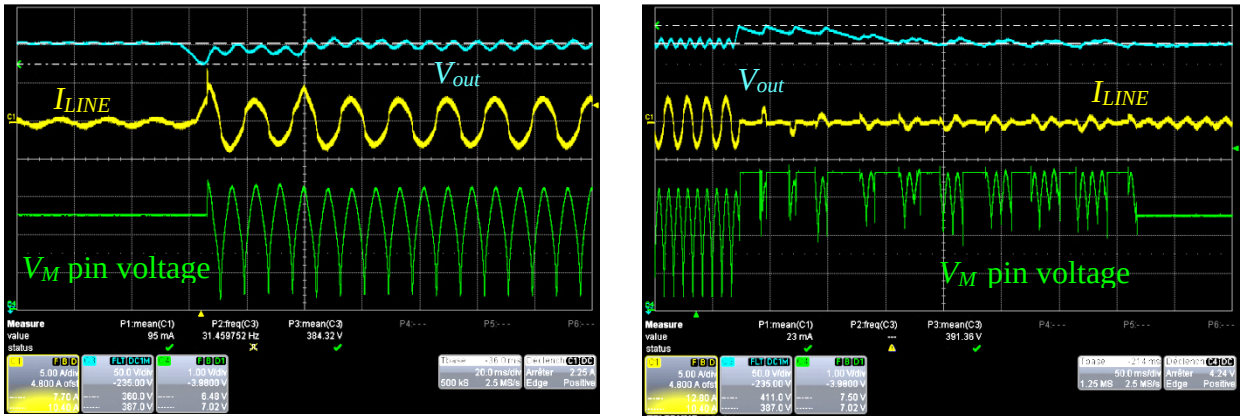
Figure 15 shows the resulting output voltage under the load changes at 115 V rms. We can see that the NCP1618 is able to maintain the output voltage above 350 V when the load is abruptly raised from 10% to 100% (Figure 15a) and below about 410 V when the load is suddenly 90% reduced (Figure 15b).



a) Rising load step b) Falling load step

Figure 15. 10% to 100% Load Steps at 115 V rms

The same test is made at 230 V rms. Again as illustrated by Figure 16, the output voltage remains within a narrow range (between about 360 and 411 V).



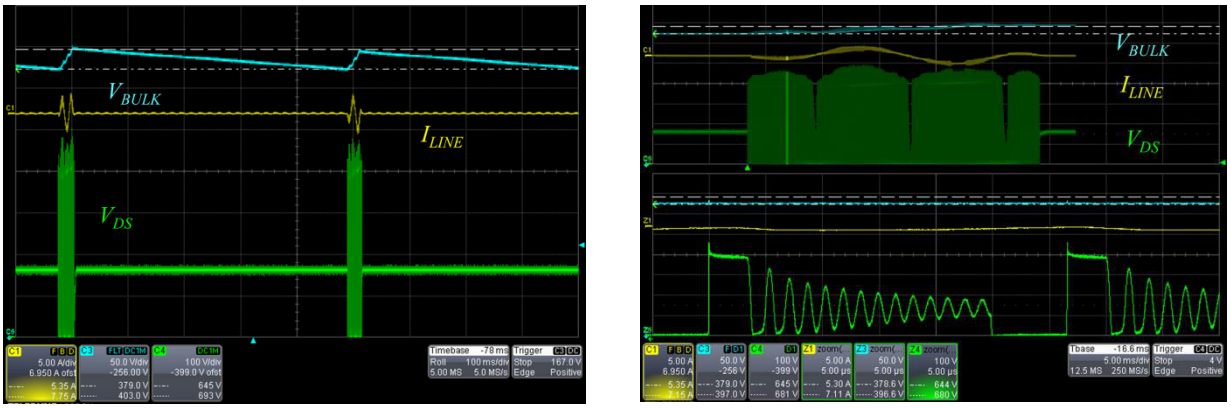
a) Rising load step b) Falling load step

Figure 16. 10% to 100% Load Steps at 230 V rms

The V_M pin voltage is shown in Figure 15 and Figure 16 as it is indicative of the operation mode. It is a constant dc voltage in FCCrM mode (2.50 V) and during an operation interruption caused by the over−voltage protection (3.75 V) while the V_M pin voltage is a rectified sine−wave in CCM.

Soft−SKIP Mode

The NCP1618 is designed to be externally forced to enter the soft−SKIP mode by grounding the V_M pin or applying negative pulses on the pfcOK pin. When in soft−SKIP mode, the circuit charges the output voltage to 103% of its nominal voltage and at that moment, enters a deep idle mode where no DRV pulses are generated and all non−necessary circuitries are turned off so that the circuit consumption is reduced to a minimum (250 μA typically). The circuit wakes up when the output voltage has decayed down to 98% of its nominal level and restarts a new active burst cycle. In other words, as illustrated by Figure 17a, the output voltage swings between 103% and 98% of its nominal value. Magnified view of Figure 17b shows the active part of the burst. It illustrates that for best efficiency, the PFC stage operates at low frequency with valley switching.



a) General view b) Magnified view

Figure 17. Soft−Skip Operation (115 V, 1% Load)

Line−Sag Tests

Tests can be made which consist of rapidly and repeatedly plug and unplug the power supply. If no specific function is implemented, a huge current can take place when the power supply is reconnected.

The NCP1618 detects short drops/interruptions of the mains to prevent an excessive stress when the line recovers. Practically, such line−sag situations are detected when the input voltage remains below 100 V for 25 ms or more (typical values) and in such cases, CCM mode is disabled and a soft−stop sequence starts. Soft stop is the gradual down−to−zero discharge of the control signal to smoothly stop operation.

When the line recovers, the circuit resets the BUV timer. It is because a line−sag event is likely to cause a BUV (bulk under−voltage) detection. When a BUV fault is detected, no restart is normally possible until the BUV timer (500 ms typically) has elapsed. However, if the BUV protection trips during a line−sag sequence, operation resumes as soon as the line recovers. Also, the NCP1618 interrupts the soft−stop discharge, grounds the control signal and charges V_{CC} to its startup level ($V_{CC(on)}$ = 17 V) if below for a clean start−up [1].

a) 20 −ms line sag (115 V rms, full load)

b) 50 −ms line sag (115 V rms, full load)

Figure 18. Line Short Drops to 50 V rms

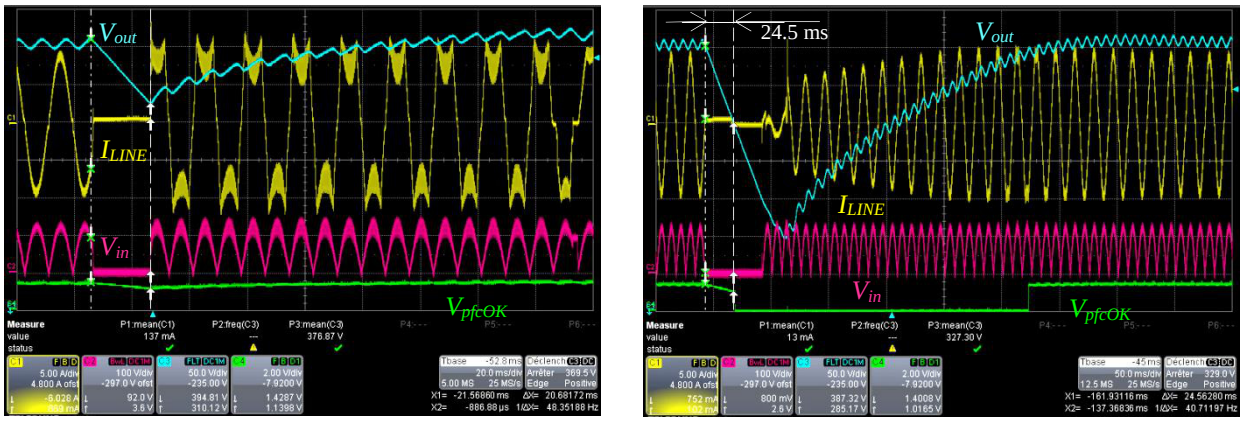
Figure 18a shows the case of a very short line sag (20 ms) while the circuit is operating at 115 V rms, full load. It is too short to trip the line−sag protection. Figure 18b shows a longer line sag situation (50 ms). In this case, we can see that after 25 ms, soft−stop is engaged and that after 37.5 ms, the BUV protection trips as attested by the pfcOK grounding. Operation resumes as soon as the line is back without waiting for the BUV timer being elapsed.

Hold−Up Time

Hold−up time tests are made at 90 V, full load. In the Figure 19a case, the line is interrupted for 20 ms. In this situation, the output voltage drops to 310 V which is well above the bulk under−voltage level ($V_{out,BUV}$ = 280 V). In turn, pfcOK remains high and keeps enabling the downstream converter which loads the PFC stage.

In the Figure 19b case, the line interruption is extended to 50 ms (test still made at 90 V, full load). This test enables to confirm the BUV level (about 280 V) which is reached after about the first 24 ms of line absence. This is the moment when due to the bulk under−voltage tripping (BUV), the pfcOK pin is grounded to disable the downstream converter.

The two plots of Figure 19 also show that when the output voltage decays, so does the pfcOK voltage (when it is not grounded). Actually, when in high state, the pfcOK voltage is proportional to the output voltage to provide the downstream converter not only with an enable/disable signal but also with a signal representative of the output voltage for feedforward.



a) 20 −ms line interruption (90 V, full load)

b) 50 −ms line interruption (90 V, full load)

Figure 19. Mains Interruptions

BILL OF MATERIAL

BILL OF MATERIAL

Reference	Qty	Description	Value	Tolerance / Constraints	Footprint	Manufacturer	Part number	Substitution allowed
Power Section								
J10	1	AC Connector	GSF1.1xx x.xx			SCHURTER	GSF1.1201.31	NO
	1	Fuse	8 A / 250 V			SCHURTER	34562611	NO
J1b	1	VBULK connector				Multicomp	24.243.1	NO
J1a	1	GND connector				Multicomp	24.243.2	NO
HS1	1	Diodes Bridge (U1) Heatsink	4.5°C/W			Fischer Elektronik	SK481−50	NO
HS2	1	Q1a, Q1b and D1 Heatsink	2.8°C/W			Fischer Elektronik	SK481−100	NO
	4	HS1 and HS2 Heatsink clip				Fischer Elektronik	THFU1	NO
C1, C2	2	X2 capacitor	470 nF	277V	through−hole	Wurth Elektronik	890334025039CS	NO
C3a, C3b	2	Filtering capacitor	680 nF	450V	through−hole	Wurth Elektronik	890283425008CS	NO
C4	1	Electrolytic capacitor	330 μF	450 V	through−hole	Wurth Elektronik	861141486022	NO
C5, C6	2	Y2 capacitors (note)	1 nF	275 V	through−hole	EPCOS	B32021A3102	NO
C7	1	Ceramic capacitor	220 nF	25V, 10%	SMD, 1206	various	various	YES
C9	1	High−voltage capacitor	100 pF	500 V	through−hole	Vishay	D101K20Y5PL6.J5 .	NO
C10, C11	2	Capacitor	10 nF	25V, 10%	SMD, 1206	various	various	YES
C12	1	Capacitor	1 nF	25V, 10%	SMD, 1206	various	various	YES
C19	1	Electrolytic Capacitor	220 μF	35 V	through−hole	Wurth Elektronik	860020273009	YES
U1	1	Diodes Bridge	GSIB1580	15A, 800V	through−hole	VISHAY	GSIB1580	NO
CM1	1	Common−Mode Filter	2 mH	6 mΩ	through−hole	Wurth Elektronik	7448031002	NO
D1	1	Boost diode	FFSPF0865A	8A, 650V	TO220F	ON Semiconductor	FFSPF0865A	NO
D2, D3	2	Bypass diode	1N5406	3A, 600 V	Axial	ON Semiconductor	1N5406G	NO
D4, D5, D6, D7, D8, D9	6	Switching diode	D1N4148	100 V	SOD123	Vishay	1N4148W−V	NO
DZ1	1	24−V zener diode	MMSZ24T1	24V, 0.5W	SOD−123	ON Semiconductor	MMSZ24T1G	NO
L1	1	Boost Inductor	175 μH, 14 A		PQ3230	Wurth Elektronik	750 317557	NO
L2	1	DM Choke	56 μH	17 mΩ	through−hole	BOURNS	2310−V−RC	NO
Q1a, Q1b	2	Power MOSFET	FCFP165N65	650V	TO220F	ON Semiconductor	FCPF165N65S3L1	NO
Q2	1	Power MOSFET	FCA76N60	600 V, 76 A	TO−3PN	ON Semiconductor	FCA76N60N	NO
Q3	1	NPN transistor	MMBT489LT1G	40 V / 1 A	SOT−23	ON Semiconductor	MMBT489LT1G	NO
Q4	1	PNP transistor	MMBT589LT1G	30V / 2A	SOT−23	ON Semiconductor	MMBT589LT1G	NO
NTC1	1	Inrush Current Limiter	10 Ω @ 25°C		through−hole	EPCOS	B57237S0100M0	NO
R1, R2, R16	3	SMD resistor, 1206, 1/4W	10 Ω	10%, 1/4W	SMD, 1206	various	various	YES
R3	1	Through hole resistor	0 Ω	1 W	through−hole	Vishay	AC01	
R4, R5	2	SMD resistor, 1206, 1/4W	100 kΩ	10%, 1/4W	SMD, 1206	various	various	YES
R8, R9, R15	3	SMD resistor, 1206, 1/4W	2.2 Ω	10%, 1/4W	SMD, 1206	various	various	YES

BILL OF MATERIAL (continued)

Reference	Qty	Description	Value	Tolerance / Constraints	Footprint	Manufacturer	Part number	Substitution allowed
R10, R11, R12, R13	4	SMD resistor, 1206, 1/4W	27 kΩ	10%, 1/4W	SMD, 1206	various	various	YES
R14	1	Current sense resistor	30 mΩ	1%, 3W	through−hole	Vishay	LVR03R0300FE12	NO
V1	1	TVS Varistor		275 V rms		Wurth Elektronik	820513011	NO
Control Section and Circuitry for Soft−SKIP Testing								
R18, R20	1	SMD resistor, 1206, 1/4W	0 kΩ	1%	SMD, 1206	various	various	YES
R19	1	SMD resistor, 1206, 1/4W	5.6 kΩ	1%	SMD, 1206	various	various	YES
R21	1	SMD resistor, 1206, 1/4W	560 kΩ	1%	SMD, 1206	various	various	YES
R22, R23	2	SMD resistor, 1206, 1/4W	1800 kΩ	1%	SMD, 1206	various	various	YES
R24	1	SMD resistor, 1206, 1/4W	27 kΩ	1%	SMD, 1206	various	various	YES
R25	1	SMD resistor, 1206, 1/4W	56 kΩ	1%	SMD, 1206	Vishay	various	YES
R26, R27, R28	3	SMD resistor, 1206, 1/4W	1 kΩ	1%	SMD, 1206	Vishay	various	YES
R29	1	SMD resistor, 1206, 1/4W	6.8 kΩ	1%	SMD, 1206	Vishay	various	YES
R30, R34, R35	3	SMD resistor, 1206, 1/4W	10 kΩ	1%	SMD, 1206	Vishay	various	YES
R31, R33	2	SMD resistor, 1206, 1/4W	22 Ω	1%	SMD, 1206	Vishay	various	YES
R32	1	SMD resistor, 1206, 1/4W	470 Ω	1%	SMD, 1206	Vishay	various	YES
D10, D11	2	Standard Recovery Diodes	1N4007	1000 V	through−hole	ON Semiconductor	1N4007G	NO
D12, D13, D14	3	Switching diode	D1N4148	100 V	SOD123	Vishay	1N4148W−V	NO
DZ3	1	10−V zener diode	MMSZ10 T1	10 V, 0.5 W	SOD−123	ON Semiconductor	MMSZ10T1G	NO
DZ4	1	27−V zener diode	MMSZ27 T1	27 V, 0.5 W	SOD−123	ON Semiconductor	MMSZ27T1G	NO
C14	1	Capacitor	2.2 nF	25 V, 10%	SMD, 1206	various	various	YES
C15, C18	1	Capacitor	10 nF	25 V, 10%	SMD, 1206	various	various	YES
C16	1	Capacitor	220 pF	25 V, 10%	SMD, 1206	various	various	YES
C20	1	Capacitor	22 nF	25 V, 10%	SMD, 1206	various	various	YES
C22	1	Capacitor	220 nF	25 V, 10%	SMD, 1206	various	various	YES
C23	1	Capacitor	22 pF	25 V, 10%	SMD, 1206	various	various	YES
Q6	1	NPN transistor	MMBT489 LT1G	40 V / 1 A	SOT−23	ON Semiconductor	MMBT489LT1G	NO
S1	1	Manual Switch	1K2serie		SW_sip3	EOZ secme	09−03290.01	NO
U2	1	controller	NCP1618		SOIC9	ON Semiconductor	NCP1618	NO
J11	1	Vcc socket				WEIDMULLER	PM5.08/2/90	YES

NOTE: All Components are Lead−Free

References

[1] NCP1618 data sheet: https://www.onsemi.com/pub/Collateral/NCP1618−D.PDF
[2] FCPF165N65 data sheet: https://www.onsemi.com/pub/Collateral/FCPF165N65S3L1−D.PDF
[3] FFSPF0865 data sheet: https://www.onsemi.com/pub/Collateral/FFSPF0865A−D.PDF
[4] FCA76N60 data sheet: https://www.onsemi.com/products/discretes−drivers/mosfets/fca76n60n
[5] Joel Turchi, “NCP1618 tips and tricks”, application note AND90011/D, https://www.onsemi.com/pub/Collateral/AND90011−D.PDF

ANNEX

The board provides some flexibility and consists of few components which are shorted or not connected. For the sake of clarity, below schematic diagrams report them together with implemented ones.

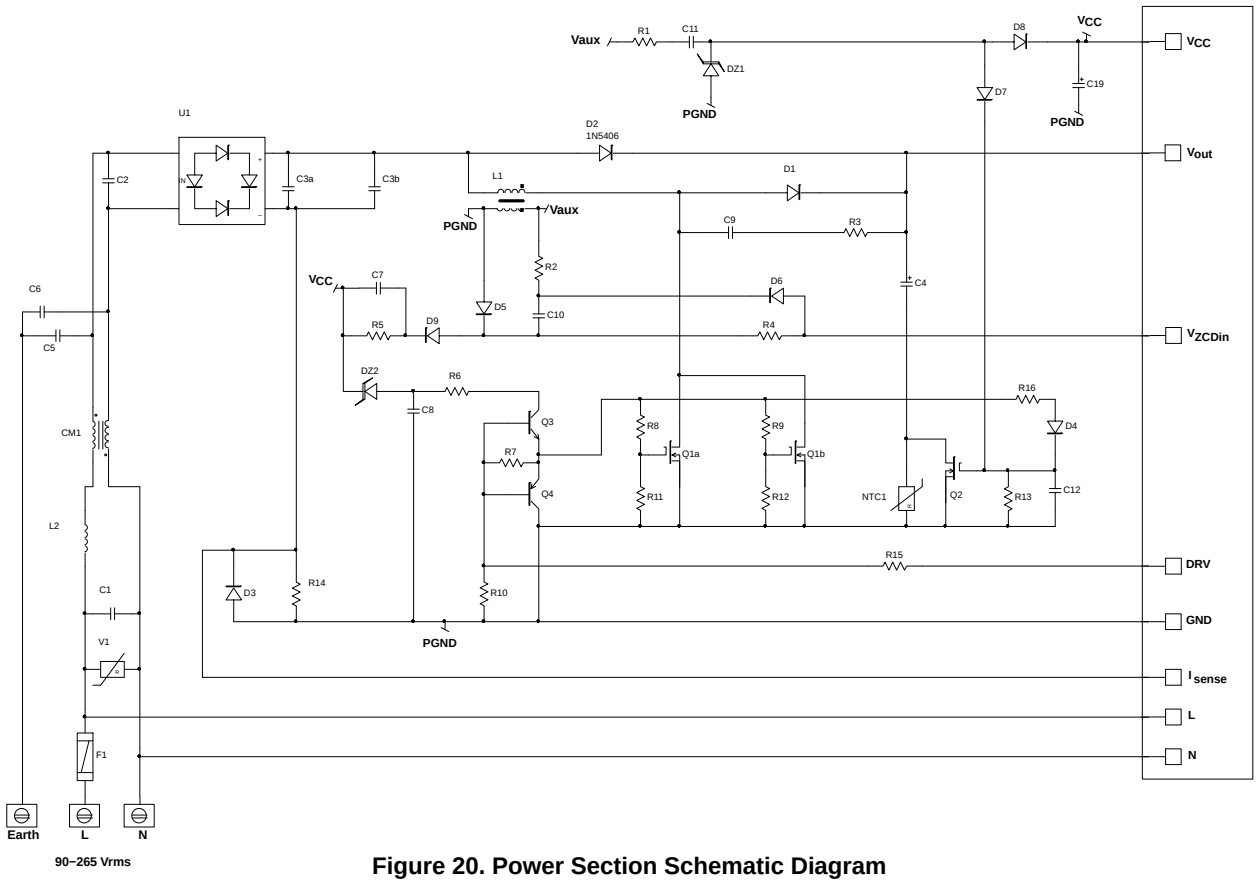


Figure 20. Power Section Schematic Diagram

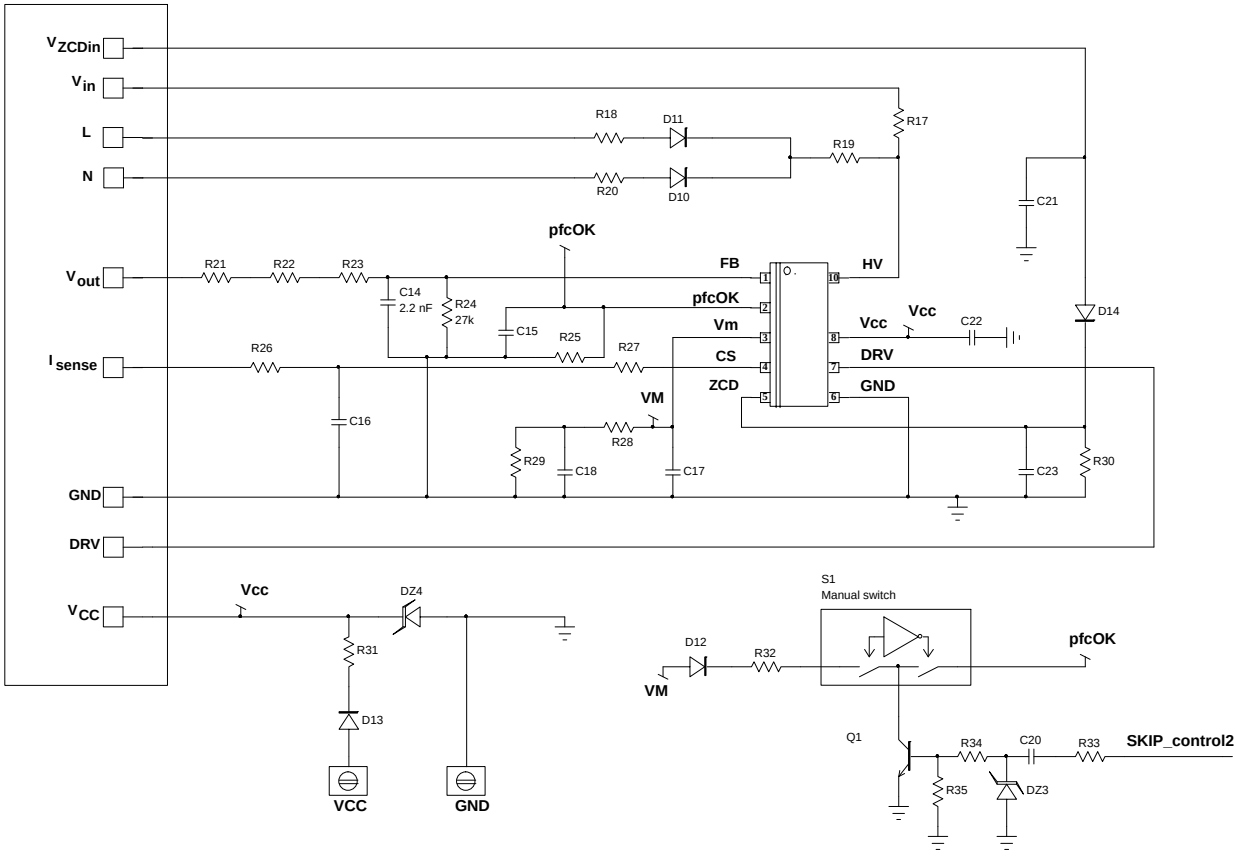


Figure 21. Control Section and Circuitry for Soft−SKIP Testing

ADDITIONAL INFORMATION

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