EVBUM2635/D

X-Cube Imaging System X-Cube HiSPi-to-MIPI Converter Board User's Manual

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EVAL BOARD USER'S MANUAL

Figure 1. HiSPi−to−MIPI Converter Board Shown Connected to the X−Cube XGS 12000 Imager Board and Installed in the C−Mount Lens Housing

HISPI−TO−MIPI CONVERTER BOARD OVERVIEW

The X−Cube Imaging System (X−Cube) is designed to demonstrate the features of ON Semiconductor's XGS family of image sensors in machine vision applications.

The X−Cube is designed to conform to the machine vision industry standard 29 mm × 29 mm form factor.

This HiSPi−to−MIPI Converter Board is designed to be compatible with the X−Cube Imaging System's family of XGS imager boards. The function of this HiSPi−to−MIPI Converter Board is to convert HiSPi Packetized−SP mode format image data output from an X−Cube XGS Imager Board to MIPI CSI−2 image data format. The XGS sensor image data in MIPI format can then be connected to a host via the output connector on the HiSPi−to−MIPI Converter Board.

For more information about the X−Cube, please refer to the X−Cube Imaging System Developer Guide. (AND9891/D)

FEATURES

- HiSPi−to−MIPI Convertion Process Implemented in a Lattice LIF−MD6000 FPGA
- HiSPi Packetized−SP Mode Image Data Input (12 Lane Implementation)
- MIPI CSI−2 Image Data Output (4 Lane Implementation)
- 26 mm × 26 mm PCB Sized to Fit the Machine Vision Industry Standard 29 mm × 29 mm Camera Case and Lens Mount
- Operates Off of a Single Power Supply Supplied by the Host
- A Host Controlled I^2C Interface is used to Configure and Operate the Imaging System

All of the PCB design files (schematic and PCB layout files) are available to customers (NDA is required) to enable and accelerate the design of a customized camera based on the XGS family of image sensors.

The file required to program the Lattice FPGA is provided in binary format (.bit file) and therefore no modifications to the FPGA code are possible. Customers can request support directly from Lattice if they wish to develop an alternative implementation of this FPGA code. Another option is for the customer to develop their own code to perform the function(s) they desire.

For information on how to obtain the design files for this board please contact the ON Semiconductor technical support team in your region.

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BLOCK DIAGRAM

The board block diagram is shown in Figure 2.

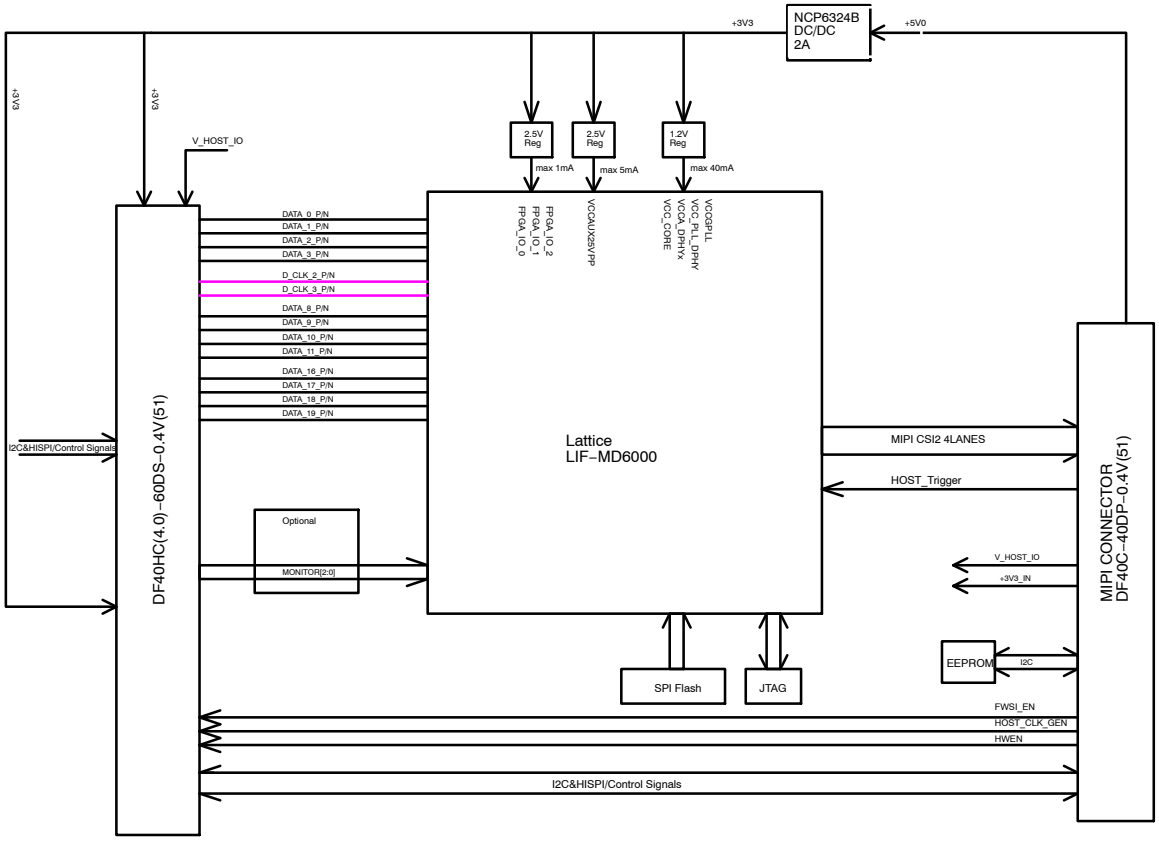
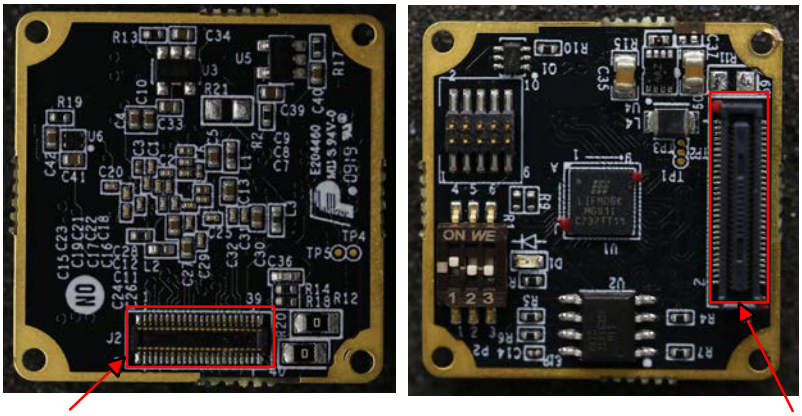


Figure 2. HiSPi−to−MIPI Converter Board Block Diagram

HISPI−TO−MIPI CONVERTER BOARD

The HiSPi−to−MIPI Converter Board is shown in Figure 3. The board is designed to be connected to an X−Cube compatible imager board. The board is sized to conform to the X−Cube Lens Mount Housing's form factor.



MIPI CSI−2 Mode Data Output Connector

HiSPi Packetized−SP Mode Data Input Connector

Figure 3. HiSPi−to−MIPI Converter Board: Top and Bottom View

Specification

The HiSPi−to−MIPI Converter Board requires only a single +5 V power supply input that is provided by the Host. The HiSPi−to−MIPI Converter Board utilizes on−board power regulators designed by ON Semiconductor to generate all of the power supplies voltages required by the FPGA from the single power supply provided by the Host. In addition, the HiSPi−to−MIPI Converter Board includes a LDO regulator to generate a +3.3 V power supply that can be used to power an X−Cube Imager Board when the boards are connected together. Please refer to the HiSPi−to−MIPI Converter Board schematic for detailed information on these circuits.

Upon power−up, the HiSPi−to−MIPI Converter Board will be initialized.

After initialization, the Lattice FPGA on the HiSPi−to−MIPI Converter Board can then begin to receive image data in HiSPi Packetized−SP Mode format from the X−Cube Imager Board. The FPGA will first buffer, and then re−order the incoming image data. The re−order process converts the incoming HiSPi formatted data to the MIPI CSI−2 four lane data format. The HiSPi−to−MIPI Converter Board then outputs the four lane MIPI data to the Host.

It is the Host's responsibility to then buffer the incoming MIPI data stream and to process this image data as desired (color interpolation etc..). The HiSPi−to−MIPI Converter Board can be connected to a number of X−Cube compatible Imager Boards. Note however, that the FPGA on the HiSPi−to−MIPI Converter Board requires unique firmware programming for each image sensor resolution.

Table 1. HISPI−TO−MIPI CONVERTER BOARD SPECIFICATIONS

Item	Definition	Min	Typ	Max	Unit
Input Image Data Format	**HiSPi Packetized – SP – SLVS mode**				
Number of HiSPi Lanes	Configurable via FPGA Firmware options	6	12	12	Lanes
Input Data Bitdepth	Configurable: 10−Bit Raw Data or 12−Bit Raw Data	10	12	12	Bits
Input Resolution	Configurable: Typical Resolution = 4176 H × 3102 V		12		Mpix
Output Image Data Format	**MIPI – CSI2 – 4 data lanes (one clock) D−Phy**				
Bandwidth	Per lane		1.5	1.5	Gbps
Output Resolution	4176 H × 3102 V		12		Mpix
Frame rate	At full resolution video input (4176 H × 3102 V)		21	41	fps
Power Supply					
VDD	Single power supply input to the HiSPi−to−MIPI Converter Board	+4.9	+5	+5.1	V
IDD	Total current load at max frame rate operation		400		mA
POWER	Power dissipation at max frame rate operation		2		W

REFERENCES

[1] AND9891/D (n.d.) X−Cube Imaging System X−Cube Machine Vision Reference Module Developer Guide.

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