

# NCP45491PMNGEVB

## NCP45491 Paired Mode Evaluation Board User's Manual



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### Introduction

This user's manual provides detailed information regarding the configuration and use of the NCP45491PMNGEVB evaluation board. The evaluation board serves as a demonstration of NCP45491 general functionality for *dual* mode chip mode featuring power monitoring of 6 channels. The evaluation board also provides a means of quick prototyping for specific applications.

### Features

- 2 NCP45491 Connected in Paired Mode
- Connectors for 6 High Current Loads and 3 Separate Bus Voltage Supplies
- Configuration Options for Shunt Current and Bus Voltage Gain Settings
- Appropriate Test Points for Easy Evaluation

### Quick Start

#### Recommended Equipment

Before beginning, the following equipment is needed:

- 4 DC Power Supplies (3.3 V VCC Supply, 12 V Bus Voltage, 6 V Bus Supply, 8 V Bus Supply)
- 6 DC loads (Up to at Least 2 A)
- 1 Function Generator
- 1 Oscilloscope
- 1 Digital Multi-meter
- SMA to BNC Cables Recommended for Connection to DIFF\_OUTN, DIFF\_OUTP, and MUX\_SEL

NOTE: Bus voltage supplies need to be capable of sourcing load currents times 2 since each supply sources 2 loads on the default setup.

### Board Setup

The assembled evaluation board targets Bus Voltages and Shunt Currents shown in Tables 1 and 2. VBUS1 ties to both channel 1 and channel 2 bus voltage inputs. VBUS2 ties to both channel 3 and channel 4 bus voltage inputs. VBUS3 ties to both channel 5 and channel 6 bus voltage inputs. Refer to the schematic and layout diagrams found in [Appendix A](#) and [Appendix B](#) respectively as needed.

## EVAL BOARD USER'S MANUAL

Table 1. BUS VOLTAGE SETUP

Channel	Target Bus Voltage	Bus Divider
1 (VBUS1)	12 V	1/60 V/V
2 (VBUS1)	12 V	1/60 V/V
3 (VBUS2)	6 V	1/30 V/V
4 (VBUS2)	6 V	1/30 V/V
5 (VBUS3)	8 V	1/40 V/V
6 (VBUS3)	8 V	1/40 V/V

Table 2. SHUNT CURRENT SETUP

Channel	Shunt Current Target	Shunt Gain Default Setting
Load 1	1 A	400 mV/A
Load 2	0.5 A	400 mV/A
Load 3	1 A	400 mV/A
Load 4	0.5 A	400 mV/A
Load 5	1 A	400 mV/A
Load 6	0.5 A	400 mV/A

The specific resistor configuration populated on the board facilitates these gain settings. The nominal differential amplifier gain is 2 V/V. Therefore, the expected differential output for any channels voltage or current can be calculated as follows:

- For Bus Voltage:  
Diff Output = Bus Voltage × Channel Bus Divider × 2
- For Load Current:  
Diff Output = Load Current × Channel Shunt Gain × 2

The output for each channel is calculated as follows:

$$\text{Diff Output} = \text{Bus Voltage} \times \frac{R4}{R4 + R3} \times 2 \quad (\text{eq. 1})$$

The channel shunt current gain is calculated as follows:

$$\text{Diff Output} = I_{\text{load}} \times \frac{R2 \times R_{\text{sense}}}{R1} \times 2 \quad (\text{eq. 2})$$

## NCP45491PMNGEV B

These gain settings can be adjusted by changing the bus divider resistors, and the shunt current network resistors as desired.

### Board Connections & Jumper Settings

The following board to bench equipment connections are required for demonstration of 6 channel power monitoring.

Make all board connections with supplies and loads disabled. Take adequate precautions when working with high current and high voltage applications. Table 3 below defines all default board connections and their purpose.

Table 4 below defines all default jumper connections and their purpose.

**Table 3. EVALUATION BOARD DEFAULT CONNECTIONS**

Connection	Connect To...	Purpose
VBUS1 (banana)	12 V supply	Provides channel 1 and channel 2 bus voltages
VBUS2 (banana)	6 V supply	Provides channel 3 and channel 4 bus voltages
VBUS3 (banana)	8 V supply	Provides channel 5 and channel 6 bus voltages
LOAD1 & GND (banana)	1 A load current	Provides channel 1 load current
LOAD2 & GND (banana)	0.5 A load current	Provides channel 2 load current
LOAD3 & GND (banana)	1 A load current	Provides channel 3
LOAD4 & GND (banana)	0.5 A load current	Provides channel 4 load current
LOAD5 & GND (banana)	1 A load current	Provides channel 5 load current
LOAD6 & GND (banana)	0.5 A load current	Provides channel 6 load current
VCC & GND	3.3 V	Provides NCP45491 supply
MUX_SEL (sma)	3.3 V to 0 V signal generator	Channel mux select input
EN (sma/header)	3.3 V to 0 V signal generator or tied to GND	NCP45491 enable input. Active low
DIFF_OUT_P (sma)	Oscilloscope	Differential output (positive)
DIFF_OUT_N (sma)	Oscilloscope	Differential output (negative)

1. All connections to the board have an accompanying ground connection. Use all ground connections with the evaluation board being the center of a star ground to avoid ground loops.
2. Connect to DIFF\_OUTN/P signals with either 2 SMA to BNC cables to an oscilloscope (where the subtraction of the 2 signals gives the differential voltage), or connect to the DIFF\_OUT\* test loops with a twisted pair or differential probe. Connecting in this manner mitigates noise via EMI.
3. SH\_INx inputs need to be driven to a voltage between VCC and 26 V, even for unused channels. Jumpers 1, 2, 5, and 8 provide a means to connect unused channels to VCC. If a channel is not in use, the jumper should be switched to the VCC position and the SH\_Ox jumper should be removed to float the SH\_Ox pin.

**Table 4. DEFAULT JUMPER DEFINITION**

Jumper	Default Setting	Function
J3, J6, J11, J12, J13, J14	Shorted [1,2]	Connects channel bus voltages. [2,3] connection sets bus voltage to 3.3 V if that channel is not in use
J4, J5, J9, J7, J8, J10	Shorted	Connects SH_Ox. Short for all used channels
J2	Shorted [1,2]	SKIP input connection
J1	Open	SMD jumper that can be shorted to tie EN to GND

4. The number of used channels for each NCP45491 chip must match. The default connects set 3 channels for each chip for a total of 6 channels. Up to 8 can be used.

## NCP45491PMNGEVB

### Testing Procedure

The NCP45491PMNGEVB comes fully assembled and tested. Follow the steps below to verify board operation. Refer to the schematic and layout diagrams found in [Appendix A](#) and [Appendix B](#) respectively as needed.

1. Apply power to VBUS inputs (12 V, 6 V, and 8 V supply).
2. Apply load currents for all channels.
3. Apply 3.3 V VCC power.
4. Ensure that EN is held at 0 V.
5. Apply MUX\_SEL signal. (Square wave 50% duty cycle, 100 kHz or faster, VCC to 0 V)
  - a. 12 cycles will read out voltage and current data for all 6 default channels.
  - b. Continuous cycles on MUX\_SEL will read out bus voltage and current data continuously, repeating channels 1–6.
6. Observe the following:
  - a. 1.3 V on BG\_REF\_OUT
  - b. 650 mV on CM\_REF\_IN
  - c. 170 mV on BS\_REF
  - d. Bus voltages and currents represented on DIFF\_OUTP and DIFF\_OUTN with oscilloscope.

### PCB Layout

Care must be taken in PCB layout regarding a few specific nodes for proper operation of the NCP45491. Connections to the external sense resistor for each channel must be treated as a 4 wire Kelvin connection. The SH\_IN\_Nx and the SH\_IN\_Px (connected through R1) must connect directly to the sense resistor leads for each respective channel. These should also be large traces to avoid error in the shunt current measurement. See [Appendix C](#) for the example layout of the evaluation board.

# NCP45491PMNGEVB

## APPENDIX A: NCP45491 PAIRED MODE EVALUATION BOARD SCHEMATIC

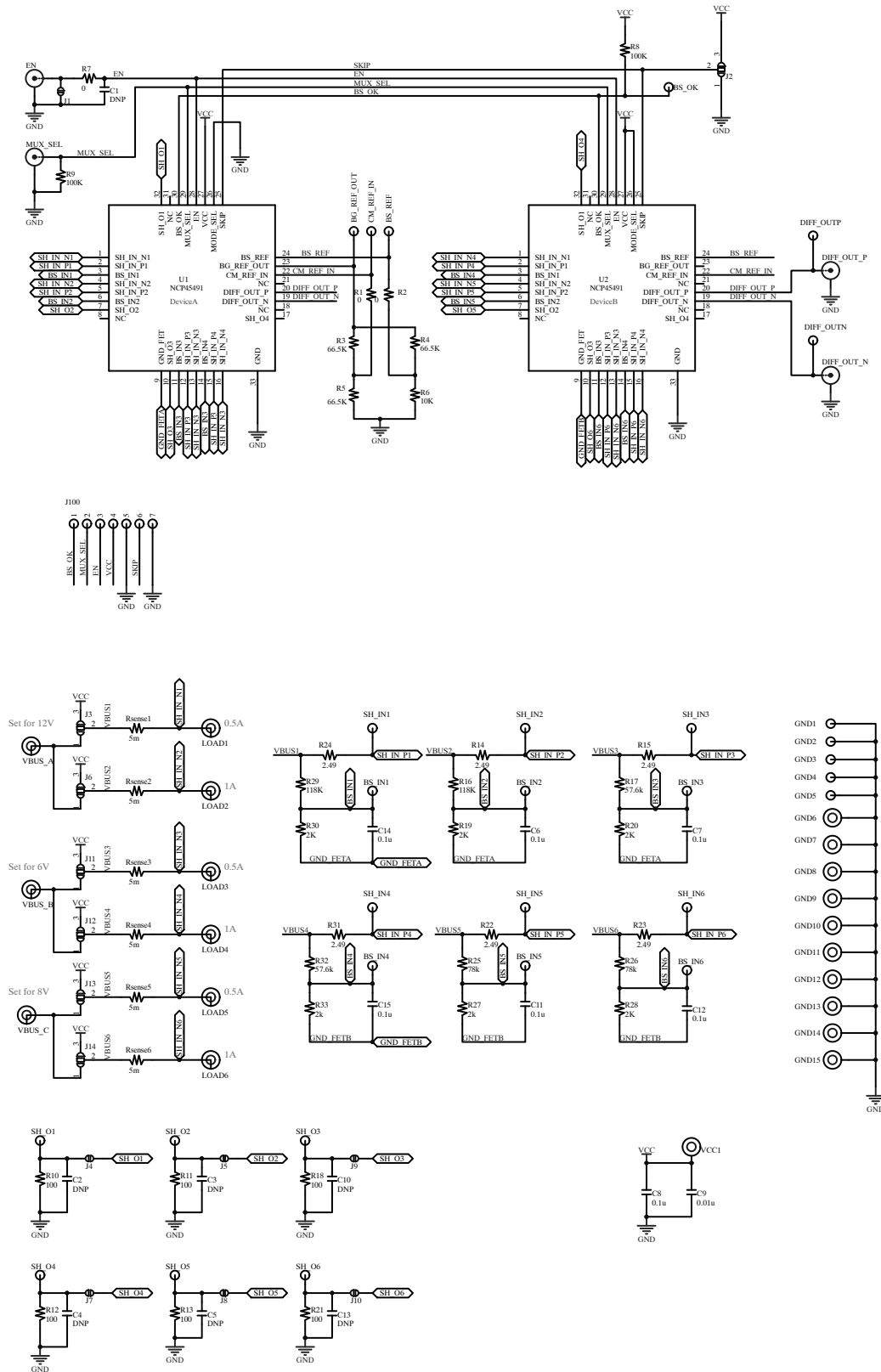


Figure 1. NCP45491 Paired Mode Evaluation Board Schematic

# NCP45491PMNGEVB

## APPENDIX B: BILL OF MATERIALS

**Table 5. BILL OF MATERIALS**

Designator	Description	Value	Manufacturer	Manufacturer P/N	Footprint
BG_REF_OUT, BS_IN1, BS_IN2, BS_IN3, BS_IN4, BS_IN5, BS_IN6, BS_OK, BS_REF, CM_REF_IN, DIFF_OUTN, DIFF_OUTP, GND1, GND2, GND3, GND4, GND5, SH_IN1, SH_IN2, SH_IN3, SH_IN4, SH_IN5, SH_IN6, SH_O1, SH_O2, SH_O3, SH_O4, SH_O5, SH_O6	Test Points	n/a	Keystone Electronics	5009	Test_Point
C1, C2, C3, C4, C5, C10, C13	SMD capacitor	Do not populate	n/a	n/a	SMD_0805
C6, C7, C8, C11, C12, C14, C15	SMD capacitor	0.1 $\mu$ F	Murata Electronics	GCM21BR71H104KA37K	SMD_0805
C9	SMD capacitor	0.01 $\mu$ F	Samsung Electro-Mechanics	CL21B103KBANNNC	SMD_0805
DIFF_OUT_N, DIFF_OUT_P, EN, MUX_SEL	SMB/SMA Straight Connector	SMA/SMB	Molex	733910060	SMB_V-RJ45
GND6, GND7, GND8, GND9, GND10, GND11, GND12, GND13, GND14, GND15, LOAD1, LOAD2, LOAD3, LOAD4, LOAD5, LOAD6, VBUS_A, VBUS_B, VBUS_C, VCC1	Interconnect	Banana Jack, female	Cinch Connectivity	111-2223-001	Bannana_Connector
J1	10th inch header	Leave open	n/a	n/a	SMD_2
J2, J3, J6, J11, J12, J13, J14	3 way jumper	3 pin 10" header	Würth Electronics Inc	61300311121	HEADER_3
J4, J5, J7, J8, J9, J10	10th inch header	2 pin 10" header	Würth Electronics Inc	61300211121	HEADER_2
R7, R1, R2	SMD resistor	0 $\Omega$	Stackpole Electronics	HCJ1206ZT0R00	RES1206
Rsense1, Rsense2, Rsense3, Rsense4, Rsense5, Rsense6	SMD resistor	5 m $\Omega$	Rohm Semiconductor	PMR18EZPFU5L00	RES1206
R29, R16	SMD resistor	118 k $\Omega$	Panasonic	ERJ-8ENF1183V	RES1206
R17, R32	SMD resistor	57.6 k $\Omega$	Vishay Dale	CRCW120657K6FKEA	RES1206
R25, R26	SMD resistor	78 k $\Omega$	Yageo	RC1206FR-0778K7L	RES1206
R30, R19, R20, R33, R27, R28	SMD resistor	2 k $\Omega$	Panasonic	ERA-8AEB202V	RES1206
R10, R11, R18, R12, R13, R21	SMD resistor	100 $\Omega$	Panasonic	ERA-8AEB101V	RES1206
R8, R9	SMD resistor	100 k $\Omega$	Rohm Semiconductor	ESR18EZPJ104	RES1206
R3, R4, R5	SMD resistor	66.5 k $\Omega$	Yageo	RC1206FR-0766K5L	RES1206
R6	SMD resistor	10 k $\Omega$	Stackpole Electronics	RNCP1206FTD10K0	RES1206
R14, R15, R22, R23, R24, R31	Resistor	2.49 $\Omega$	Vishay Dale	CRCW12062R49FKEAHP	RES1206
U1, U2	NCP45491	NCP45491	ON Semiconductor	NCP45491	RES1206

# NCP45491PMNGEVB

## APPENDIX C: NCP45491 EVALUATION BOARD LAYOUT

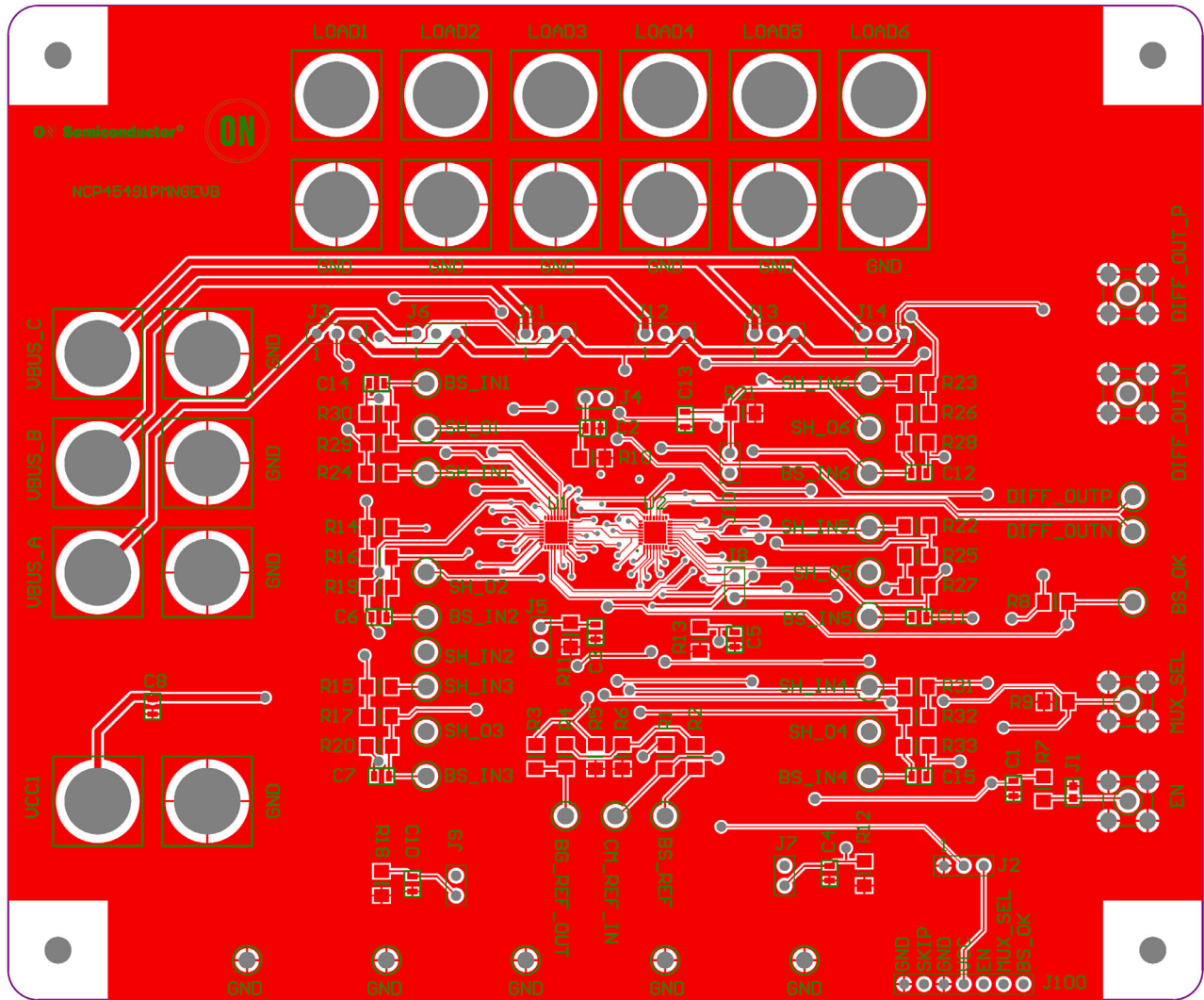


Figure 2. PCB Front (Top Metallization)

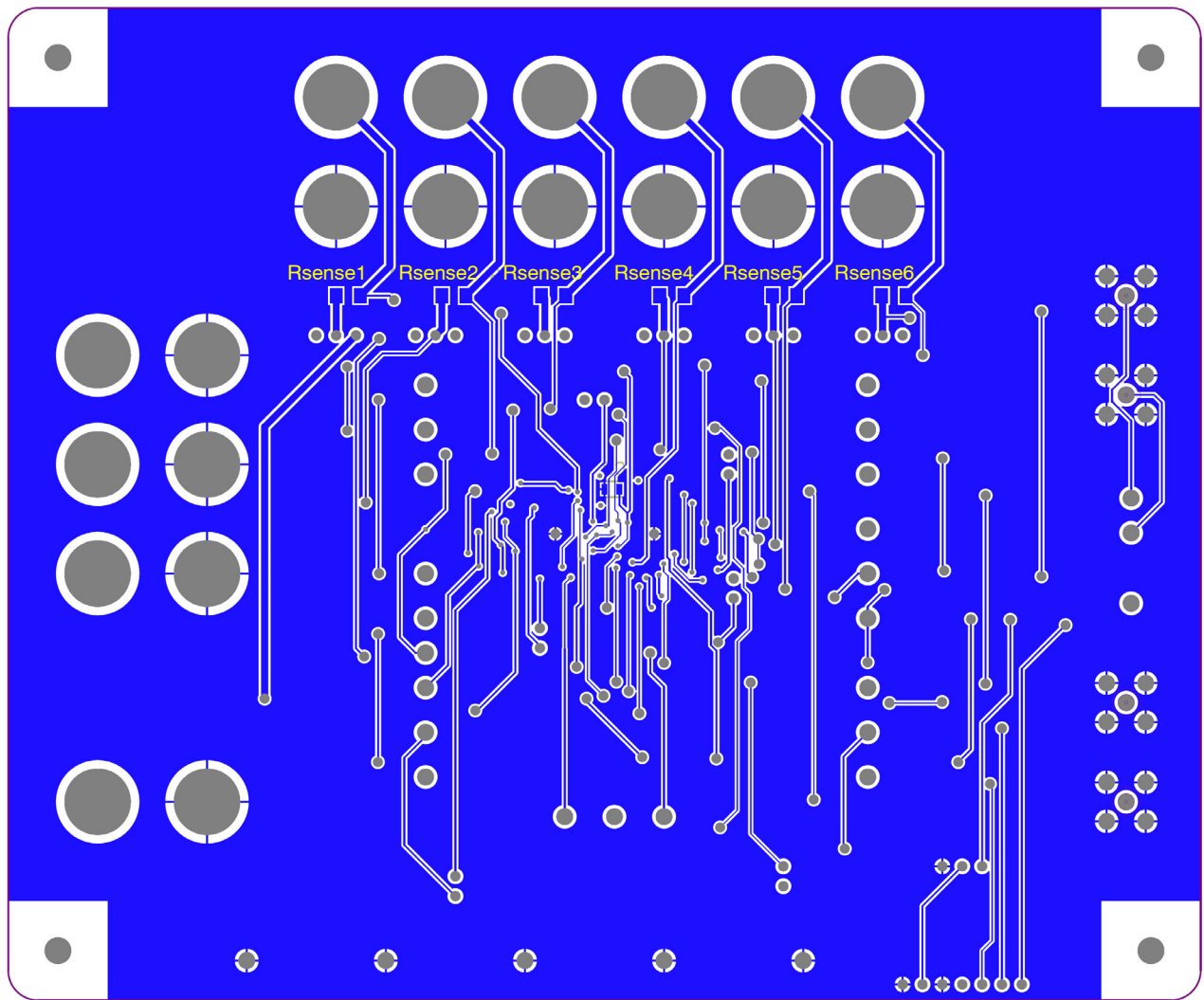


Figure 3. PCB Backside (Bottom Metallization)

**onsemi**, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

The evaluation board/kit (research and development board/kit) (hereinafter the "board") is not a finished product and is not available for sale to consumers. The board is only intended for research, development, demonstration and evaluation purposes and will only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. This person assumes full responsibility/liability for proper and safe handling. Any other use, resale or redistribution for any other purpose is strictly prohibited.

**THE BOARD IS PROVIDED BY ONSEMI TO YOU "AS IS" AND WITHOUT ANY REPRESENTATIONS OR WARRANTIES WHATSOEVER. WITHOUT LIMITING THE FOREGOING, ONSEMI (AND ITS LICENSORS/SUPPLIERS) HEREBY DISCLAIMS ANY AND ALL REPRESENTATIONS AND WARRANTIES IN RELATION TO THE BOARD, ANY MODIFICATIONS, OR THIS AGREEMENT, WHETHER EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, INCLUDING WITHOUT LIMITATION ANY AND ALL REPRESENTATIONS AND WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, NON-INFRINGEMENT, AND THOSE ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE CUSTOM OR TRADE PRACTICE.**

**onsemi** reserves the right to make changes without further notice to any board.

You are responsible for determining whether the board will be suitable for your intended use or application or will achieve your intended results. Prior to using or distributing any systems that have been evaluated, designed or tested using the board, you agree to test and validate your design to confirm the functionality for your application. Any technical, applications or design information or advice, quality characterization, reliability data or other services provided by **onsemi** shall not constitute any representation or warranty by **onsemi**, and no additional obligations or liabilities shall arise from **onsemi** having provided such information or services.

**onsemi** products including the boards are not designed, intended, or authorized for use in life support systems, or any FDA Class 3 medical devices or medical devices with a similar or equivalent classification in a foreign jurisdiction, or any devices intended for implantation in the human body. You agree to indemnify, defend and hold harmless **onsemi**, its directors, officers, employees, representatives, agents, subsidiaries, affiliates, distributors, and assigns, against any and all liabilities, losses, costs, damages, judgments, and expenses, arising out of any claim, demand, investigation, lawsuit, regulatory action or cause of action arising out of or associated with any unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of any products and/or the board.

This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and may not meet the technical requirements of these or other related directives.

**FCC WARNING** – This evaluation board/kit is intended for use for engineering development, demonstration, or evaluation purposes only and is not considered by **onsemi** to be a finished end product fit for general consumer use. It may generate, use, or radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment may cause interference with radio communications, in which case the user shall be responsible, at its expense, to take whatever measures may be required to correct this interference.

**onsemi** does not convey any license under its patent rights nor the rights of others.

**LIMITATIONS OF LIABILITY:** **onsemi** shall not be liable for any special, consequential, incidental, indirect or punitive damages, including, but not limited to the costs of requalification, delay, loss of profits or goodwill, arising out of or in connection with the board, even if **onsemi** is advised of the possibility of such damages. In no event shall **onsemi**'s aggregate liability from any obligation arising out of or in connection with the board, under any theory of liability, exceed the purchase price paid for the board, if any.

The board is provided to you subject to the license and other terms per **onsemi**'s standard terms and conditions of sale. For more information and documentation, please visit [www.onsemi.com](http://www.onsemi.com).

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)