
INTRODUCTION

Purpose
This manual provides detailed information about the configuration and use of the RSL10 Evaluation and Development Board (RSL10−002GEVB). The Evaluation and Development Board is designed to be used with the software development tools to evaluate the performance and capabilities of the RSL10 radio System-on-Chip (SoC).

Manual Organization
The Evaluation and Development Board Manual contains the following chapters and appendices:

• Chapter 1: Introduction describes the purpose of this manual, describes the target reader, explains how the book is organized, and provides a list of suggested reading for more information.
• Chapter 2: Overview provides an overview of the Evaluation and Development Board described in this manual.
• Chapter 3: Evaluation and Development Board provides the details of the Evaluation and Development Board. The chapter is divided into the following topics:
  ♦ Development Board Setup
  ♦ Development Board Design
  ♦ Power Supply
  ♦ Level Translators
  ♦ LED Circuitry
  ♦ RSL10 SoC
  ♦ Measuring the Current Consumption
  ♦ SWJ−DP Debug Port
  ♦ Digital Input/Output (DIO)
  ♦ Power Supply and Test Points
• Appendix A: Connectors provides a complete list of the connectors and jumpers on the Evaluation and Development Board.
• Appendix B: Schematics contains the schematics for the Evaluation and Development Board.
• Appendix C: Bill of Materials contains a list of the parts that are used to manufacture the Evaluation and Development Board.

Further Reading
For more information, refer to the following documents:

• Getting Started with RSL10
• RSL10 Firmware Reference

OVERVIEW

Introduction
The RSL10 Evaluation and Development Board is used for evaluating the RSL10 SoC and for application development. The board provides access to all input and output connections via 0.1” standard headers. The on-board communication interface circuit provides communication to the board from a host PC. The communication interface translates RSL10 SWJ−DP debug port signals to the USB of the host PC. There is also an on-board 4-bit level shifter for debugging; it translates the I/O signal level of RSL10 to the 3.3 V digital logic level. It is not enabled by default; you enable it when it is needed.

Evaluation and Development Board Features
The Evaluation and Development Board enables developers to evaluate the performance and capabilities of the RSL10 radio SoC in addition to developing, demonstrating and debugging applications.

Key features of the board include:

• J−Link onboard solution provides a SWJ−DP (serial-wire and/or JTAG) interface that enables you to debug the board via a USB connection with the PC
• Alternate onboard SWJ−DP (serial-wire and/or JTAG) interface for Arm® Cortex®−M3 processor debugging
• Access to all RSL10 peripherals via standard 0.1” headers
• Onboard 4-bit level translator to translate the LPDSP32 debug interface at low voltage to a 3.3 V JTAG debugger
• Antenna matching and filtering network
• Integrated PCB antenna
• Compliance with the Arduino form factor
• Support for PMOD (i.e., J4 is a standard connector)
Evaluation and Development Board Setup

This section is an overview of how to configure the Evaluation and Development Board. Details of the development board configuration are discussed later in this manual.

Figure 1 represents an overview of the board setup.

If you want to use an external J–Link debugger instead of the onboard one, connect the debugger to connector P2 on the QFN board, as shown in Figure 2. Notice that for this setup, you also need a power supply.

Evaluation and Development Board Design

The following sections detail the various sub-circuits of the RSL10 Evaluation and Development Board. The block diagram in Figure 3 shows the locations of the various circuit sections. Figure 5 and Figure 6 provide 3-dimensional illustrations of the QFN board.
Figure 4. Circuit Location Block Diagram (Bottom View)
Figure 5. Three-Dimensional Line Drawing of the Board (Top View)
Power Supply
The Evaluation and Development Board can be powered by one of the following:

- Micro USB port with regulator
- External power supply connector (P5) with regulator
- External power supply connector (P5) without regulator

Use the jumpers on pin headers P4, P7, and P10 to select a power supply option as shown in Table 1.

Table 1. POWER SUPPLY SELECTION

<table>
<thead>
<tr>
<th>Power Source</th>
<th>Jumper Position on P4</th>
<th>Jumper Position on P7</th>
<th>Jumper Position on P10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro USB Port with Regulator</td>
<td>1&amp;2</td>
<td>2&amp;3</td>
<td>1&amp;2</td>
</tr>
<tr>
<td>External Power Supply with Regulator</td>
<td>3&amp;4</td>
<td>2&amp;3</td>
<td>1&amp;2</td>
</tr>
<tr>
<td>External Power Supply without Regulator</td>
<td>5&amp;6</td>
<td>2&amp;3</td>
<td>2&amp;3</td>
</tr>
</tbody>
</table>

Table 2. MINIMUM/MAXIMUM EXTERNAL REGULATED VOLTAGES

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Header</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSL10 and J–Link OB MCU</td>
<td>EXT–PSU Regulated</td>
<td>3.3 V</td>
<td>3.6 V</td>
<td>12.0 V</td>
</tr>
<tr>
<td>RSL10 and J–Link OB MCU</td>
<td>USB</td>
<td>–</td>
<td>5.0 V</td>
<td>–</td>
</tr>
<tr>
<td>RSL10</td>
<td>EXT–PSU Unregulated</td>
<td>1.1 V</td>
<td>1.25 V</td>
<td>3.6 V</td>
</tr>
</tbody>
</table>

Level Translators
The board has level translators for the DIO signals of RSL10, including the clock signal. The level translators facilitate interfacing to external devices that operate at a higher voltage than RSL10.

VDDO and 3.3 V are two different power rails. The translator allows a logic signal on the VDDO side to be translated to either a higher or a lower logic signal voltage on the 3.3 V side, and vice-versa.

The level translation circuitry consists of components U4 and the 2x4 header. Signals are translated from the VDDO voltage reference to 3.3 V (default) voltage provided by the regulator output or by an external supply. The VDDO voltage is configured by the pin on header P11 (located on the board edge) to either VB {A}T {D}UT, 3.3 V or other level within the VDDO voltage range, which is 1.1 to 3.3 V.

The NLSX5014 level translators are bi-directional. They have the following features:

- Wide voltage operating range: 0.9 V to 4.5 V
- VDDO and 3.3 V are independent
- VDDO can be equal to, or less than, 3.3 V when connected to the power rail

To enable the level translators, populate positions R34 and R35 with 0 ohms. By default, the level translators are disabled. NOTE: Enabling the level translator affects power consumption.

LED Circuitry
There are two LEDs on the board. One is a dual color LED, called LD1, connected to the J–Link emulator microcontroller unit (MCU). The other is the green LED, connected to DIO 6 of RSL10. You can use this LED within your applications as an indication LED by programming DIO 6. If DIO 6 is high, this LED is on.

Measuring the Current Consumption
This section deals with measuring current consumption for the Evaluation and Development Board.

Headers are provided for each of the regulated voltages for additional capacitance and/or for measurements. RSL10 has 16 digital I/Os. The VDDO pin in header P9 configures the I/O voltages for power domains to VB {A}T. The VB {A}T pin in header P10 configures the VB {A}T source. The power select pin in header P4 configures the power source of the RSL10. In addition, the measurements should be done by connecting an ammeter to current measure header P3 to measure the device power consumption in isolation.

To measure the current consumption of RSL10 only, you need to source the chip using the external power supply without the regulator as shown in Table 2. To remove leakage currents during current measurement, remove the jumpers on header SWD. Removing the jumpers between the MCU and RSL10 that connect nRESET, SWDIO and SWCLK prevents current leakage from the JTAG interface, avoiding inaccurate current measurements. In addition, DIOs 4, 5, and 6 must be configured to High–Z (disabled) without pull up in software. DIOs 4 and 5 are directly connected to the Atmel chip and will leak power into it. DIO 6 is directly connected to the transistor driving the LED and can leak power into it.
SWJ–DP DEBUG Port
The J–Link adapters are typically used to communicate with RSL10 using the standard Coresight SWJ–DP debug port in a JTAG/SW communication protocol. The 9-pin 0.05 in Samtec FTSH header (P1), defined by the Arm Cortex–M3 core on the board, connects RSL10 to external adapters compatible with the Arm Cortex–M3 processor’s SWJ–DP interface. Alternatively, you can connect the micro USB port on the board to a PC.

DIGITAL Input/Output (DIO)
RSL10 contains 16 digital I/O (DIO) signals. The DIO voltage domain is VDDO, while the input voltage can be VBAT or external voltage as outlined in Section “Measuring the Current Consumption” on page 7.

The DIO signals on RSL10 are multiplexed with several interfaces, including:
• One I2C interface (DIO [7:8])
• Four external inputs to the low-speed analog to digital converters (DIO [0:3])
• One PCM interface
• Two PWM drivers
• Two SPI interfaces (DIO [13:15])
• One UART interface (DIO [4:5])
• Support interfaces that can be used to monitor control of the RF front-end and Bluetooth® baseband controller

For more information about the DIO multiplexed signals, refer to the RSL10 Hardware Reference.

The board provides access to any of the DIOs or their multiplexed signals via the Arduino Headers (Power1, AD1, IOL1, and IOH1).

The LED circuit provides visual monitoring of the DIOs; refer to Section “LED Circuitry” on page 7 for further information.

Power Supplies
There are several external power supplies available on your Evaluation and Development Board.

The user can also access signals on various headers on boards, as described throughout this document.

The external power supplies available for QFN boards are:
• VBUS, 5 V from USB connection – available only when USB is plugged in
• V3.3, 3.3 V from LDO – available when regulated supply is selected
• VEXT, (P5 header) unregulated external supply – available when unregulated supply is selected
• Battery (J5 Battery Holder, 12 mm coin cell battery)
APPENDIX A – CONNECTORS

Overview
This appendix lists all connectors on the Evaluation and Development Board. The sections that follow provide descriptions for:
- Jumpers and their possible configurations
- Headers
- Switches and their possible configurations
- Connectors

Configuration Header Jumpers

Table 3. JUMPER DESCRIPTIONS

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P4</td>
<td>Regulated or Unregulated power supply selection</td>
</tr>
<tr>
<td>P10</td>
<td>VBAT Power Source selection (3.3 V, Vext or Battery)</td>
</tr>
<tr>
<td>P9</td>
<td>VDDO selection (VBAT_DUT, 3.3 V)</td>
</tr>
<tr>
<td>P8</td>
<td>VDD_AT selection (3.3 V, VDDO)</td>
</tr>
<tr>
<td>P1</td>
<td>Onboard JTAG debugger connection</td>
</tr>
</tbody>
</table>

Headers

Table 4. HEADER DESCRIPTIONS

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER1</td>
<td>Arduino Power header 3.3 V, VDDO, nRESET, GND</td>
</tr>
<tr>
<td>AD1</td>
<td>Arduino Analog Inputs header A [0:3]</td>
</tr>
<tr>
<td>IOI1</td>
<td>Arduino IOI header UART, INT [0:1], SPI2</td>
</tr>
<tr>
<td>IOH1</td>
<td>Arduino IOH header I2C, SPI1</td>
</tr>
<tr>
<td>P2</td>
<td>External JTAG debug connection header</td>
</tr>
<tr>
<td>P3</td>
<td>Current measurement header</td>
</tr>
<tr>
<td>P5</td>
<td>External power supply header</td>
</tr>
<tr>
<td>P6</td>
<td>Input and output of level shifter</td>
</tr>
</tbody>
</table>

Switches

Table 5. SWITCH DESCRIPTIONS

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1</td>
<td>Pushbutton switch to reset RSL10</td>
</tr>
<tr>
<td>SW2</td>
<td>Pushbutton switch for DIO5</td>
</tr>
</tbody>
</table>

Connectors

Table 6. CONNECTOR DESCRIPTIONS

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>RF switch connector</td>
</tr>
<tr>
<td>J2</td>
<td>Micro USB port for power supply, JTAG and UART emulation</td>
</tr>
<tr>
<td>J3</td>
<td>MCU programming connector</td>
</tr>
<tr>
<td>J4</td>
<td>Digilent PMOD peripheral connector I2C, SPI1, INT0</td>
</tr>
<tr>
<td>J5</td>
<td>Battery Holder (12 mm coin cell)</td>
</tr>
</tbody>
</table>
This appendix contains schematics for the Evaluation and Development Board, version 1.3:

- The Top-level (Arduino interface) schematic
- The RSL10 schematic
- The Interface MCU schematic
- The Power Supply schematic
Figure 7. Top-Level (Arduino Interface) Schematic
Figure 8. RSL10 SoC Schematic
Figure 9. Interface MCU Schematic
Figure 10. Power Supply Schematic

VDD is the digital IO ring supply (provided externally). Range: 1.1V - 3.3V

Optional Level Shifter

POWER SUPPLY CONFIGURATION HEADERS P4, P7, P10

ARDUINO ORION POWERED VIN3.3V: P4 (no jumper), P7(1-2), P10(1-2)
STAND ALONE USB POWERED: P4(1-2), P7(2-3), P10(1-2)
STAND ALONE Vext POWERED: P4(3-4), P7(2-3), P10(1-2)
STAND ALONE USB and Vext POWERED: P4(1-2), (5-6), P7(2-3), P10(2-3)

V3.3

VIN3.3V

Power Select

VDD_AT Select

VDDO Select

V3.3

U3

NCP551SN32T1G

VIN3.3V

123

U5

PCA9655

INT

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

R45

R44

DIO6

DIO9

DIO8

DIO7

DIO[15:9]

DIO[15:8]

DIO5

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

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DIO[7:0]

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DIO[7:0]

DIO8

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INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0

SCL

SDA

DIO[7:0]

DIO8

DIO7

INT0
<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
<th>Footprint Doc</th>
<th>Manufacturer Part Number</th>
<th>Supplier Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD1</td>
<td>Arduino Stackable Header 6-pin</td>
<td>n/a</td>
<td>SSQ-106-03-G-S</td>
<td>SAM1198-06-ND</td>
</tr>
<tr>
<td>C2, C3, C4, C5, C6</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM1555C1E120GA101</td>
<td>490-8169-1-ND</td>
</tr>
<tr>
<td>C7</td>
<td>CAP CER 2.2 μF 10 V X5R 0402</td>
<td>0402</td>
<td>GKM155R61A225KE96D</td>
<td>490-10451-1-ND</td>
</tr>
<tr>
<td>C9, C16, C40</td>
<td>CAP CER 4.7 μF 10 V X5R 0603, CAP CER 4.7 μF 25 V X5R 0603</td>
<td>0603</td>
<td>GKM188R61A475KE15</td>
<td>490-10477-1-ND</td>
</tr>
<tr>
<td>C11</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM1555C1H101JA01J</td>
<td>490-7754-1-ND</td>
</tr>
<tr>
<td>C12, C13</td>
<td>CAP CER 1.5 PF 50 V NP0 0402</td>
<td>0402</td>
<td>GCM1555C1H15RCA16D</td>
<td>490-13289-1-ND</td>
</tr>
<tr>
<td>C14</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM1555C1E120GA101</td>
<td>490-8169-1-ND</td>
</tr>
<tr>
<td>C10, C18, C19, C20, C21, C23, C25, C27, C29, C30, C31, C32, C33, C36, C37, C38, C39, C48</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM155R61E104KA87D</td>
<td>490-5920-1-ND</td>
</tr>
<tr>
<td>C22</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM1555C1E100UA01D</td>
<td>490-6168-1-ND</td>
</tr>
<tr>
<td>C24, C34, C35</td>
<td>Capacitor, X5R, ±10%</td>
<td>0603</td>
<td>GKM188R61A106KE8D</td>
<td>490-10474-1-ND</td>
</tr>
<tr>
<td>C26, C28</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM1555C1E180JA01D</td>
<td>490-6172-1-ND</td>
</tr>
<tr>
<td>C1, C8, C17, C41, C42, C45, C46</td>
<td>Capacitor, NP0, ±10%</td>
<td>0402</td>
<td>GKM155R61A105KE15D</td>
<td>490-3890-1-ND</td>
</tr>
<tr>
<td>C44, C47</td>
<td>Capacitor, NP0, ±12%</td>
<td>0402</td>
<td>GKM155R71H103KA88D</td>
<td>490-4516-1-ND</td>
</tr>
<tr>
<td>D1</td>
<td>Ultra low capacitance double rail-to-rail ESD protection diode</td>
<td>SOT-143B</td>
<td>PRTR5V0U2X125</td>
<td>568-4140-1-ND</td>
</tr>
<tr>
<td>IDH1</td>
<td>Arduino Stackable Header 10-pin</td>
<td></td>
<td>SSQ-110-03-G-S</td>
<td>SAM1198-10-ND</td>
</tr>
<tr>
<td>IO1, POWER1</td>
<td>Arduino Stackable Header 8-Pin</td>
<td></td>
<td>SSQ-108-03-G-S</td>
<td>SAM1198-08-ND</td>
</tr>
<tr>
<td>J1</td>
<td>Coaxial Connector with Switch</td>
<td>COAXIAL-SWF</td>
<td>MMB130-2600RA2</td>
<td>490-4981-1-ND</td>
</tr>
<tr>
<td>J2</td>
<td>MicroUSB-B- SMT</td>
<td>FCI_1018193-0001LF</td>
<td>1018193-0001LF</td>
<td>609-4616-1-ND</td>
</tr>
<tr>
<td>J4</td>
<td>WR-PhD 2.54 mm Angled Dual Socket Header, 12p</td>
<td></td>
<td>613012243121</td>
<td>SS559-ND</td>
</tr>
<tr>
<td>J5</td>
<td>HOLDER BATTERY 12 MM COIN</td>
<td></td>
<td>2996</td>
<td>36-2996-ND</td>
</tr>
<tr>
<td>L1</td>
<td>FIXED IND 3NH 800MA 170 MOHM SMD</td>
<td>0402</td>
<td>LQG15HS3N0S02D</td>
<td>490-6570-1-ND</td>
</tr>
<tr>
<td>L2</td>
<td>FIXED IND 1.8NH 950MA 100 MOHM</td>
<td>0402</td>
<td>LQG15HS1N8S02D</td>
<td>490-2613-1-ND</td>
</tr>
<tr>
<td>L3</td>
<td>Inductor, 320 mA, ±5%</td>
<td>0402</td>
<td>HK100515NJ-T</td>
<td>587-1521-1-ND</td>
</tr>
<tr>
<td>L4</td>
<td>Imported</td>
<td>0805</td>
<td>CKP2012N2R2M-T</td>
<td>587-2771-1-ND</td>
</tr>
<tr>
<td>LD1</td>
<td>Ultra bright AlInGaP Bi-Color LED</td>
<td></td>
<td>LED_DUAL_0606</td>
<td>LTST-C195KGJKRT</td>
</tr>
<tr>
<td>LED 1</td>
<td>LED SMARTLED GREEN 570NM 0603</td>
<td>0603</td>
<td>LNJ337W83RA</td>
<td>LNJ3782RFAC-ND</td>
</tr>
<tr>
<td>P1, P4</td>
<td>Header 2x3 SMT</td>
<td>15-91-2090</td>
<td>WM17449-ND</td>
<td></td>
</tr>
<tr>
<td>P2</td>
<td>SAMTEC - CONN HEADER 10POS DUAL. 05” SMD KEYING SHROUD</td>
<td>FTSH-105</td>
<td>FTSH-105-01-F-DV-K</td>
<td>SAM8796-ND</td>
</tr>
<tr>
<td>P3, P5</td>
<td>HEADER, 2POS, 1ROW: Series: 961; Pitch Spacing: 2.54 mm; RA</td>
<td>961102-6004-AR</td>
<td>3M9467-ND</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>2x4 Pin Header</td>
<td>15-91-2090</td>
<td>WM17450-ND</td>
<td></td>
</tr>
<tr>
<td>P7, P8, P9, P10</td>
<td>HEADER, 3POS, 1ROW: Series: 961; Pitch Spacing: 2.54 mm;</td>
<td>961103-6404-AR</td>
<td>3M9448-ND</td>
<td></td>
</tr>
<tr>
<td>Q1</td>
<td>NMOS Transistor</td>
<td>SOT65P210X105-3N</td>
<td>RU1J002YNTCL</td>
<td>RU1J002YNTCLCT-ND</td>
</tr>
<tr>
<td>R1, R2, R4, R9, R30, R31</td>
<td>Resistor, ±1%, 0.063 W</td>
<td>0402</td>
<td>ERF-2R6068R0X</td>
<td>P68.OLCT-ND</td>
</tr>
</tbody>
</table>
Table 7. BILL OF MATERIALS FOR RSL10 QFN EVALUATION AND DEVELOPMENT BOARD VERSION 1.3

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
<th>Footprint Doc</th>
<th>Manufacturer Part Number</th>
<th>Supplier Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>R3, R6, R26, R27, R32, R44, R46, R48, R49, R50,</td>
<td>Resistor, ±1%, 0.063 W</td>
<td>0402</td>
<td>ERJ-2RKF68R0X, ERJ-2RKF68R0X</td>
<td>P68.0LCT-ND, P68.0LCT-ND, P0.0JCT-ND, P0.0JCT-ND, 173-8862, P10KJCT-ND, P10KJCT-ND, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862, 173-8862</td>
</tr>
<tr>
<td>R10, R11</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2RKF39R0X</td>
<td>P39.0LCT-ND</td>
</tr>
<tr>
<td>R12, R13, R14, R20</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2RKF4701X</td>
<td>P4.70KLCT-ND</td>
</tr>
<tr>
<td>R15, R16</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2RKF2200X</td>
<td>P220LCT-ND</td>
</tr>
<tr>
<td>R17, R18, R19, R29</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2RKF8001X</td>
<td>P6.80KLCT-ND</td>
</tr>
<tr>
<td>R21, R45, R47, R52, R53</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2GEO800X</td>
<td>P0.0JCT-ND</td>
</tr>
<tr>
<td>R22, R23, R24, R25, R28</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2RKF1500X</td>
<td>173-8862</td>
</tr>
<tr>
<td>R54</td>
<td>Resistor, ±1%, 0.1 W</td>
<td>0402</td>
<td>ERJ-2RKF1000X</td>
<td>P100KJCT-ND</td>
</tr>
<tr>
<td>SW1, SW2</td>
<td>ALPS - SKHU000280 - Tactile Switch, 6.5 x 6.2 x 2.5 mm</td>
<td>0402</td>
<td>SKHU000280</td>
<td>35-790-00</td>
</tr>
<tr>
<td>U1</td>
<td>RSL10 QFN</td>
<td>0402</td>
<td>ATSAM3U2CA-AU</td>
<td>ATSAM3U2CA-AU</td>
</tr>
<tr>
<td>U2</td>
<td>IC MCU 32 bit 128 kbyte Flash 100LQFP</td>
<td>0402</td>
<td>NCP114ASN330T1G</td>
<td>NCP114ASN330T1G</td>
</tr>
<tr>
<td>U3</td>
<td>IC REG LIN 3.3 V 600MA TSOP</td>
<td>0402</td>
<td>NLSX5014DTR2G</td>
<td>NLSX5014DTR2G</td>
</tr>
<tr>
<td>U4</td>
<td>TRANSLATOR LEVEL 4BIT 14-TSSOP</td>
<td>0402</td>
<td>PCA9655EMTXXG</td>
<td>PCA9655EMTXXG</td>
</tr>
<tr>
<td>U5</td>
<td>Remote 16-bit expander QFN50P400X400</td>
<td>0402</td>
<td>ECS-480-8-47-JTN-TR</td>
<td>X1969CT-ND</td>
</tr>
<tr>
<td>X1</td>
<td>ECS 48 MHz Crystal</td>
<td>0402</td>
<td>X1_3215</td>
<td>FC-135 32.7680kHz E20PPM</td>
</tr>
<tr>
<td>X2</td>
<td>EPSON TOYOMOM - FC-135 32.768 kHz ±20 ppm</td>
<td>0402</td>
<td>BT-XTAL_3225</td>
<td>FC-135 32.7680KA-AC-ND</td>
</tr>
<tr>
<td>X3</td>
<td>XTAL SMD 3225, 12 MHz, 18 pf, ±50 ppm</td>
<td>0402</td>
<td>BT-XTAL_3225</td>
<td>7M-12.000MAJ-T</td>
</tr>
</tbody>
</table>

NOTE: Designators C2, C3, C4, C5, C6 and R3, R5, R6, R26, R27, R32, R44, R46, R48, R49, R50 are not populated.

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