AP0200ATSL00XUGAH3-GEVB

AP0200AT Evaluation Board User's Manual

ON Semiconductor®

EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of image sensors products from ON Semiconductor. This headboard is intended to plug directly into the Demo 3 system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Figure 1. AP0200AT Evaluation Board

Features

- Clock Input
  - Default – 27 MHz Crystal Oscillator
  - Optional Demo 3 Controlled MClk
- Two Wire Serial Interface
  - Selectable Base Address
- Parallel Interface
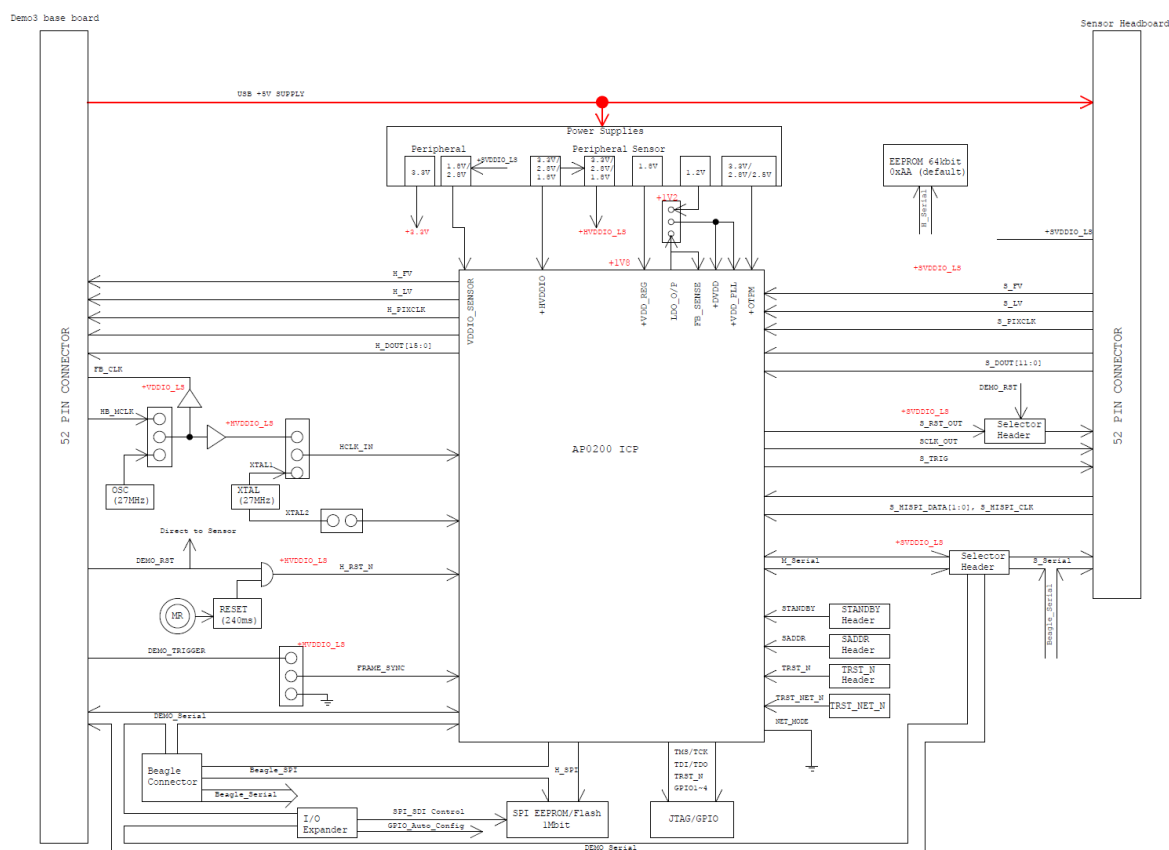- HiSPi (High Speed Serial Pixel) Interface
- ROHS Compliant

Block Diagram

Figure 2. Block Diagram of AP0200ATSL00XUGAH3−GEVB

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Top View

Headboard Connector **P6**

RESET Switch **SW7**
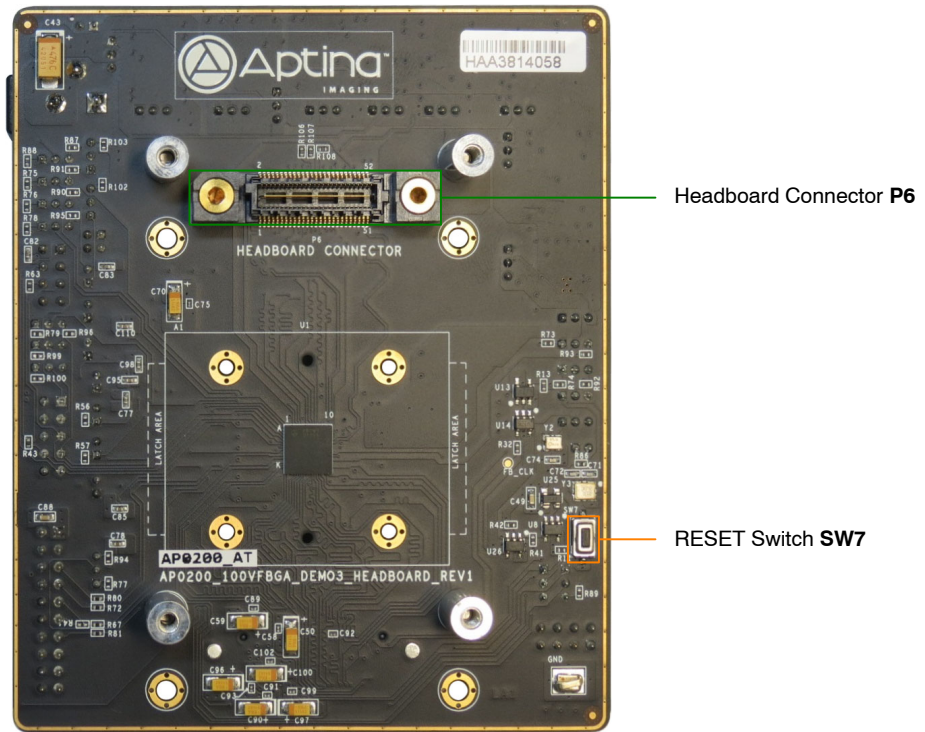
Figure 3. Top View of the Board − Default Jumpers

Bottom View

+VDDIO Select **P57**
+VDDIO_LS **P13**
+VDDIO_SENSOR **P19**
+2V8_VDDPHY **P12**
+1V8_VAA **P41**

+3V3 **P24**

+1V2_DVDD_REG **P56**

+1V2_DVDD Sel **P55**
ENLDO **P36**
EXT_REG **P37**
OSC/XTAL **P22**
MCLK_IN **P16**
OSC/XTAL **P23**

SEN_RST_OUT **P54**
FRAME_SYNC **P40**

+VDDIO **P21**

+2V8_VAA_OTPM **P14**
ON_LED **P11**
+5V0 **P8**

SEN_DATA **P51**
TRIGGER **P59**
STANDBY **P38**
SADDR **P39**
TRST_NET_N **P49**

LSC EPROM **P27**

SENSOR Access SCL **P30**

NET_MODE **P58**
BEAGLE SCL **P52**
BEAGLE SDA **P53**
SENSOR Access SDA **P31**

DIAG Operation **P32**

FRAME_SYNC **P40**

Baseboard Connector **J1**

Figure 4. Bottom View of the Board − Connectors

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.
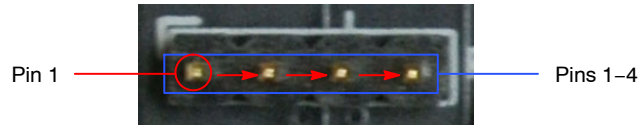
Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right
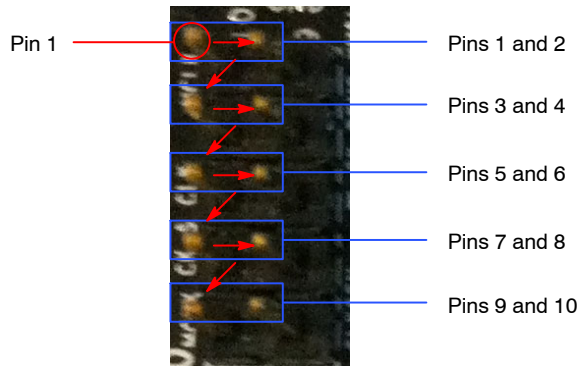

**Figure 6. Pin Locations and Assignments of Grouped Jumpers.
Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture**

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
P5, P47	EEPROM Mode	P5 Closed, P47 Open (Default)	Set to Host Mode during Power On
		P5 Open, P47 Open	Set to Flash Mode during Power On
		P47 Closed	Set to Auto-Config Mode during Power On
P8	+5V0	2–3 (Default)	Using On-Board +5V0 Power Supply
		1–2	Using +5V0 Supply from External Power Adapter
P11	ON_LED	1–2 (Default)	Connects to On-Board to Indicate "Power On"
P12	+2V8_VDDPHY	2–3 (Default)	Using On-Board +2V8_VDDPHY_ADJ Power Supply
		1–2	Using +2V8_VDDIO_HB Power Supply from Demo 3 Baseboard
P13	+VDDIO_LS	2–3 (Default)	Using On-Board Power Supply
		1–2	Using +1V8_HB Power Supply from Demo 3 Baseboard
P14	+2V8_VAA_OTPM	2–3 (Default)	Using On-Board +2V8_VAA_OTPM_ADJ Power Supply
		1–2	Using +2V8_VAA_HB Power Supply from Demo 3 Baseboard
P16	MCLK_IN	1–2 (Default)	Connects to On-Board Oscillator
		2–3	Connects to XMCLK
P19	+VDDIO_SENSOR	2–3 (Default)	Using On-Board Power Supply
		1–2	Using +1V8_HB Power Supply from Demo 3 Baseboard

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P21	+VDDIO	2−3 (Default)	Using On-Board Power Supply
		1−2	Using +1V8_HB or +2V8_HB Power Supply from Demo 3 Baseboard
P22, P23	OSC/XTAL Select	P22 2−3, P23 Open (Default)	Oscillator/Demo Clock Selected
		P22 1−2, P23 Closed	On-Board Crystal Selected
P24	+3V3	2−3 (Default)	Using On-Board Power Supply
		1−2	Using +3V3_HB Power Supply from Demo 3 Baseboard
P25, P34	I/O Expander Address	P25 Closed, P34 Open (Default)	I/O Expander Address Set to 0x48
		P25 Open, P34 Open	I/O Expander Address Set to 0x4C
		P25 Open, P34 Closed	I/O Expander Address Set to 0x44
		P25 Closed, P34 Closed	I/O Expander Address Set to 0x40
P27	LSC EEPROM	1−2 Closed, 3−4 Open (Default)	EEPROM Address Set to 0xA8
		1−2 Open, 3−4 Open	EEPROM Address Set to 0xAC
		1−2 Open, 3−4 Closed	EEPROM Address Set to 0xA4
		1−2 Closed, 3−4 Closed	EEPROM Address Set to 0xA0
P30	Sensor Access SCL	Open (Default)	Beagle Serial No Access to Demo 3 & Sensor
		1−2	Beagle Serial Access to Demo 3 & Sensor
P31	Sensor Access SDA	Open (Default)	Beagle Serial No Access to Demo 3 & Sensor
		1−2	Beagle Serial Access to Demo 3 & Sensor
P32	Diag Operation	Open (Default)	Disable Diag Operation
		1−2	Enable Diag Operation
P36	ENLDO	2−3 (Default)	Internal Regulator Not Enabled
		1−2	Regulator Enable
P37	EXT_REG	1−2 (Default)	Select External Regulator
		2−3	Select Internal Regulator
P38	STANDBY	2−3 (Default)	Active Mode
		1−2	Standby Mode
P39	SADDR	2−3 (Default)	I^{2}C Address Set to 0x90
		1−2	I^{2}C Address Set to 0xBA
P40	FRAME_SYNC	2−3 (Default)	GND
		1−2	Connect to Demo 3 Trigger
P41	+1V8_VAA	2−3 (Default)	Using On-Board +1V8_VAA Power Supply
		1−2	Using +1V8_HB Power Supply from Demo 3 Baseboard
P42	TRST_N	2−3 (Default)	Normal Mode
		1−2	Test Mode for Image System Processor
P49	TRST_NET_N	2−3 (Default)	Normal Mode
		1−2	Test Mode for Image Agent Processor
P50	SEN_SCLK	2−3 (Default)	AP0102 Serial Control
		1−2	Demo 3 Serial Control

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P51	SEN_SDATA	Open (Default)	AP0102 Serial Control
		1−2	Demo 3 Serial Control
P52	BEAGLE_SCL	1−2	Demo 3 Accessed
		2−3	Sensor Accessed
P53	BEAGLE_SDA	1−2	Demo 3 Accessed
		2−3	Sensor Accessed
P54	SEN_RST_OUT	2−3 (Default)	AP0102 Reset
		1−2	Demo 3 Reset
P55	+1V2_DVDD Selection	2−3 (Default)	Using On-Board Regulator +1V2 Power Supply
		1−2	Using +1V2 Internal Power Supply
P56	+1V2_DVDD_REG	2−3 (Default)	Using On-Board +1V2_DVDD_ADJ Power Supply
		1−2	Using +1V2_HB Power Supply from Demo 3 Baseboard
P57	+VDDIO Selection	1−2 (Default)	Using +1V8_HB Supply for +VDDIO
		2−3	Using +2V8_HB Supply for +VDDIO
P58	NET_MODE	2−3 (Default)	I^{2}C to Image Co-Processor
		1−2	I^{2}C to Agent Co-Processor
P59	TRIGGER	2−3	Connect to GND
		1−2	Connect to +VDDIO
		Open (Default)	Control from Demo 3 Baseboard
SW7	RESET	N/A	When Pushed, 240 ms Reset Signal will be Sent to AP0200

Interfacing to ON Semiconductor Demo 3 Baseboard

The ON Semiconductor Demo 3 baseboard has a similar 52-pin connector which mates with J1 of the headboard.

The four mounting holes secure the baseboard and the headboard with spacers and screws.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
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