

AP0100CSSL00SPGAH-GEVB

AP0100CS Evaluation Board User's Manual



ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 2X system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Features

- Clock Input
 - ♦ Default – 27 MHz Crystal Oscillator
 - ♦ Optional Demo 2X Controlled MCLK
- Two Wire Serial Interface
- Parallel Interface
- HiSpi (High Speed Serial Pixel) Interface
- ROHS Compliant



Figure 1. AP0100CS Evaluation Board

Block Diagram

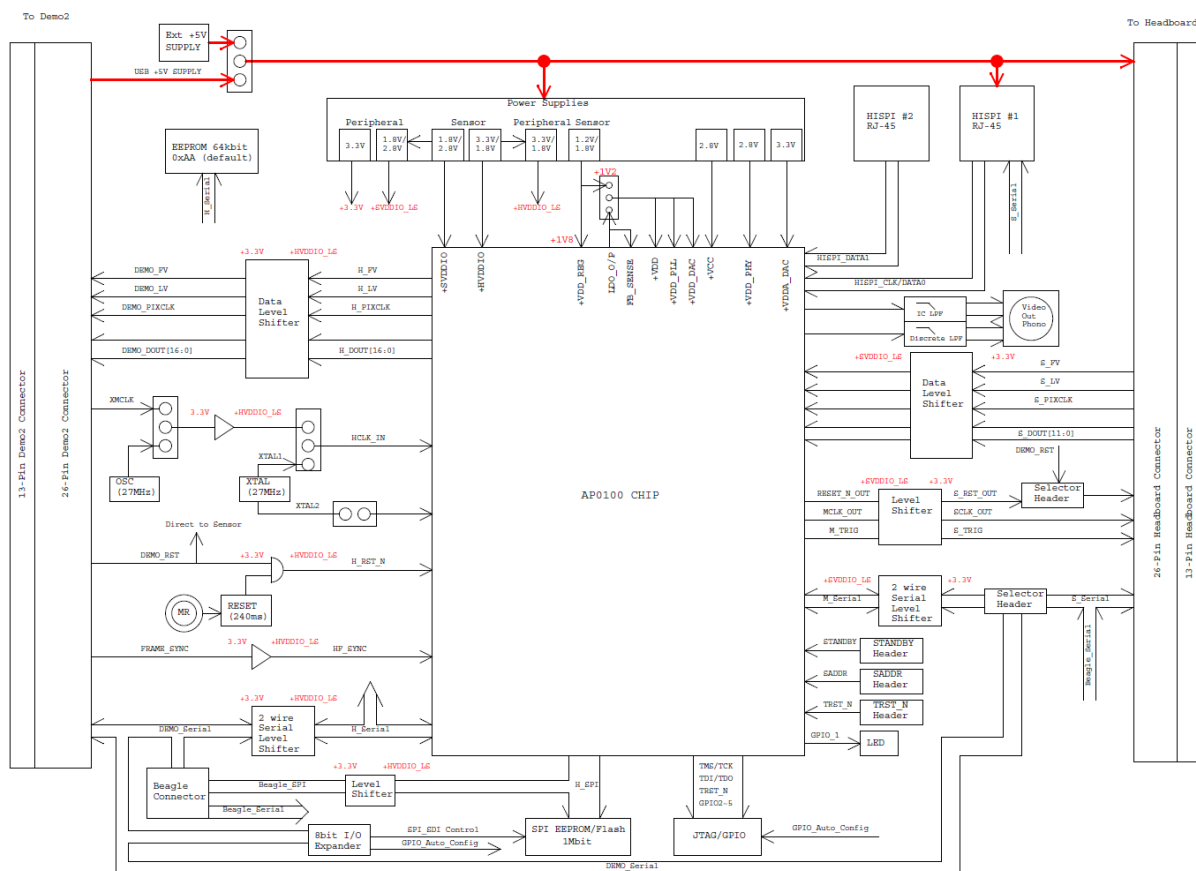


Figure 2. Block Diagram of AP0100CSSL00SPGAH-GEVB

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Top View

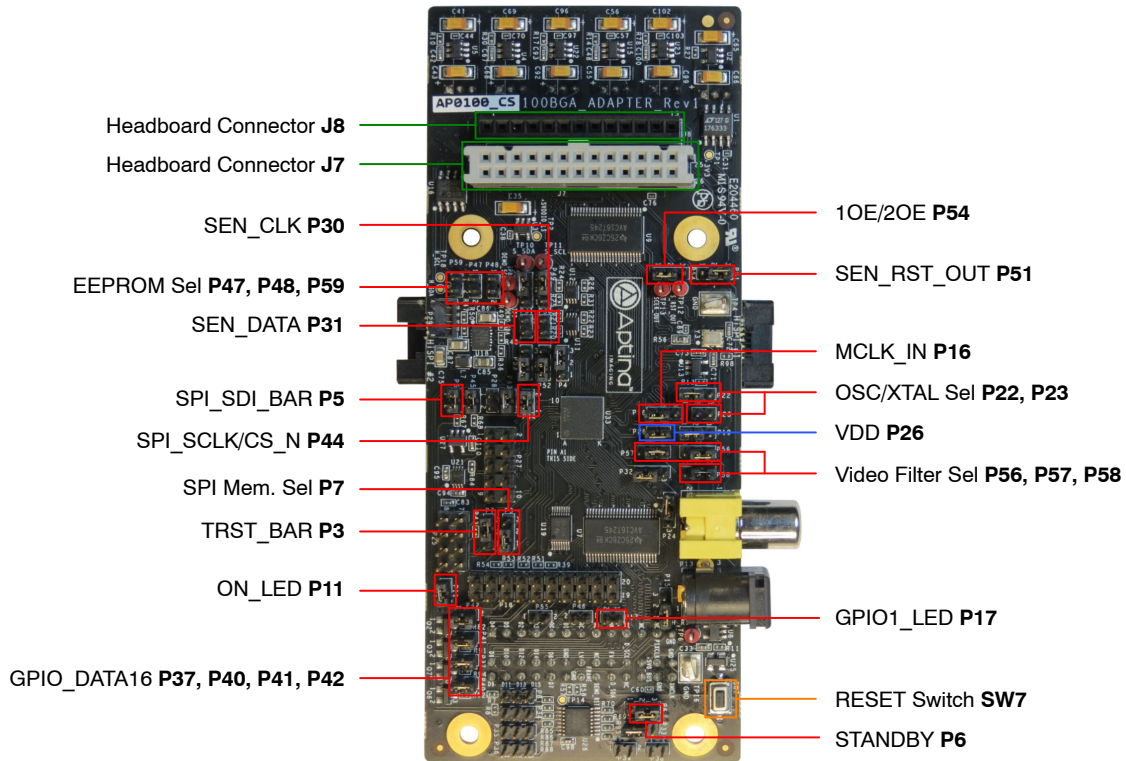


Figure 3. Top View of the Board with Default Jumpers

Bottom View

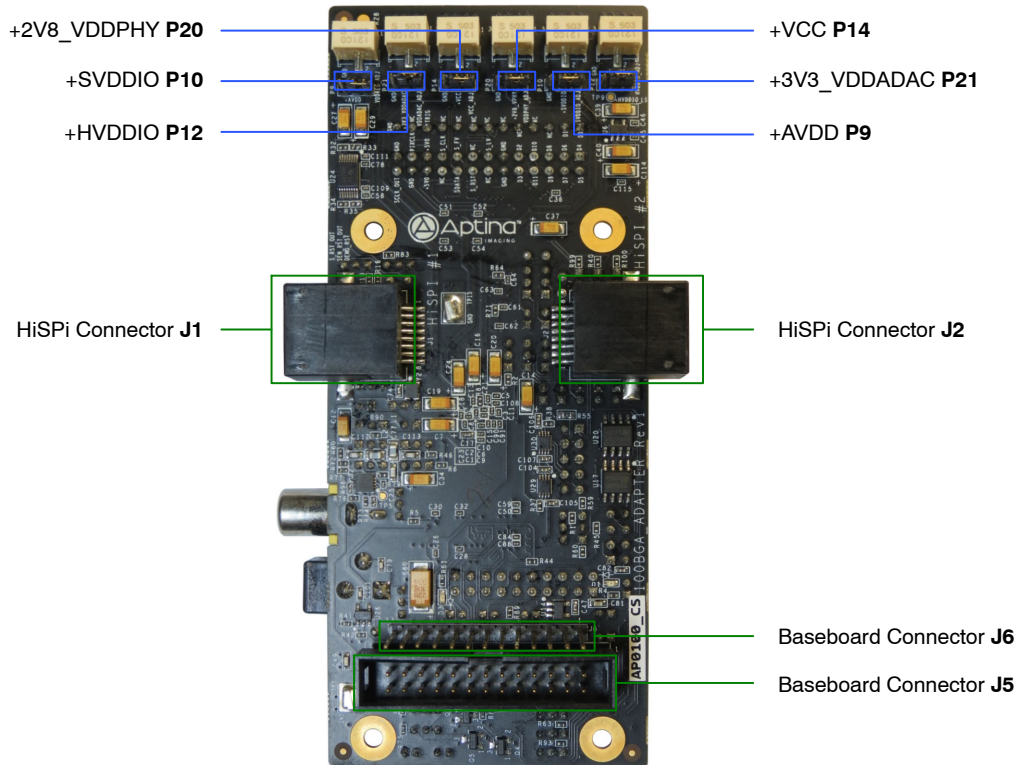


Figure 4. Bottom View of the Board

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

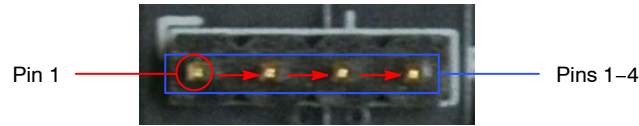


Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

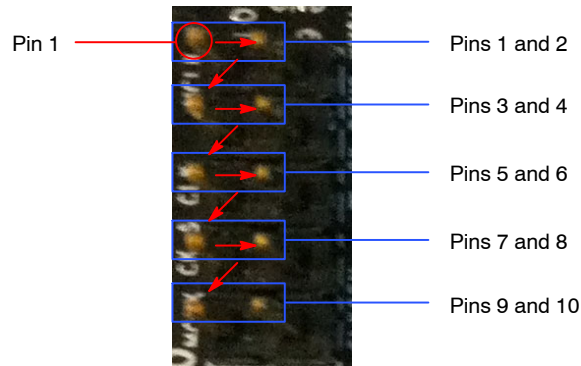


Figure 6. Pin Locations and Assignments of Grouped Jumpers. Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

| Jumper/Header No. | Jumper/Header Name | Pins | Description |
|-------------------|----------------------|------------------|--|
| P3 | TRST_BAR | Open | OTPM Programming Voltage Not Supplied |
| | | 2-3 (Default) | Set to Normal Mode |
| P4 | SADDR | Open | Set to Test Mode |
| | | Open | Analog Test 1 Header |
| P5 | SPI_SDI_BAR | 1-2 (Default) | GND; AP0100 in Host Mode |
| | | Open | SPI_SDI_SEL; AP0100 in Flash Mode |
| P6 | STANDBY | 2-3 (Default) | Active Mode |
| | | 1-2 | Standby Mode |
| | | Open | I ² C IO Expander Control |
| P7 | SPI Memory Selection | 2-3 (Default) | EEPROM Disable/Flash Enable |
| | | 1-2 | Flash Disable/EEPROM Enable |
| P8 | GPIO_5 | Open (Default) | Serial IO expander Control |
| | | 1-2 | Set to Normal |
| | | 2-3 | Set to Vertical Flip |
| P9 | +AVDD | Closed (Default) | Connects to On-Board Regulator +1V8, Internal Regulator Use |
| | | Open | Disconnects from On-Board Regulator +1V8, External Regulator Use |
| P10 | +SVDDIO | 3-5 | Select Demo 3 Baseboard Clock |
| | | 2-4 | Select Slave Clock (for Slave Sensor in Multi-Camera Mode) |

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Table 1. JUMPERS AND HEADERS (continued)

| Jumper/Header No. | Jumper/Header Name | Pins | Description |
|-------------------|---------------------------|-----------------------------|--|
| P11 | ON_LED | 1–2 (Default) | Connects to On-Board to Indicate Power On |
| P12 | +HVDDIO | 1–2 (Default) | Connects to On-Board +HVDDIO Power Supply |
| | | 2–3 | External Power Supply Connection |
| P14 | +VCC | 1–2 (Default) | Connects to On-Board +VCC Power Supply |
| | | 2–3 | External Power Supply Connection |
| P15 | +5V0 | 1–2 (Default) | USB +5V0_BUS Power Supply Connection |
| | | 2–3 | Connects to On-Board +5V0_EXT Power Supply |
| P16 | MCLK_IN | 1–2 (Default) | Connects to On-Board Oscillator |
| | | 2–3 | Connects to XMCLK (i.e. Clock Signal from Demo 2 Baseboard) |
| P17 | GPIO1_LED | Open (Default) | Off Frame LED |
| | | Closed | On Frame LED |
| P19 | +AVDD | Closed (Default) | Connects to On-Board Regulator +1V8, Internal Regulator Use |
| | | Open | Disconnects from On-Board Regulator +1V8, External Regulator Use |
| P20 | +2V8_VDDPHY | 1–2 (Default) | Connects to On-Board +2V8_VDDPHY Power Supply |
| | | 2–3 | External Power Supply Connection |
| P21 | +3V3_VDDADAC | 1–2 (Default) | Connects to On-Board +3V3_VDDADAC Power Supply |
| | | 2–3 | External Power Supply Connection |
| P22, P23 | Oscillator/Xtal Selection | P22 1–2, P23 Open (Default) | Selects Oscillator as AP0100 Input Clock |
| | | P22 2–3, P23 Closed | Selects Crystal as AP0100 Input Clock |
| P24 | EXT_REG | 1–2 (Default) | Internal Regulator |
| | | 2–3 | External Regulator |
| P26 | VDD | 1–2 (Default) | Internal Regulator +1V2_VDD |
| | | 2–3 | External On-Board Regulator U2 Set +1V2 |
| P28 | UART Transceiver | Open (Default) | Turn off UART Transceiver |
| | | Closed | Turn on UART Transceiver |
| P30 | SEN_CLK | Open (Default) | Beagle Serial No Access to Demo 2X & Sensor |
| | | 1–2 | Beagle Serial Access to Demo 2X & Sensor |
| P31 | SEN_DATA | Open (Default) | Beagle Serial No Access to Demo 2X & Sensor |
| | | 1–2 | Beagle Serial Access to Demo 2X & Sensor |
| P32 | ENLDO | 1–2 (Default) | Enable Internal Regulator |
| | | 2–3 | Disable Internal Regulator |
| P33 | GPIO1_LED | 1–2 | Set to GPI |
| | | 2–3 | Set to GPO |
| P34 | GPIO_4 | Open (Default) | Serial IO Expander Control |
| | | 1–2 | Set to Normal |
| | | 2–3 | Set to Horizontal Mirror |
| P35 | GPIO_3 | Open (Default) | Serial IO Expander Control |
| | | 1–2 | Set to NTSC |
| | | 2–3 | Set to PAL |
| P36 | GPIO_2 | Open (Default) | Serial IO Expander Control |
| | | 1–2 | Set to No Pedestal |
| | | 2–3 | Set to Pedestal |
| P37 | GPIO_DATA16 | 1–2 (Default) | Auto-Configuration Access |
| | | Open | JTAG/UART Access |

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Table 1. JUMPERS AND HEADERS (continued)

| Jumper/Header No. | Jumper/Header Name | Pins | Description |
|-------------------|--|--------------------------------|--|
| P38, P39 | IO Expander U38 Setting | P39 Open, P38 Closed (Default) | EEPROM Address Set to 0x48 |
| | | P39 Open, P38 Open | EEPROM Address Set to 0x4C |
| | | P39 Closed, P38 Open | EEPROM Address Set to 0x44 |
| | | P39 Closed, P38 Closed | EEPROM Address Set to 0x40 |
| P40 | GPIO_DATA17 | 1–2 (Default) | Auto-Configuration Access |
| | | Open | JTAG/UART Access |
| P41 | GPIO_DATA18 | 1–2 (Default) | Auto-Configuration Access |
| | | Open | JTAG/UART Access |
| P42 | GPIO_DATA19 | 1–2 (Default) | Auto-Configuration Access |
| | | Open | JTAG/UART Access |
| P43 | SP1_SDO/SDI | 1–2 (Default) | Beagle SPI No Access to Sensor SPI |
| | | Open | Beagle SPI Access to Sensor SPI |
| P44 P44 | SP1_SCLK/CS_N | 1–2 (Default) | Beagle SPI No Access to Sensor SPI |
| | | Open | Beagle SPI Access to Sensor SPI |
| P45 | SPI_SDI | Open (Default) | Data or GND; AP0100 in Flash/Host Mode |
| | | 1–2 | High Z; AP0100 in Auto-Config Mode |
| P47, P48, P59 | Serial I ² C EEPROM Address | P47 Closed, P48 Open, P59 Open | EEPROM Address Set to 0xAA (Default) |
| | | P47 Closed, P48 Open, P59 Open | EEPROM Address Set to 0xA2 |
| | | P47 Open, P48 Closed, P59 Open | EEPROM Address Set to 0xA6 |
| | | P47 Open, P48 Open, P59 Open | EEPROM Address Set to 0xAE |
| P49 | SEN_SCLK | 2–3 (Default) | AP0100 Serial Control |
| | | 1–2 | Demo 2X Serial Control |
| P50 | SEN_SDATA | 2–3 (Default) | AP0100 Serial Control |
| | | 1–2 | Demo 2X Serial Control |
| P51 | SEN_RST_OUT | 2–3 (Default) | AP0100 Reset |
| | | 1–2 | Demo 2X Reset |
| P52 | BEAGLE_SCL | 1–2 (Default) | Demo 2X Accessed |
| | | 2–3 | Sensor Accessed |
| P53 | BEAGLE_SDA | 1–2 (Default) | Demo 2X Accessed |
| | | 2–3 | Sensor Accessed |
| P54 | 1OE/2OE | 1–2 (Default) | Enable Level Transistor U9 |
| | | 2–3 | Disable Level Transistor U9 |
| P56, P57, P58 | Video Filter Selection | 1–2 (Default) | Active Low Pass Filter |
| | | 2–3 | Discrete Low Pass Filter |
| SW7 | RESET | N/A | When Pushed, 240 ms Reset Signal will be Sent to AP0100 Chip |

Interfacing to ON Semiconductor Demo 2X Baseboard

The ON Semiconductor 2X baseboard has a similar 26-pin connector and 13-pin connector which mate with J5

and J6 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

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