NCP3065D3SLDGEVB

High Brightness LED SEPIC Driver Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Circuit Description

This circuit is intended for driving high power LEDs, such as the Cree XLAMP™ series, Lumileds LUXEON® Rebel and K2 and OSRAM, Golden and Platinum DRAGON® as well as the OSTAR®. It is designed for such wide input nominal 12 Vdc applications as automotive and low voltage lighting (12 Vdc/12 Vac). An optional dimming PWM input is included. The circuit is based on NCP3065 operation at 250 kHz in a non-isolated configuration. The primary advantages of this circuit are in the wide input voltage range, wide output voltage range, and in its high efficiency.

A pulse feedback resistor (R8) is used to vary the slope of the oscillator ramp, achieving duty cycle control and steady switching frequency over a wide input voltage range.

Key Features

- Buck-Boost Operation
- Wide Input and Output Operation Voltage
- Regulated Output Current
- Dimming
- High Frequency Operation
- Minimal Input and Output Current Ripple
- Open LED Protection
- Output Short Circuit Protection

Minimum Efficiency	70%

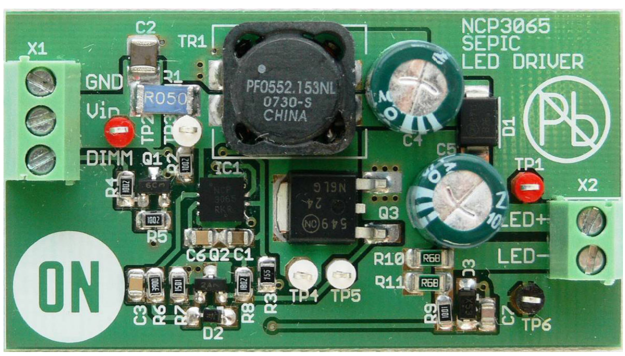

Figure 1. NCP3065 Top Side

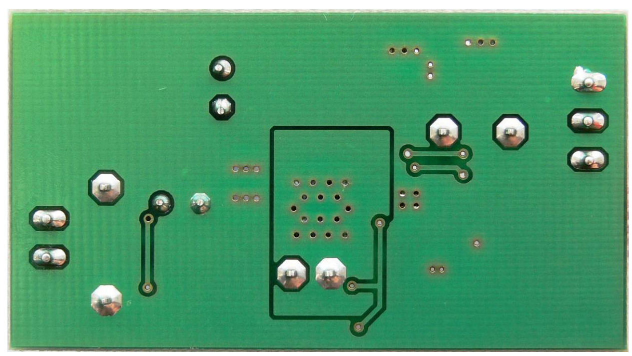

Figure 2. NCP3065 Bottom Side

Device	Application	Input Voltage	Output Power	Topology	I/O Isolation
NCP3065 NCV3065	Solid State, Automotive and Marine Lighting	8–25 V	< 15 W	SEPIC	None

Table 1. Other Specifications

	Output 1	Output 2	Output 3	Output 4
Output Voltage	7.2–23 V	N/A	N/A	N/A
Current Ripple	< 15%	N/A	N/A	N/A
Nominal Current	0.35, 0.7 A	N/A	N/A	N/A
Max Current	1 A	N/A	N/A	N/A
Min Current	N/A	N/A	N/A	N/A

Schematic

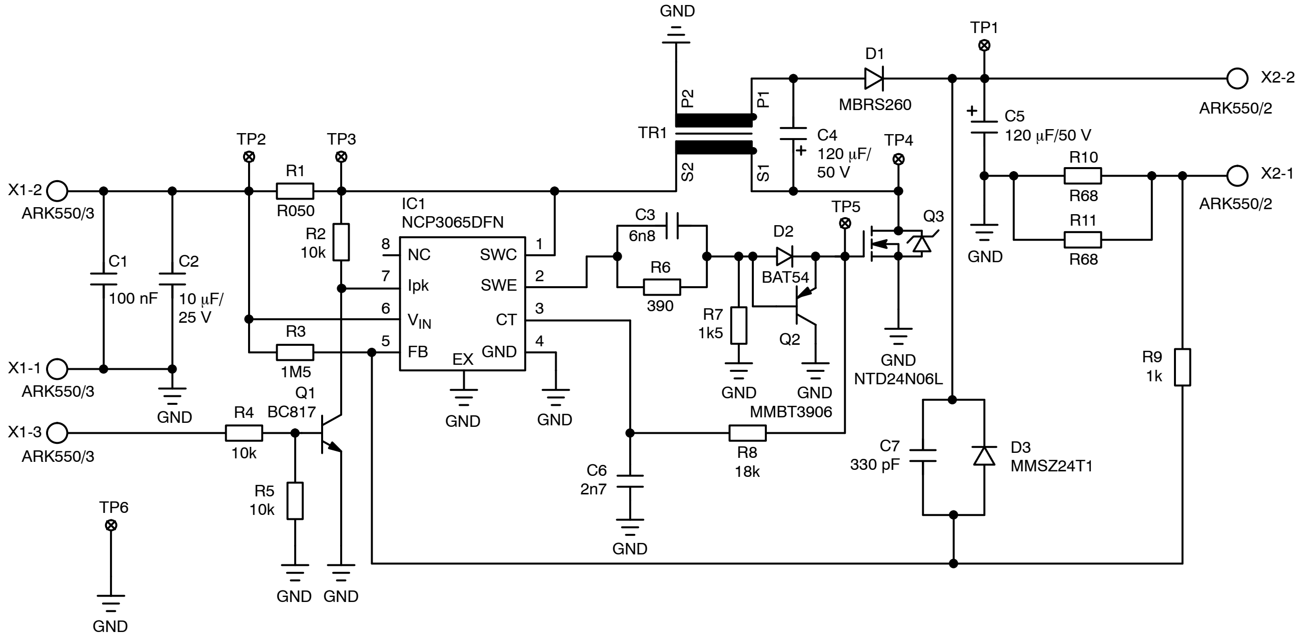

Figure 3. SEPIC Converter Schematic

Design Notes

A SEPIC (single-ended primary inductance converter) is distinguished by the fact that its input voltage range can overlap the output voltage range. The basic schematic is shown in Figure 4.

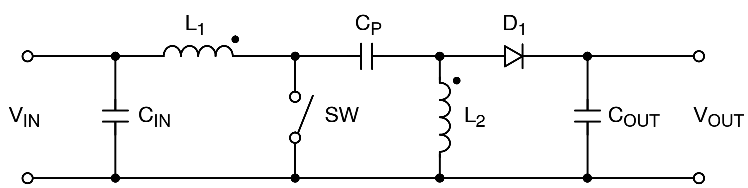

Figure 4. Generalized SEPIC Schematic

When switch SW is ON, energy from the input is stored in inductor L_1. Capacitor C_P is connected in parallel to L_2, and energy from C_P is transferred to L_2. The voltage across L_2 is the same as the C_P voltage, which is the same as the input voltage. At this time, the diode is reverse biased and C_{OUT} supplies output current.

If the switch SW is OFF, current in L_1 flows through C_P and D_1 then continues to the load and C_{OUT}. This current recharges C_P for the next cycle. Current from L_2 also flows through D_1 to the load and C_{OUT} that is recharging for the next cycle.

Inductors L_1 and L_2 could be uncoupled, but then they must be twice as large as if they are coupled. Another advantage is that if coupled inductors are used there is very small input current ripple.

Values of coupled inductors are set by these equations:

$$D = \frac{V_{OUT}\,\text{min}}{V_{OUT}\,\text{min} + V_{IN}\,\text{min}} = \frac{7.2}{7.2 + 8} = 0.47 \qquad \text{(eq. 1)}$$

$$\Delta I = r \times I_{OUT}\frac{D}{1 - D} = 0.8 \times 0.7 \times \frac{0.47}{1 - 0.47} = \\ = 0.51\ \text{A} \qquad \text{(eq. 2)}$$

$$L_{1,2} = \frac{V_{IN}\,\text{min} \times D}{2 \times f \times \Delta I} = \frac{8 \times 0.47}{2 \times 250 \times 10^3 \times 0.51} = \\ = 15.0\ \mu\text{H} \qquad \text{(eq. 3)}$$

where r is the maximum inductor current ripple factor.

For a 0.35 A output current variant of this circuit, the values of inductors are

$$\Delta I = r \times I_{OUT}\frac{D}{1 - D} = 0.95 \times 0.35 \times \frac{0.47}{1 - 0.47} = \\ = 0.3\ \text{A} \qquad \text{(eq. 4)}$$

$$L_{1,2} = \frac{V_{IN}\,\text{min} \times D}{2 \times f \times \Delta I} = \frac{8 \times 0.47}{2 \times 250 \times 10^3 \times 0.3} = \\ = 25.1\ \mu\text{H} \qquad \text{(eq. 5)}$$

The nearest coupled inductor value for the 0.7 A variant is 15 μH. A variant with 0.35 A output current needs to use inductors with value 22 μH.

The output current is set by R10 (R11). So this resistor can be calculated by the formula:

$$R10 = \frac{0.235}{I_{OUT}} = 350\ m\Omega \qquad \text{(eq. 6)}$$

To protect the circuit against high output voltage under light loads or a fault condition, the output voltage is clamped by a Zener diode (D3) to approximately 24.5 V. Capacitor C7 is used to stabilize feedback, but it impacts line regulation. R3 fixes the line regulation error caused by C7.

External power MOSFET is driven by internal NPN Darlington transistor, external diode D2 and PNP transistor Q2. Compensated divider C3, R6 and R7 is used to reduce gate-source voltage, mainly for high input voltage and to keep sharp edges. Maximum gate-source voltage can be calculated by this formula:

$$V_{GS}\max = \left(V_{IN} - V_{CE} - V_{D2}\right) \times \frac{R7}{R6 + R7} = (27 - 1.4 - 0.4) \times \frac{1500}{390 + 1500} = 18.4\ V \qquad \text{(eq. 7)}$$

Maximum MOSFET current can be calculated in this way:

$$I_{Q4max} = \left(1 + \frac{r}{2}\right) \times I_{OUT} \times \frac{V_{OUT}\max}{V_{IN}\min} = \left(1 + \frac{0.8}{2}\right) \times 0.7 \times \frac{23}{8} = 2.5\ A \qquad \text{(eq. 8)}$$

To minimize power MOSFET conductance losses, it is recommended to select a transistor with small R_{DSON}. To minimize switching losses, it is recommended to select a transistor with small gate charge. Power MOSFET must also have a breakdown voltage higher than:

$$V_{FETPK} = V_{IN} + V_{OUT} = 18 + 23 = 41\ V \qquad \text{(eq. 9)}$$

Cycle by cycle switch current protection is set by R1 at

$$I_{PKset} = \frac{0.2}{R1} \qquad \text{(eq. 10)}$$

A suitable value is higher than maximum switch current.

$$R1 < \frac{0.2}{I_{Q1_{max}}} = \frac{0.2}{2.5} = 80\ m\Omega \qquad \text{(eq. 11)}$$

Diode D1 maximum voltage is determined by this equation:

$$V_{D1max} = V_{IN} + V_{OUT} = 18 + 32 = 41\ V \qquad \text{(eq. 12)}$$

and with current

$$I_{D1} = I_{OUT} = 0.7\ A \qquad \text{(eq. 13)}$$

The C4 coupling capacitor is selected based on input voltage and on current

$$D\max = \frac{V_{OUT}\max}{V_{OUT}\max + V_{IN}\min} = \frac{23}{23 + 8} = 0.74 \qquad \text{(eq. 14)}$$

$$I_{C4RMS} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \sqrt{\frac{1 - D\max}{D\max}} = \frac{23 \times 0.7}{8} \sqrt{\frac{1 - 0.74}{0.74}} = 1.2\ A \qquad \text{(eq. 15)}$$

and its minimal value is

$$C4 > \frac{I_{OUT} \times D\min}{0.05 \times V_{IN}\min \times f} = \frac{0.7 \times 0.47}{0.05 \times 8 \times 250 \times 10^3} = 2\ \mu F \qquad \text{(eq. 16)}$$

The output capacitor's current is

$$I_{C5} = I_{OUT} \sqrt{\frac{D\max}{1 - D\max}} = 0.7 \sqrt{\frac{0.74}{1 - 0.74}} = 1.2\ A \qquad \text{(eq. 17)}$$

$$C5 > \frac{\frac{V_{OUT}\min}{V_{IN}\min} \times I_{OUT} \times D\min}{f \times r \times V_{OUT}\min} = \frac{\frac{7.3}{8} \times 0.7 \times 0.47}{250 \times 10^3 \times 0.1 \times 7.3} = 1.7\ \mu F \qquad \text{(eq. 18)}$$

The value could be much larger for higher stability, but a higher value impacts the dimming function at low duty cycle.

The resistor R8 is used to stabilize feedback loop. Used value is compromise for whole input and output voltage range. If this circuit is used for specified load only, it should be tuned by this resistor to better efficiency and line regulation.

X1-3 input is used for dimming. The dimming signal level is 2−10 V. The recommended dimming frequency is about 200 Hz. For frequencies below 100 Hz the human eye will see the flicker. The dimming function utilizes the NCP3065's peak current protection input. The second way to achieve this is to use the FB pin. See Figure 12.

Conclusion

This circuit is ideal in applications with strings of two to six LED chips powered from a power supply with wide input range (8-20 V). The advantages of this circuit include its small size, low price, wide input and output voltage ranges, and very small input current ripple.

PC BOARD

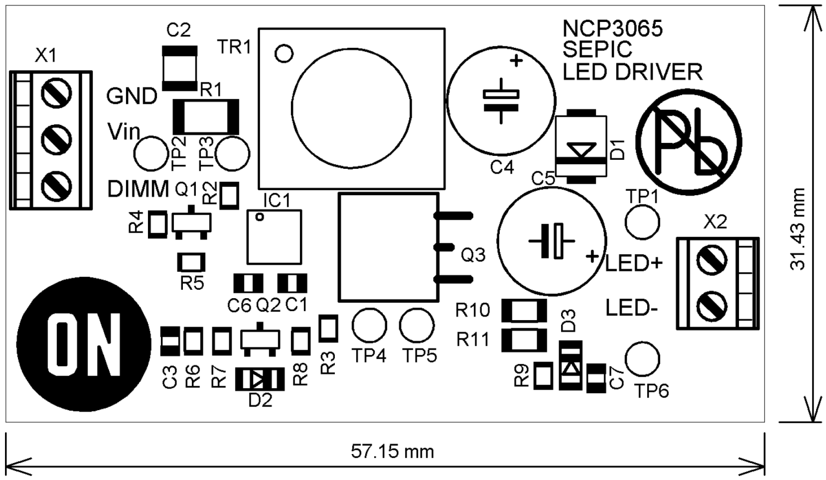

Figure 5. Components Position on PCB

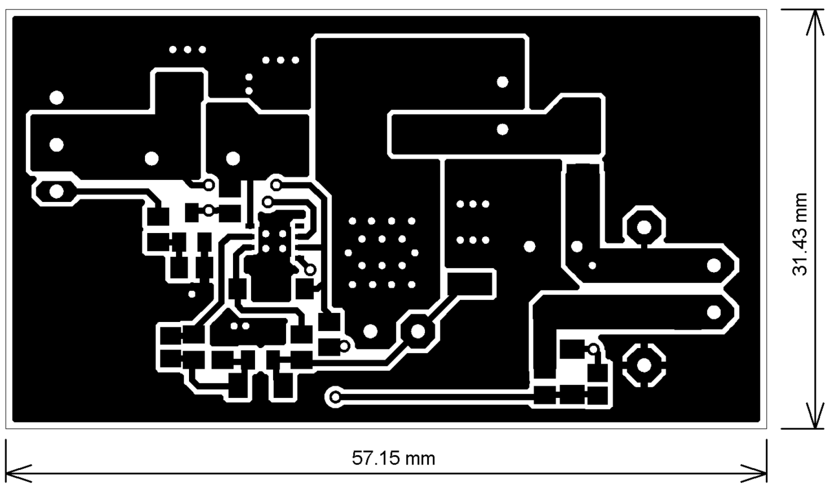

Figure 6. PCB's Top Side

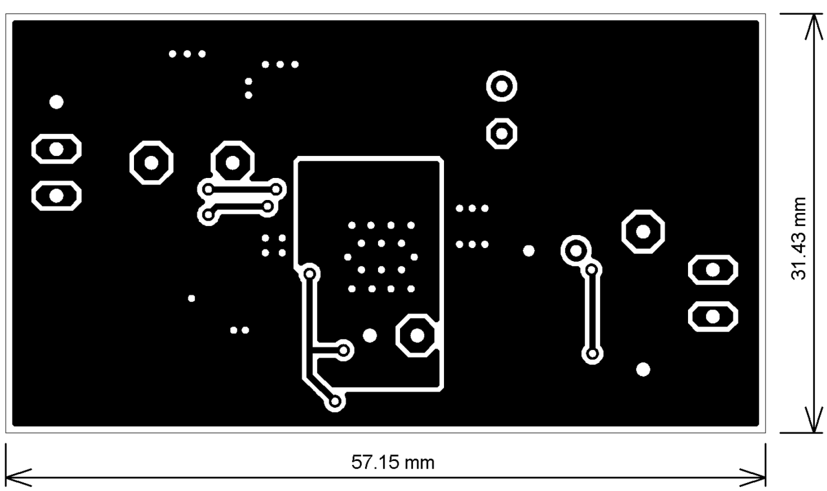

Figure 7. PCB's Bottom Side

Table 2. BILL OF MATERIALS

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
R3	1	Resistor SMD	1M5	1%	0805	Vishay	CRCW08051M50FKEA	Yes	Yes
R9	1	Resistor SMD	1k	1%	0805	Vishay	CRCW08051K00FKEA	Yes	Yes
R7	1	Resistor SMD	1k5	1%	0805	Vishay	CRCW08051K50FKEA	Yes	Yes
C6	1	Ceramic Capacitor SMD	2n7	5%	0805	Murata	GCM2165C1H272JA16D	Yes	Yes
C3	1	Ceramic Capacitor SMD	6n8	10%	0805	Kemet	C0805C682K5RAC	Yes	Yes
R2, R4, R5	3	Resistor SMD	10k	1%	0805	Vishay	CRCW080510K0FKEA	Yes	Yes
C2	1	Ceramic Capacitor SMD	10 μF/50 V	+80% / −20%	1210	Murata	GRM32NF51E106ZA01L	Yes	Yes
R8	1	Resistor SMD	27k	1%	0805	Vishay	CRCW080527K0FKEA	Yes	Yes
C1	1	Ceramic Capacitor SMD	100 nF	5%	0805	Kemet	C0805C104J5RAC	Yes	Yes
C4, C5	2	Ceramic Capacitor SMD	120 μF/50 V	20%	8x15	Koshin	KZH-50V121MG4	Yes	Yes
C7	1	Capacitor	330 pF	5%	0805	Kemet	C0805C331J5GAC-TU	Yes	Yes
R6	1	Resistor SMD	390R	1%	0805	Vishay	CRCW0805390RFKEA	Yes	Yes
X2	1	Inlet Terminal Block	DG350-3.50-02	–	–	Degson	DG350-3.50-02	Yes	Yes
X1	1	Outlet Terminal Block	DG350-3.50-03	–	–	Degson	DG350-3.50-03	Yes	Yes
D2	1	Schottky Diode 30 V	BAT54HT1G	–	SOD-323	ON Semiconductor	BAT54HT1G	No	Yes
Q1	1	General Purpose Transistor NPN	BC817-40LT1G	–	SOT-23	ON Semiconductor	BC817-40LT1G	No	Yes
D1	1	Surface Mount Schottky Power Rectifier	MBRS260T3G	–	SMB	ON Semiconductor	MBRS260T3G	No	Yes
Q2	1	PNP General Purpose Transistor	MMBT3906LT1G	–	SOT-23	ON Semiconductor	MMBT3906LT1G	No	Yes
D3	1	Zener Diode 500 mW 24 V	MMSZ24T1G	5%	SOT-123	ON Semiconductor	MMSZ24T1G	No	Yes
IC1	1	Constant Current Switching Regulator	NCV3065MNTXG	–	DFN	ON Semiconductor	NCV3065MNTXG	No	Yes
Q3	1	Power MOSFET 24 Amps, 60 V, Logic Level, N-Channel	NTD24N06LT4G	–	DPAK	ON Semiconductor	NTD24N06LT4G	No	Yes
R1	1	Resistor SMD	0R050	1%	2010	Welwyn	LR2010-R05FW	Yes	Yes
R10, R11	2	Resistor SMD	0R68	5%	1206	Tyco Electronics	RL73K2BR68JTD	Yes	Yes
TP1, TP2, TP3, TP4, TP5, TP6	6	Test Point	Terminal, PCB Black PK100	–	1.02 mm	Vero	20-2137	Yes	Yes
TR1	1	Transformer for 0.35 A Version	PF0553.223	–	–	Pulse	PF0553.223	No	Yes
TR1	1	Transformer for 0.7 A Version	PF0553.153	–	–	Pulse	PF0553.153	No	Yes

MEASUREMENTS

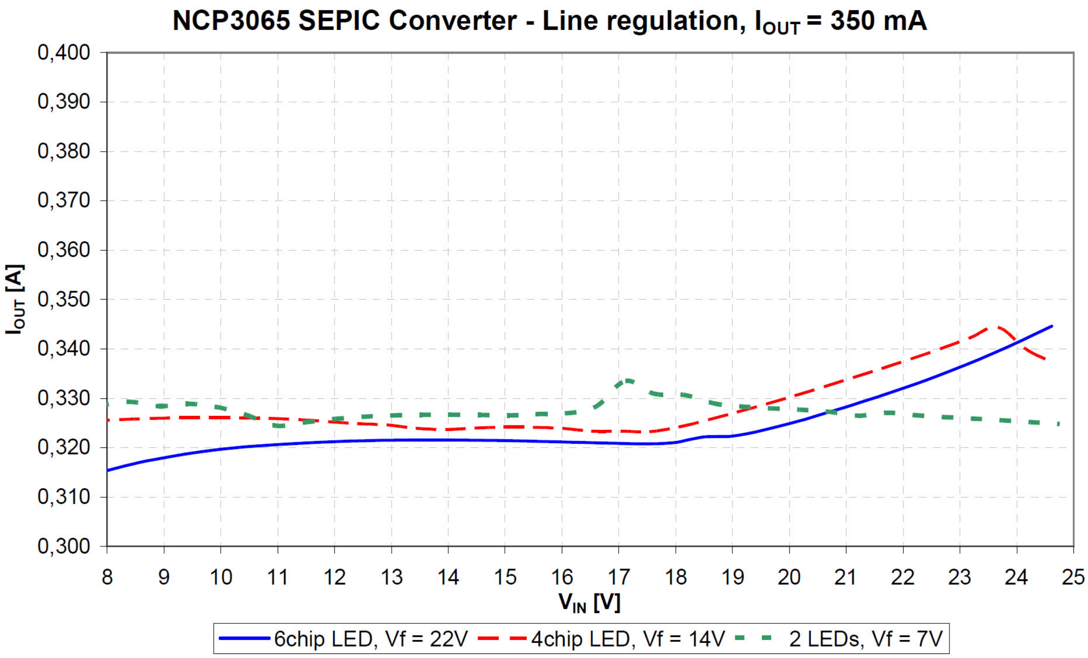

Figure 8. Line Regulation for I_{OUT} = 350 mA

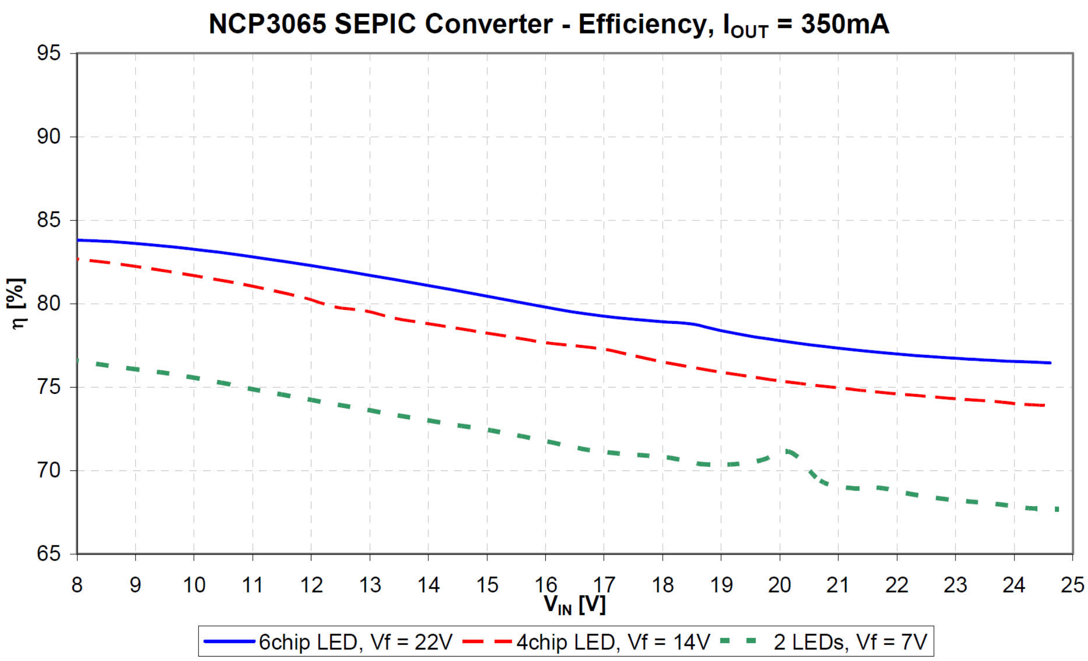

Figure 9. Efficiency for I_{OUT} = 350 mA

MEASUREMENTS

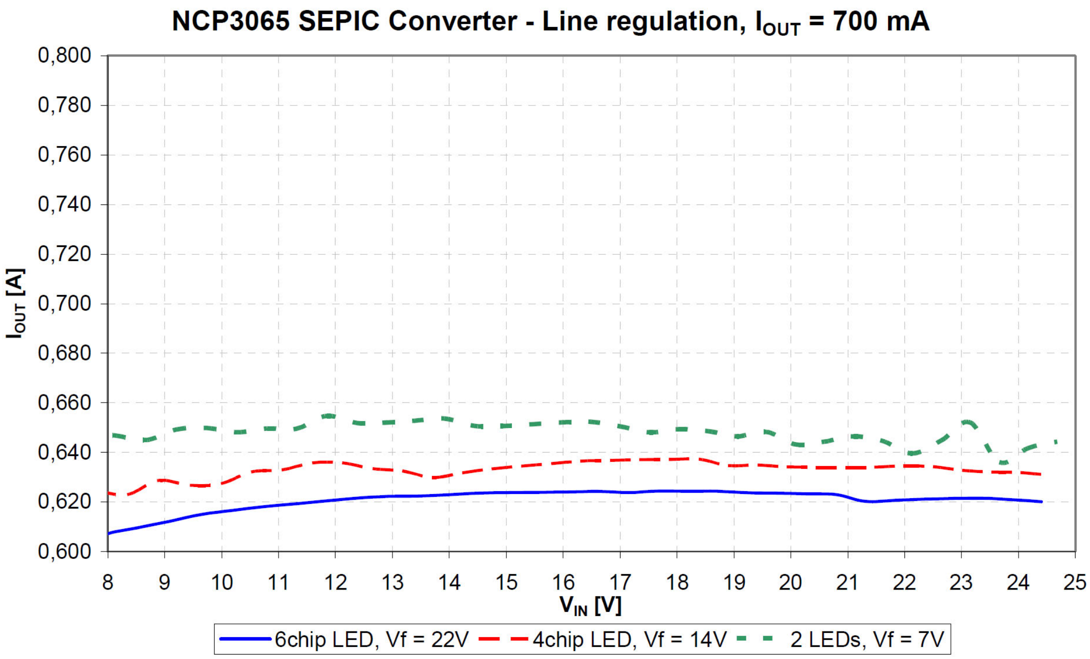

Figure 10. Line Regulation for I_{OUT} = 700 mA

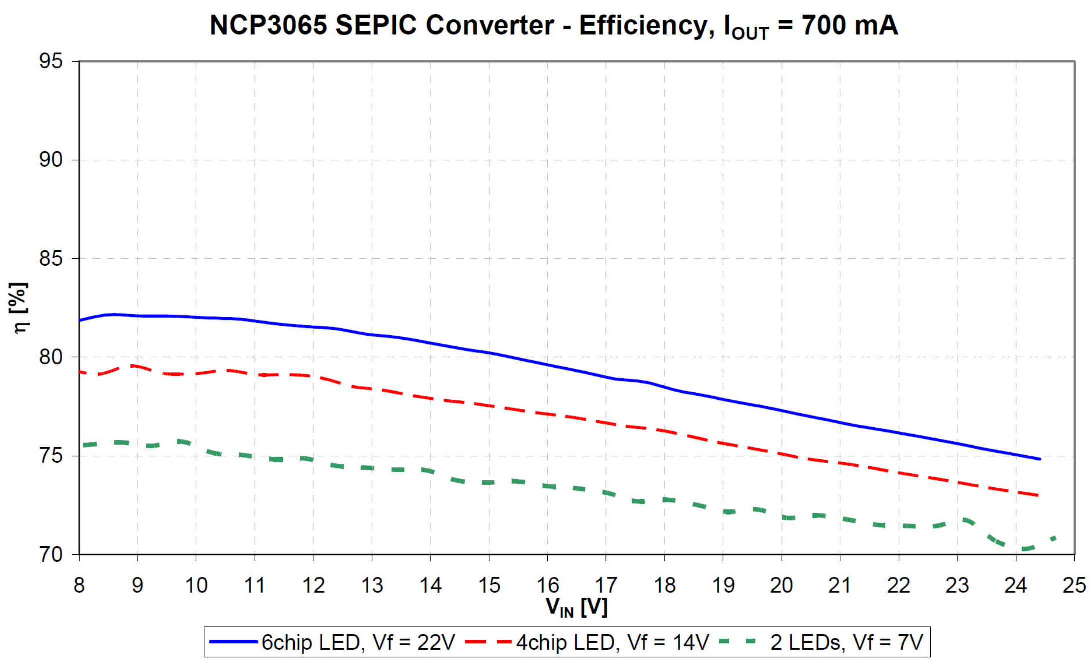

Figure 11. Efficiency for I_{OUT} = 700 mA

MEASUREMENTS

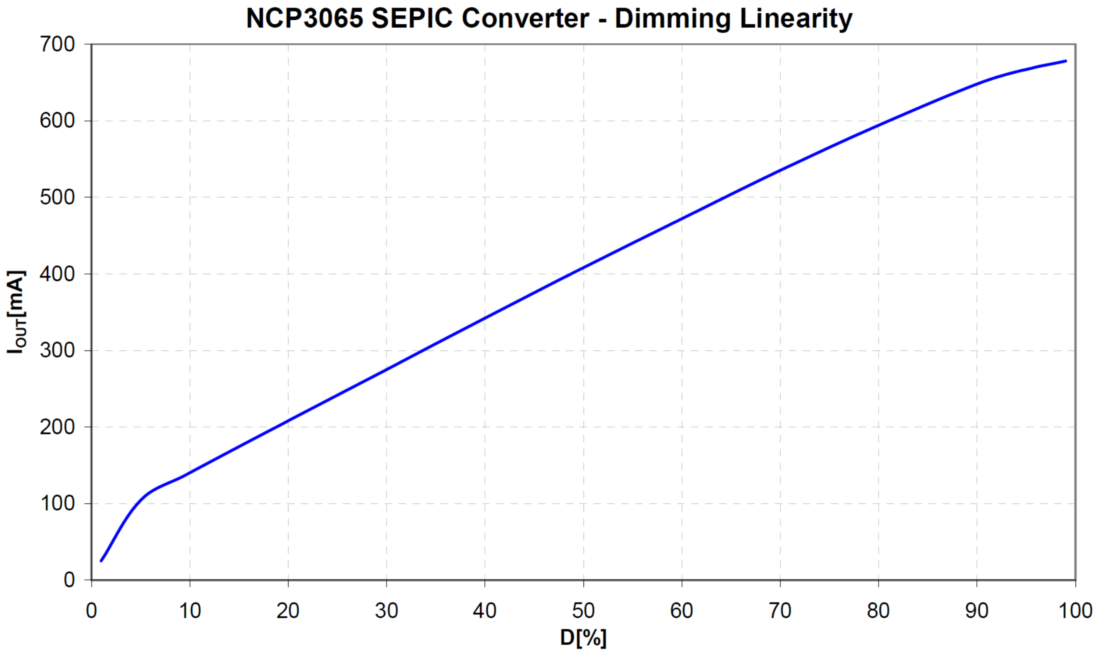

Figure 12. Dimming Linearity, Dimming Frequency 200 Hz

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